Organic thin-film transistors (OTFTs) are promising devices for future low-cost electronics\cite{1}\cite{2}. However, to enable the development of this technology, circuit design simulation is needed. TCAD with MixedMode approach provides a suitable route for the physics based simulation of these transistors within simple circuits. As circuits become more complicated, more devices are needed and the computing time increases significantly. Compact models describe the behavior of the device with only a few equations and thus the computing time is reduced to a viable magnitude. Such equations are written down in a Verilog-A format which can be used by most SPICE simulators.

These compact models have to be verified through comparison with measurements and/or TCAD simulation data. A MixedMode simulation provides a small SPICE-like circuit with TCAD devices.

In this article MixedMode is used to simulate a CMOS inverter circuit as in Figure 1 with two OTFTs, both of which are expressed as TCAD models using the Atlas simulator. Ultimately, four CMOS inverters are simulated with the following channel lengths of 0.3, 1, 2 and 10 microns. Subsequently the compact model is fitted to the MixedMode simulation data of the CMOS inverter with a channel length of 2 microns. The further scaling from 10 microns down to 0.3 microns simulations were done using the same fitting parameters in order to test the scalability of the proposed compact model.

**Compact Model**

The investigated compact model is a charge-based model derived by Franziska Hain \cite{3}. It is based on the well-known equations in terms of drift-diffusion transport of free carriers \cite{3}. If the charge-density expressions \( Q'_{ms} \) and \( Q'_{md} \) at the source/drain end of the channel are known, then the transistor current can be calculated as follows:

\[
I_{ds} = \mu_{eff} W \left( \frac{kT}{q} \cdot \frac{Q'_{ms} - Q'_{md}}{L} + \frac{Q'^{2}_{ms} - Q'^{2}_{md}}{2LC'_{ox}} \right)
\]

Additionally the charge-carrier mobility \( \mu_{eff} \), device width \( W \), channel length \( L \), temperature \( T \) and the oxide capacity-density \( C'_{ox} \) along the channel is necessary. The corresponding equations for \( Q'_{ms} \) and \( Q'_{md} \) depend on the slope \( S \), the threshold voltage \( V_T \) and the bias conditions \( V \) \cite{3}:

\[
Q'_{ms/d} = \frac{S}{\ln(10)} C'_{ox} \cdot \text{LambertW}\left\{ \exp\left( \frac{V_{gs/d} - V_T}{S/L} \right) \right\}
\]

The charge-carrier mobility \( \mu_{eff} \) can be modified to implement the influence of a contact resistance \( R_c \), of a first-order approximation \cite{3}:

\[
\mu_{eff} = \frac{\mu}{1 + \frac{W}{L} (R_s + R_c) Q'_{ms}}
\]

Here, \( R_c \) is the constant part of the contact resistance. Parameter \( \mu \) is the mobility of quasi-free carriers, taking into account variable-range hopping transport mechanism of charges in the LUMO of an n-type organic semiconductor. In the model the mobility is replaced by \( \mu_{eff} \) to capture...
the contact resistance influence into the compact model.

A further extension of the compact model assumes a Schottky barrier at the drain/source contacts which due to the barrier lowering effect is reduced by the electric field. This means that the contact resistance at the source end is non-linear and is reduced for increasing bias conditions. This extension enables to capture the s-shape effect on the output characteristic of the transistor that normally appear in short-channel devices. The influence of the Schottky barrier is described as a resistance $R_{sb}$ in the model[4]:

$$R_{sb} = \frac{(V_{gs} - V_T)(1 - f_Q) + f_Q V_{ds}}{tW J_{s0} \exp \left( -\frac{q\Phi_{B0}}{\eta k_B T} \right) \exp \left( \frac{q\Delta\Phi_B}{\eta k_B T} \right)}$$

Here $f_Q$ and $\eta$ are fitting parameter, $t$ is the effective injection length, $J_{s0}$ the current density, $\Phi_{B0}$ is the Schottky barrier height and $\Delta\Phi_B$ is the barrier lowering due to the electric field. This expression is subsequently inserted into the equation to calculate $\mu_{eff}$.

**SmartSpice Simulation**

The simulation of the compact model was done with SmartSpice. Therefore the Verilog-A model has to be loaded at the beginning of the InputFile:

```verbatim
.verilog "OTFT_compact_n.va"
.verilog "OTFT_compact_p.va"
```

In the further definition of the device in the netlist has to be taken into account that Verilog-A models must add the prefix YVLG_ to their name:

```verbatim
Vdd n_Vdd GND 5
Vin n_Gate GND
YVLG_OTFTn n_Out n_Gate n_Vdd OTFT_compact_n
YVLG_OTFTp n_Out n_Gate GND OTFT_compact_p
```

Whereof OTFT_compact_n and OTFT_compact_p are the defined model names inside the files OTFT_compact_n.va and OTFT_compact_p.va. In case of a CMOS inverter like in Figure 1 the netlist is quite simple but for more complicated circuits Gateway is a useful software tool with a Graphical User-Interface.

Ultimately, the simulation conditions and plot settings:

```verbatim
.dc Vin 0 5 0.001
.iplot v(n_OUT)
```

**TCAD Structure**

The structure in Figure 2 of a staggered device is close to manufactured structures published in [5] was kept as simple as possible and is shown in Figure 3.

The insulator and organic semiconductor (OSC) have the thicknesses of 5.1 nm and 25 nm respectively to match the manufactured device [5]. The same goes for the overlap length of 2 microns. Details of the paper by F. Ante et al. [5] describe the PMOS transistors that use DNTT as OSC and is using AIOx as Insulator.

A CMOS inverter requires a PMOS and a NMOS transistor. The basic structure of both transistors is the same. The transistors differ by their OSC materials. In the TCAD model for these transistors the semiconductor regions were defined as either ‘pentacene’ for the PMOS and ‘organic’ for the NMOS, which is a generic organic semiconductor material. A full material definition was used for the ‘organic’ region. Furthermore, the pentacene material parameters were customised using the material statement to match the experimental data for the PMOS transistor. Once a reasonable match was obtained between the TCAD ATLAS stand alone simulations and the measured data, both structures were deployed in the MixedMode simulations.

**Atlas MixedMode Simulation**

The simulation input deck starting with .begin and finishing with .end, the SPICE-like circuit and simulations conditions are defined. Previously saved structures structure_pmos.str and structure_nmos.str are loaded while
the electronic devices and the respective circuit is defined using the following syntax. Please note in this work the supply voltage is set to 5 V:

\[
\begin{align*}
\text{vdd} & \text{ n_vdd} \text{ GND} \ 5 \\
\text{vin} & \text{ n_in} \text{ GND} \ 0 \\
\text{atftp} & \text{ n_in}=\text{gate} \text{ n_vdd}=\text{source} \text{ n_out}=\text{drain} \\
& \text{infile}=\text{structure_pmos.str width=1} \\
\text{atftn} & \text{ n_in}=\text{gate} \text{ GND}=\text{source} \text{ n_out}=\text{drain} \\
& \text{infile}=\text{structure_nmos.str width=1}
\end{align*}
\]

After that, the simulation conditions as a DC voltage sweep from 0 V to 5 V in a stepsize of 1 mV are defined as well as the name of the appropriate output file:

\[
\begin{align*}
\text{.nodeset} & \text{ v(n_in)=0 v(n_out)=5 v(n_vdd)=5} \\
\text{.numeric} & \text{ imaxdc=200} \\
\text{.options} & \text{ m2ln print temp=300} \\
\text{.dc} & \text{ vin 0 5 0.001} \\
\text{.log} & \text{ outfile=cmosinv_Lch2microns}
\end{align*}
\]

The corresponding material parameters for the organic semiconductors of the PMOS and NMOS transistor are defined after the MixedMode section using the following syntax [6]:

\[
\begin{align*}
\text{material} & \text{ material=organic affinity}=4.09 \ \text{eg300}=3.38 \text{ permittivity}=3 \ \text{mun}=1 \text{ mup}=1e-9 \ text{nv300}=1e21 \ \text{nc300}=1e21 \\
\text{material} & \text{ material=pentacene affinity}=1.81 \ \text{eg300}=3.38 \text{ permittivity}=3 \ \text{mun}=1e-9 \text{ mup}=1 \text{ nv300}=1e21 \ \text{nc300}=1e21 \\
\text{material} & \text{ material=SiO2 permittivity}=4.08
\end{align*}
\]

The OSCs distinguish in their charge-carrier mobility. The material ‘pentacene’ is used for the PMOS transistor and the ‘organic’ material is eventually allocated to the NMOS transistor.

The OTFT in [5] exhibits an s-shape effect in its output characteristic, an assumed Schottky barrier of $\Phi_{bn} = 0.55$ eV between the source/drain contacts and the OSC leads to a similar behavior of the TCAD simulation to measurements. It is implemented by an appropriate work function at the contacts:

\[
\begin{align*}
\text{contact} & \text{ name=source workfunction}=5.355 \ \text{device=atfn} \\
\text{contact} & \text{ name=source workfunction}=4.64 \ \text{surf.rec alt.barrier} \ \text{device=atfn} \\
\text{contact} & \text{ name=drain workfunction}=4.64 \ \text{surf.rec device=atfn}
\end{align*}
\]

**Simulation Results**

Figure 4 shows the output characteristics of the CMOS inverters. The solid lines are the inverter using TCAD devices and the dashed lines are computed with the compact model. During the transition area from 1 V to 2.5 V the output voltage $V_{out}$ of the compact model is slightly above the TCAD simulation data. The same deviation can be seen between 2.5 V and 4 V. Nevertheless, the deviation is still within acceptable limits.

![Figure 4. Comparison between the TCAD and compact-model inverter with various channel length from 10 µm down to 0.3 µm.](image)

**Summary**

This article demonstrates how the MixedMode extension of Atlas can be used to simulate a simple digital circuit like a CMOS inverter which further can be used to verify a compact model for organic thin-film transistors.
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