a-IGZO TFT Simulation

1. Introduction

The flat panel device for active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diode displays (AMOLEDs) has utilized a low cost amorphous silicon or low temperature poly-silicon (LTPS) as a fast switching transistor in mobile devices, TVs, and other display consumer electronics. Recently, amorphous InGaZnO (a-IGZO) thin-film transistor (TFT) is now one of the most important materials in the display area for flexibility, large-area uniformity and high mobility. The conventional a-Si:H TFT or LTPS devices have many degradation problems such as bias stress and photo induced instabilities that are the most important factors which must be fully understood and analyzed to improve the device design. These instabilities come from time-dependent density of states (DOS) change in forbidden band gap of material during device operation.

This article aims to make a real DOS shape in Atlas device simulation software from experimentally extracted DOS and to reproduce the reference data. From this DOS, we can simulate a-IGZO TFT more correctly and this is the basic start point of further analyzing device instabilities.

2. Simulation Structure

Firstly, we need to extract the correct DOS function in the channel region and at gate insulator interface. After that, we can simulate the effect of this DOS shape to various electrical properties of device. Because a-IGZO TFT device has stability issues such as negative bias temperature, bias-stress effect, and light induced instabilities like a-Si:H TFT from DOS change during device operations, we need to carefully examine this DOS change during device operation.

We simulated 2D Atlas structures to validate the proper model and material parameters such as DOS and especially S/D (source/drain) Schottky barrier height of Molybdinium metal for S/D contact.

For S/D Schottky contact simulation, we used UST (universal Schottky tunneling) model and adjusted the metal work function to be around 5.0eV. The key simulation parameters are listed in Table 1.

The total gate insulator thickness was assumed at equivalent thickness (Tox) of 258nm but in our simulation we adopted double gate insulator of SiNx/SiO2 (400nm/50nm) to make a correct structure.

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3. Density of State (DOS) Extraction

General density of state in bulk a-IGZO forbidden bandgap can be incorporated into Atlas TFT simulator. For example, total acceptor-like traps are the sum of deep-state and shallow states as defined by the following equation.

\[ g_A(E) = g_{DA}(E) + g_{TA}(E) = N_{DA} \times \exp\left(\frac{E - E_c}{kT}\right) + N_{TA} \times \exp\left(\frac{E - E_a}{kT}\right) \] (1)

Here, \( g_{DA}(E) \) is deep-state and \( g_{TA}(E) \) is shallow state. (red color in Figure 3) \( N_{DA} \) and \( N_{TA} \) is maximum traps concentration at \( E=E_c \).

The equivalent interface traps are defined as the sum of donor-like and acceptor-like traps (refer to Figure 3).

\[ D_{it}(E) = D_{itA}(E) + D_{itD}(E) = N_{itA} \times \exp\left(\frac{E - E_c}{kT}\right) + N_{itD} \times \exp\left(\frac{E - E_a}{kT}\right) \] (2)

The total donor-like states in bulk a-IGZO film are defined as the sum of tail distribution from valence band edge and deep Gaussian function shape at fixed position with \( E_{ov} \) (left plot in Figure 3: blue color).

\[ g_{D}(E) = g_{TD}(E) + g_{OV}(E) = N_{TD} \times \exp\left(\frac{E - E_{ov}}{kT}\right) + N_{OV} \times \exp\left(\frac{E - E_{ov}}{kT}\right) \] (3)

After obtaining proper simulation model and parameters through fitting to experimental data, we need to take a look at the more general 2D structures using Athena because CV simulation highly depends on the exact 2D profile such as gate-source/drain overlap and other geometrical effects (Figure 2).

<table>
<thead>
<tr>
<th>A-IGZO affinity(eV)</th>
<th>Gate workfunction(eV)</th>
<th>S/D metal workfunction(eV)</th>
<th>GI permittivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.6</td>
<td>5</td>
<td>5</td>
<td>7(SiNx)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.9(SiOx)</td>
</tr>
</tbody>
</table>

Table 1. Simulation parameters(S/D work function and GI(gate insulator) relative permittivity).
Here, \( g_{TD}(E) \) is shallow trap from valence band edge and \( g_{OV}(E) \) is donor-like with peak position energy of \( E_{OV} \).

Figure 3 shows simulation DOS and reference data. These DOS were used for subsequent simulation tasks to see various effects on the electrical behavior.

We simulated the dependence of donor-like Gaussian traps on \( IDVG \) and \( IDVD \) (Figure 4). When donor-like Gaussian (Nov here) traps is increased then \( IDVG \) is shifted to negative gate bias direction and \( IDVD \) is rapidly increased to higher drain current. When donor-like traps is above \( 1 \times 10^{18} / cm^3 \) then simulated \( IDVG \) differs from reference result of analytical model. It is related to a-IGZO band-gap and position of donor-like traps. If a-IGZO band-gap is fixed at 3.2eV as it can be seen in the DOS plot of the reference paper[1], the most probable cause are the different values of positions of donor-like traps (\( E_{OV} = 2.9eV \)).

When we adjust the peak position of Gaussian profile to a lower value from the conduction band edge (\( \sim 0.15eV \)) then we can reproduce the same trend of \( IDVG \) with different donor-like trap (Figure 4-1). The position of peak Gaussian is a very sensitive parameter which decides the overall device characteristics as shown in the simulation result.

Figure 5 shows the effect of acceptor-like interface trap on the \( IDVG \) shape.

Figure 3. Definition of DOS (Density Of States in forbidden band gap of IGZO active (left is bulk DOS in a-IGZO channel region and right is a-IGZO / gate insulator interface trap. Bottom plot is reference’s extracted DOS by multifrequency CV analysis).
4. Simulation Results

From previous observation about IDVG and IDVG behavior with the DOS shape, we fitted to the experiment data using bulk DOS and a-IGZO/GI interface traps.

Figure 6 shows the simulation result of IDVG as compared to experiment data and differs only below 3.0V at high drain bias (Vd=10.1) which is still unknown mechanism and will be further investigated with the physical model. It may be related to some trap-related leakage current at high drain bias before threshold voltage.

Figure 7 shows that total gate capacitance is very close to the experiment and frequency dispersion is also well reproduced by using 2D Athena structures.

The exact DOS in IGZO channel is commonly verified through CV analysis as reference paper and we also used this experimentally verified in the DOS function in subsequent simulation (Figure 3) using DEFECT and the INTDEFECT statement. In the simulation we have included both bulk DOS in IGZO channel and at interface between a-IGZO active channel and gate insulator.
5. Summary

We studied a-IGZO simulation using 2D Athena structures and reproduced the experiment result. It is believed that the general purpose numerical simulation is the much more powerful tool and accurate description than the analytical model which is described in the reference paper. The position of donor-like traps in forbidden band gap and accurate band gap is a very important factor to characterize device performance. To simulate S/D ohmic contact, we used UST Schottky tunneling model and it properly reproduced the current level with experiments. The correct DOS shape and concentration are key points to accurately simulate a-IGZO thin film transistor as we discussed so far.

This initial DOS could be changed due to various stress conditions and we leave this simulation about dynamic DOS change for subsequent stress simulations.

References
