Single Event Gate Rupture (SEGR) Simulations in Vertical Planar Power MOSFETs

Introduction

Power MOSFETs exposed to particle-rich, space-like or terrestrial, environment, can exhibit Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB). The use of power devices as high power solid state switches for the electric and hybrid car manufacturers, has generated new non-military, and non-space interest power device failure modes. A SEGR event is one such failure mode and the simulation of such an event is the subject of this article.

An irradiation event by a high-energy particle interacting with the material of a device gradually loses energy as it passes through the device, transferring its energy to the material by ionizing events. The net result is a high-density ionized track.

If the area of the device, through which the ionizing particle passes, has no internal electric field, then to a large extent, the high density of positive (hole) and negative (electron) charges created by the track, simply recombine, with the absence of an electric field to separate these charges by any meaningful distance.

Given there is an electrical field in the device prior to the strike, the high density of electron and hole pairs created by the primary particle can become separated. Once the positive and negative charges, escaping recombination, have become separated, the electrical field in the device is disturbed to a degree dependent on the Linear Energy Transfer (LET in MeV·cm²/mg) of the ionizing particle and the bias conditions of the device.

In a Single Event Gate Rupture (SEGR) event, there are three generally accepted response mechanisms, the gate (often referred to as capacitor or dielectric), the epitaxial, and the substrate. The initial measure drain and gate leakage currents depend upon device characteristics and oxide quality. Such that any measurable gate current increase above leakage during irradiation may indicate a SEGR event has occurred.

The gate SEGR response is measured by biasing the drain at zero volts (0V), and stepping the gate voltage in increments until SEGR occurs for the selected ion species. The SEGR gate voltage is defined as the average voltage at which the power device exhibited SEGR and the voltage of the previous irradiation, an irradiation data point where the power device exhibited no failures with failure being defined as gate current exceeding 1μA.

The gate component of SEGR can also be described as lowering of the intrinsic dielectric breakdown voltage to a new value called \( V_{\text{CRIT}} \). This \( V_{\text{CRIT}} \) value for silicon dioxide (SiO₂) dielectric is defined by the Titus-Wheatley equation (1) below:

\[
V_{\text{CRIT}} = \left[ \left( E_{\text{BD}} \right) \left( T_{\text{ox}} \right) \right] / \left( 1 + (Z/44) \right)
\]

The value \( V_{\text{CRIT}} \) is in volts, \( E_{\text{BD}} \) is the intrinsic dielectric breakdown field in volts per centimeter, \( T_{\text{ox}} \) is the dielectric thickness in centimeters, and \( Z \) is the ion atomic number. The Titus-Wheatley equation is limited to ions strikes that are perpendicular to the dielectric material, as these experimental evidence supports that the lowest values of \( V_{\text{CRIT}} \) occur for perpendicular ion strikes.²,³

The second response mechanism, the epitaxial response, is a distortion of the depletion field around the localized track area, which couples a portion of the drain voltage to the interface of the epitaxial layer and dielectric. This coupled voltage, \( V_{\text{COUPLED}} \), induces an electric field across the dielectric and is additive to the existing electric field due to the gate voltage, \( V_{\text{GS}} \). The epitaxial layer provides a standoff for a high electric field within the device. In vertical power structures, the blocking voltage capability is determined by the thickness and doping of the epitaxial layer. As thickness increases and is more lightly doped, the epitaxial blocking voltage increases, but a cost of increased on-state resistance. This makes the epitaxial response very sensitive to process and design parameters of the Power MOSFET.

The third response, the substrate response has been experimentally shown to have minimal effects, even with different substrate resistivity and thicknesses since there is no depletion layer inside the substrate.

Modeling and Simulation of Single Event Gate Rupture event in Technology Computer Aided Design (TCAD) tools, is supported by the ability to monitor gate, drain and source currents is to monitor the gate oxide field during the irradiation event.

Simulations

The simulation methodology in this example was to reduce what would normally be a three dimensional problem into a faster two dimensional problem by using circular symmetry in the device simulations, and also to define the irradiation strike to occur vertically at the center of the circular symmetry, so as not to incur any errors in the effective charge track shape.
Important Note: A vertical SEU strike at the center of a circular symmetric device is the only problem, which can be correctly reduced to two dimensions, and simulated as a 2D-Cylindrical. If the ion strike was at an angle, or the location of the strike was anywhere except the center of circular symmetry, Silvaco's full three-dimensional process, device and SEU simulation tools would be required.

A process flow of a typical power MOSFET was created in Victory Process incorporating the diffusion and implant models. The resulting structure is shown in Figure 1.

For the device simulation, an ion strike with an LET of 37.2 (corresponding to a Bromine Ion), is simulated, with the strike occurring at the center of the device (X=0). The syntax for creating the irradiation strike is invoked using the “SINGLEEVENTUPSET” statement, where the basic parameters of the primary ion are defined, such as entry and exit points and LET. For this example, the statement is given below:

```
  singleeventupset entrypoint="0,0,0" \ 
  exitpoint="0,8.5,0" radialgauss \ 
  b.density=$density pcunits \ 
  radius=0.07 t0=1e-14 tc=1e-15
```

The entry and exit points are defined as X,Y,Z points (Z=0 for a 2D device). The ion track charge density parameter, "b.density" is defined as a variable = (LET*0.011) when the charge has units of pico coulombs, specified by the parameter “pcunits”. The radius of the track and the Gaussian roll-off of charge density are defined by the parameters “radius” and “radialgauss” respectively. The primary ion strike time and duration are defined by:

```
  "t0" and "tc" parameters respectively.
```

Normally one needs to specify a fairly fine mesh along the ion track. This is necessary to account for the generated electron-hole pairs. To avoid this fine meshing, Victory Device supports numerical integration over the specified particle tracks and adds the result to the closest grid points found along the track. This not only eliminates the need for fine mesh generation along the particle track, but also allows for a more time efficient simulation. Enabling the numerical integration of the ion track, one needs to specify SEU.INTEGRATE on the method statement.

```
  method seu.integrate
```

Bias conditions during Single Event Gate Rupture (SEGR) simulation of heavy ion exposure should monitor for leakage currents through the gate, source, and drain terminals at a constant gate-to-source voltage (VGS) and a constant drain-to-source voltage (VDS). The bias conditions during simulated irradiation of the power device should hold VGS constant, with VDS incremented at each exposure until failure. At the time of the irradiation strike, a bias of -13.9 volts is applied to the gate and 30 volts on the drain. This bias condition creates a near critical condition close to that required for a gate rupture event to occur. Gate current is monitored using the self-consistent Fowler-Nordheim model.

```
  models fn.cur
```

The gate oxide field is probed near the strike, such that gate oxide field versus time could be plotted before, during and after the ion strike. The “probe” statement allows specific physical quantities in the structure file that are located at specified co-ordinates in the device, to be exported to a log file, such that these quantities can be continuously calculated during transient or DC simulations. The probe statement in this example is given by:

```
  probe name=Strike_Field field dir=270 x=0.02 y=-0.02
```

The “name” parameter in the probe statement is what will appear in the plotting tool, TonyPlot, as the name of the quantity being plotted. The “field” parameter tells the
The evolution of the hole concentration distribution was also monitored at the strike event and at 5, 50 and 150 pico-seconds after the strike. The effect of the electric fields present before the strike has on charge separation and subsequent transportation can be seen clearly in the time evolution snap-shots shown in Figure 3.

The effect of the ion strike on the drain and gate current was also monitored over a longer time span and is shown in Figure 4A and 4B. Just for completeness the breakdown voltage and unsaturated threshold voltage (for Vd=0.1 volts) were also simulated and are shown in Figures 5 and 6 respectively.

Conclusion

In conclusion, due to the nature of the near instantaneous breakdown characteristics of dielectric, the simulation of Single Event Gate Rupture (SEGR) events requires the monitoring the peak electric field and gate current in the gate oxide during and immediately after the ion strike.

If the peak electric field across the gate exceeds the “intrinsic” value of approximately 1E7 V/cm for thermal silicon dioxide, then it can be assumed that irreversible damage has occurred.

References


Figure 5. DC breakdown curve of the power MOSFET

Figure 6. Unsaturated Vt curve for Vd=0.1 volts