State of the Art 2D and 3D Process and Device Simulation of GaN-Based Devices

Introduction

Silicon has long been the semiconductor of choice for high-voltage power electronics applications. However, wide-bandgap semiconductors such as SiC and GaN have begun to attract attention because they are projected to have much better performance than silicon. In comparison with silicon, wide-bandgap semiconductors offer a lower intrinsic carrier concentration, a higher electric breakdown field, a higher thermal conductivity, and a faster saturated electron drift velocity.

Simulating GaN devices is more challenging compared to Silicon. Indeed very low intrinsic concentration combined with high doping values is usually detrimental to convergence. Since GaN is as wide a band gap material as SiC, we thus use the same simulation approach used for SiC and describe in details in http://www.silvaco.com/tech_lib_TCAD/simulationstandard/2013/jan_feb_mar/a1/state_of_the_art_3D_SiC_Process_and_device_simulation_a1.html

In the following paragraphs we will first review the physics involved and needed for accurate simulation of GaN based devices. We will then illustrate our simulation flow with few examples.

Physical Model Requirements

It is well known that AlGaN/GaN based HFETs exhibit two-dimensional electron gases (2DEG) contributing to outstanding performance without having to add doping to the structure. This 2DEG results from the also well-known combination of spontaneous (zero strain) and piezoelectric (strained) polarization. The computation of the 2DEG due to the polarization effect is performed automatically during the simulation thanks to our built-in model. From a practical point of view it means that the user do not have to specify any charges at a specific interface location between materials when changing the thicknesses or the composition fraction.

Validation of the model has been carried out in Atlas and Victory Device based on [1,2] and simulation results for an AlGaN/GaN structure as shown in Figure 1 and 2.

Mobility and impact ionization models are also GaN-specific. You can use a composition and temperature dependent low field model by specifying the FMCT.N and FMCT.P in the MOBILITY statement. FMCT stands for Farahmand Modified Caughey Thomas. This model was the result

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Figure 1. comparison of the built-in piezoelectric model between Atlas and Victory Device.
of fitting a Caughey Thomas like model to Monte Carlo data [3]. You can also choose to model low field mobility as a function of doping and temperature following the work of Albrecht et al. [4] by specifying ALBRCT on the MODEL statement or ALBRCT.N or ALBRCT.P or both on the MOBILITY statement for separate control over electrons and holes. You can finally select the nitride-specific high field dependent mobility model by specifying GANSAT.N and GANSAT.P on the MOBILITY statement. This model [3] is based on a fit to Monte Carlo data for bulk nitride and exhibits negative differential mobility as shown in Figure 3.

As far as Impact Ionization is concerned, using the tabular Selberherr model, we provide build-in tabular representations of results from several recent publications. We provide convenient access using different key words on the IMPACT statement. Figure 4 shows a comparison of the various tabular ionization rate models against the default models.

Performance of GaN devices can be altered by the presence of defects (traps and intraps) and also by self heating. It is thus important to take these effects into account during simulation. Our simulators allow 2D and 3D simulation of self heating effects. Models include heat generation, heat flow, lattice heating, heat sinks, and effects of local temperature on physical constants. Thermal and electrical physical effects are coupled through self-consistent calculations. IV characteristics are not always reproducible as a result of deep traps in the nitride material. A deep trap may be regarded as an impurity or crystal defect that captures a mobile charge carrier and keeps it strongly localized in the neighborhood of the trapping center. Deep traps can produce current collapse, a distortion of the device current-voltage (I-V) characteristic that is of particular concern because it ultimately limits the output power of the device. Discrete and continuous Traps and Interface traps are available in Atlas and Victory so that these effects can be taken into account.

The main concept of GaN-based power devices is to use epitaxial strain to create 2DEG. As mentioned above we provide a built-in model for that. On top of that, this built-in model also supports dependency on a loaded strain tensor resulting for example from a deposited stress-liner made of nitride on top of the AlGaN/GaN layers. The “intrinsic” stress resulting from this nitride layer is computed using Victory Stress and can be directly loaded in Atlas or Victory Device.

Applications

In this section we will review and show 2D and 3D simulations of different type of structures. We will compare simulation results with experiments and show different type of simulations including DC, Transient, AC and large signal.
This example demonstrates the simulation of a GaN metal-insulator-semiconductor field effect transistor (MIS-FET) with Piezo Neutralization Technique (PNT) [5].

The first feature of the PNT structure is an AlGaN buffer layer to realize a normally-off operation. The polarization charges at the interface between the AlGaN buffer and the GaN channel act as virtual p-type doping and contribute to simultaneously increase Vt and charge density in the channel. The band diagram and IdVg shown in Figure 5 and in Figure 6 respectively demonstrate the impact of the buffer Al-concentration on the electron-channel energy beneath the gate and Vth respectively.

The second feature is an Al0.07Ga0.93N PNT layer having an identical Al composition with the buffer layer to realize high Vth uniformity. Since PNT and buffer layers have an identical Al mole fraction, the polarization charges formed between these layers are completely canceled, and hence a flat band condition occurs throughout the PNT layer.

The last feature is the second supply layer at the region outside the gate electrode to reduce on-resistance of the GaN FET. Since the second supply layer is consisted of AlGaN with higher Al composition than that for the first supply layer, a large amount of 2DEG is produced both in the channel layer and the PNT layer as shown in Figure 8.

Vth dependence on the AlGaN layer thickness under the gate electrode was simulated. For the GaN FETs with the PNT structure, the Vth is not affected by the variation of AlGaN thickness whereas it varies for the conventional Al0.15Ga0.85N/GaN single heterojunction FETs as as shown in Figure 7.

The last feature is the second supply layer at the region outside the gate electrode to reduce on-resistance of the GaN FET. Since the second supply layer is consisted of AlGaN with higher Al composition than that for the first supply layer, a large amount of 2DEG is produced both in the channel layer and the PNT layer as shown in Figure 8.

A Normally-off GaN HFET with p-type GaN gate

This example demonstrates simulation of a GaN HFET with p-type GaN gate [6] shown in Figure 9.

While a Schottky-type metal on the AlGaN barrier acts as a gate for normally-on HEMTs, a p-type doped semiconductor gate is able to deplete the transistor channel.
when unbiased, thus yielding a normally-off device. The simulation of the transfer characteristic reveals a $V_t$ of around 1.25V. The sub-threshold leakage current drops significantly immediately below the threshold voltage, however the drop slows down to around 4uA/mm at $V_{GS}$=0V. The leakage current is determined by traps. The gate current in the on-state (defined as $V_{GS}$=5V) is around 3uA/mm and thus around five orders of magnitude below the drain current as shown in Figure 10.

The output characteristic shows a negative differential resistance due to lattice heating and simulated by solving the lattice heating equation. The maximum drain current is approximately 0.4A/mm as seen in Figure 11.

The Breakdown Voltage of this device is 870V as seen in Figure 12, and the leakage current is controlled by the traps.

Enhancement-Mode N-Polar GaN MISFETs

This example demonstrates simulation of an Enhancement-Mode N-Polar GaN MISFET [7]. The structure is shown in Figure 13. There is a growing interest in high performance enhancement mode GaN channel devices because of single voltage operation and simpler circuit topologies. The advantages of enhancement mode GaN FETs fabricated on N-polar GaN include reduced source/drain access resistance and wide bandgap barrier layers used for a polarization-induced field allowing 2DEG depletion under the channel. Removal of the AlN layer from the access region recovers the 2DEG induced by the bottom AlN layer. Plots of the bang diagram under the gate and under the nitride sidewall reveal 2DEG under the access region but not under the gate as seen in Figure 14.
The simulation of the transfer characteristic reveals a $V_t$ of around 1V and a maximum $I_{ds}$ of around 0.7A/mm at $V_{gs}=5V$ as seen in Figure 15.

Electron injection from the channel to the gate is limited by the AlGaN/GaN heterojunction. As a consequence no current offset is observed at zero drain since gate current is very low. This device exhibits a threshold voltage around 1V, a maximum drain current at $V_d=10V$ and $V_g=5V$ of 200mA/mm and a breakdown voltage of 640V as shown in Figure 17, Figure 18 and Figure 19 respectively.

**Normally-off AlGaN/GaN Transistor with Conductivity Modulation**

This example demonstrates simulation of a normally-off AlGaN/GaN transistor with conductivity modulation resulting from hole injection from a p-AlGaN gate to the AlGaN/GaN heterojunction [8]. The p-AlGaN gate allows normally-off operation.

When the gate voltage increases and reaches the built-in pn junction voltage at the gate (around 3.5V) holes inject into the channel and generate the equal number of electrons increasing the 2DEG. Electrons with high mobility will reach the drain under the effect of the electric field whereas the holes will stay since their mobility is much lower than the electron. The current is thus modulated by the number of holes injected. It is also interesting to notice that this device exhibits a double peak in the transconductance curve, a second proof of hole injection as shown in Figure 16.

**Figure 13.** Enhancement-Mode N-Polar GaN MISFETs.

**Figure 14.** Bang diagram under the gate, under the nitride sidewall and under the drain regions.

The simulation of the transfer characteristic reveals a $V_t$ of around 1V and a maximum $I_{ds}$ of around 0.7A/mm at $V_{gs}=5V$ as seen in Figure 15.

**Figure 15.** Drain current versus gate voltage.

**Figure 16.** Transconductance versus gate voltage.

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Fe Bulk Doping Related Current Collapse Phenomenon

This example demonstrates simulation of the “Current Collapse” and “Current Recovery” phenomenon resulting from population and de-population of Intentional Iron (Fe) Doping Traps under the gate of a GaN FET as a result of Gate to Drain Electric Fields.

Many publications suggest that unintentional surface traps are the main cause of the GaN current collapse phenomenon. In this example, we show that sometimes this is not actually the case. Current collapse in this device is mostly caused by intentional iron doping, whose main purpose is to create a semi-insulating buried layer to reduce the buried layer source-to-drain leakage path.

The device structure in this example is based on [9].

Substrate leakage current is controlled by a graduated concentration of deep level iron acceptor traps located 1eV below the conduction band edge.

The device is first biased with 0v on the gate and 5v on the drain. After a mili-second at this bias, the device is field stressed for only one further milli-second at 25v on the drain and -4v on the gate as seen in Figure 20. After this short bias stress, the device was returned to its original bias of 0v on the gate and 5 volts on the drain. After only one milli-second of bias stress, the drain current is significantly reduced demonstrating the current collapse phenomenon as seen in Figure 21.
A comparison structure file plot of the pre and post-stress ionized Fe trap density shows that the cause of the current collapse is actually the change in charge state of the Fe doping deep in the substrate under the gate, and also on the drain side between the gate and drain contacts as seen in Figure 22.

For completeness, the unstressed bias remained on the device until the traps became de-populated with electrons and the drain current returned to its original value. Interestingly, it takes over one week for the device to recover. (6e5 seconds) as seen in Figure 23. This very long recovery time may be incorrectly interpreted as device degradation from field-induced traps which is an irreversible effect resulting from electric field-induced reverse piezo-electric stress.

**2-6 3D AlGaN/GaN HEMT Including Intrinsic Stress Effect**

The device under consideration is a 3D AlGaN/GaN HEMT shown in Figure 24. 3D stress distribution is simulated by Victory Stress. This example produces stress distributions via the stress-liner made of nitride as shown in Figure 24 and Figure 25. Note that the stressor in this example is used to illustrate strain polarization on top of piezo and spontaneous polarization.
After the initial solution is obtained, the drain voltage is ramped to 1 V, then the IdVg characteristic is extracted from Vg=-8 to Vg=1.0 V as seen in Figure 26. The effect of strain is seen on IdVg. Overlay of 2D simulation results with 3D simulation results obtained with width=1 validates our 3D implementation.

Influence of the Gate to Drain distance on the breakdown voltage

This example demonstrates the influence of the gate-to-drain distance on the breakdown voltage with and without silicon substrate [10].

The structure consists of 20nm AlGaN with xcomp=0.2 and 1um GaN buffer layer as shown in Figure 27. Donor and acceptor traps are included in the simulation. Gaussian profile acceptor traps are used with a peak concentration close to the bottom of the buffer layer to mimic the fact that the material quality improves toward the surface of the device.

Donor Interface traps at the AlGaN/Nitride interface and acceptor interface traps at the GaN/Silicon interface are also included during the simulation.

Forward characteristic simulation reveals a threshold voltage of around -2V. Slow transient simulation is used to simulate the breakdown voltage curve.

The deck is parametrized so that we can vary the distance between the gate and drain (LGD). DeckBuild DoE capability is used to automate simulations of BV versus LGD with and without substrate.

We can observe in Figure 28 an almost linear increase of BV versus LGD when silicon substrate is not present. An increase of the gate current is observed in Figure 29 near breakdown, and the value is of the same order as the drain current. This result indicates that BV is defined by an avalanche phenomenon between the gate and the drain as shown in Figure 30.

BV does not depend significantly on LGD when a silicon substrate is present due to charge accumulation at the GaN/Silicon interface, related to the presence of interface traps, which screen the electric field.
GaN HEMT Thermal Optimization using Flip Chip Structure

This example demonstrates two-dimensional electro-thermal simulations with heat sink structures.

Although the superiority of GaN HFET device characteristics has been demonstrated, the self heating effect has hindered the production of high power and high speed GaN-based switching devices. This effect can be significantly reduced by the cost effective heat-sink approach. In this example, in order to understand and control the self heating effect, a GaN HFET with a flip chip concept is simulated, and device characteristics are compared versus a normal structure.

For HFETs, the GaN/AIGaN epitaxial layers have been grown on either sapphire or SiC substrates. Although sapphire has the advantage of lower cost and availability in larger wafer sizes, its poor thermal conductivity (0.3 W/cm-K) limits the achievable powers due to severe self-heating. The self-heating effect can be significantly reduced by flip-chip mounting the devices onto highly conducting substrates such as AIN (1.8 W/cm-K).

The typical GaN HFET flip chip structure in this example is a Al0.25Ga0.75 N-GaN HFET on a sapphire substrate. The structure consists of an AIN layer as a heat sink, a 2.7nm undoped AIGaN layer, and two GaN layers which includes 20nm doped 1e15 GaN and 1um undoped GaN as shown in Figure 31.

The self-heating is a local increase of crystal temperature due to dissipated Joule electric power, this effect can significantly reduce the electron mobility and degrade device performance.

DC, Transient and AC simulations are performed and compared with and without the flip chip structure as shown in Figure 32, Figure 33 and Figure 34 respectively. As expected the performance of the device is better using the flip chip architecture.
Large Signal Output Power Analysis

This example describes how to simulate typical 10 GHz large-signal measured performance quantities related to power output, such as power out versus power as shown in Figure 35, power gain as shown in Figure 36 and amplifier efficiency as shown in Figure 37 as the device is over-driven into high distortion. The example also plots in Figure 38 the output signal shape versus time for each

Figure 35. Power out versus power in.

Figure 36. Power gain versus power out.

Figure 37. Power Output Efficiency versus Power out.

The structure under test is shown in Figure 39.

Ten large signal input amplitudes are defined. Each of these waveforms are applied to the gate in order of increasing amplitude. After each waveform simulation is complete, a number of large signal parameters are calculated. The peak input and output voltages are extracted, followed by the exact times at which these peak voltages occurred. Then the input and output currents are extracted at the same times as the peak voltages occur. It is important to extract the currents at the same time as the peak voltages in order to take account of the phase between current and voltage, so that the correct power values can be calculated.
Conclusion

GaN is a very promising material for high power switching applications. However, development cost is becoming a serious concern for GaN manufacturers. This is why TCAD is so important in order to reduce cost and help optimize device performance.

Silvaco’s Process and Device solutions have all the capabilities (i.e. state of the art mesh, discretization, solvers and physical models) that we think are essential to accurately simulate GaN based devices in 2D and 3D.

References


Introduction

Interdigitated back contact silicon heterojunction (IBC-SHJ) combines the advantages of interdigitated back contact (IBC) and silicon heterojunction (SHJ) solar cells. Having all the contacts at the back of the cell eliminates contact shading, leading to a higher short-circuit current (JSC). Being a heterojunction device, IBC-SHJ also has the potential of higher open circuit voltage (VOC) due to the better surface passivation of the deposited amorphous silicon (a-Si) layer. The low temperature deposition, instead of high temperature diffusion, decreases thermal stress, which is the trend of future silicon solar cells. Rear surface passivation by deposited intrinsic amorphous silicon (a-Si) buffer layer in IBC-SHJ solar cells significantly improves open circuit voltage (VOC) and short circuit current (JSC) but can lead to very low fill factor (FF) with an “S” shape J-V curve. In this paper, methods to optimize IBC-SHJ solar cell with improved FF are discussed and guided by two-dimensional numerical simulation. The modeling of the IBC-SHJ solar cell requires device simulation software operating in two dimensions and incorporating amorphous silicon. To study this innovative structure, we use ATLAS two-dimensional (2-D) device simulation software that provides accurate bulk and interface defects needed to model amorphous silicon. We first present the geometrical structure of the solar cell, then review the general framework of the simulation by specifying the different physical models, and finally examine the simulation results in order to determine the important parameters to achieve high efficiency.

Device Structure

Back contact cells differ from conventional structures in that all contacts are on the back side (not illuminated side) of the cell. The front surface is subject to illumination. On the rear side, we have an interdigitated structure of hydrogenated amorphous silicon layers alternately n-type and p-type to play the role of emitter or back surface field (BSF) according to the c-Si substrate doping. We used an n-type c-Si substrate in this Device. The emitter (p-stripe) and the BSF (n-stripe) are covered by metal contacts. An intrinsic a-Si buffer layer was deposited over the entire rear surface of the IBC-SHJ solar cell. The IBC-SHJ solar cell presents a periodic structure. The periodicity of the structure allows us to use an elementary structure, shown in Figure 1, that will serve as a basis for optimizing the performance of this type of cell. The geometrical and material parameters of the simulated structure were chosen according to [1].

Physical Models

The simulation is based on the solution of three governing semiconductor equations: Poisson’s equation, electron and hole continuity equations. Fermi statistic was used for carriers with drift-diffusion combined with Bohm Quantum Potential for quantum correction. Fermi model and Recombination models (i.e srh, auger and surface recombination) were also included into the simulation. For a-Si layers, critical parameters like band gap, doping and defect distribution are defined in the input deck. The critical parameters for accurate simulation are energy distribution of the exponential band tails, and the Gaussian distribution of the mid-gap trap states. They were chosen according to reference [1] and shown in Figure 2. For c-Si/a-Si interfaces at the back surface a thermionic emission model was used. For even more realistic modeling of this interface we have introduced defect states at the hetero-interface by putting a very thin defective layer of c-Si [2]. An AM1.5G solar spectrum is used for the optical generation to simulate the J-V curve under standard one-sun illumination conditions. A Sopra database is used for a-Si index of refraction.

To properly simulate the behavior of the structure, it is essential to apply an adapted mesh. A mesh as thin as possible applied to the whole structure ensures good accuracy of calculations but requires greater computational time to simulate the behavior of this structure. It is therefore necessary to find a compromise between computational time and accuracy of the calculation. To reach this compromise, we applied a fine mesh only in areas where changes in physical quantities are important and a coarse mesh in areas where these quantities are quasi
static. Thus, the mesh is refined in the critical areas that are the front surface (strong absorption), the c-Si/a-Si:H hetero-interfaces and the areas around frontiers of the various layers in which the variations of physical quantities are important. In the middle of the c-Si substrate, a coarse mesh is used as the physical quantities do not vary significantly. Figure 3 represents the mesh used to simulate IBC-SHJ solar cell.

Simulation Results
A complete parametrized input deck, including geometry and mesh, was created not only to optimize simulation time and accuracy but also for solar cell optimization purposes. This input deck was used in DBinternal to vary different parameters in order to optimize the solar cell efficiency. DBINTERNAL is a simple but powerful DECKBUILD tool that allows you to create a Design Of Experiments (DOE) from a pair of input files. Amongst other things, you can create corner models for process parameters or device characteristics or both. Any parameters that are to be used as variables must be specified as set statements in a template file. Any results of interest should be calculated using extract statements. The DOE is specified with simple sweep statements in a separate design file. The sweep statement defines which variables are required in the DOE, and the range of values these variables are to take. The parameter values and the results of each simulation can be stored in a file that can be viewed in TonyPlot or used as a database for input to a statistical analysis tool such as SPAYN. We have chosen 4 parameters to optimize efficiency. These parameters are intrinsic a-Si thickness, n-stripe and p-strip width and gap width.

It was experimentally observed that an intrinsic a-Si layer increases Voc and Jsc but also decreases FF and leads to a "S" shape IV curve. Simulation results, shown in Figure 4, confirm the reduction of FF and "S" shape IV curve.
Figure 5. IBC-SHJ solar cell Key figure of merits as a function of a-Si thickness.

Figure 6. IBC-SHJ solar cell Key figure of merits as a function of n-stripe width.

Figure 7. IBC-SHJ solar cell Key figure of merits as a function of gap width.

Figure 8. IBC-SHJ solar cell Key figure of merits as a function of p-stripe width.

The results of the DoE are shown in Figures 5, 6, 7 and 8. Figure 5 shows an increase of Voc when the thickness of the intrinsic a-Si layer increases as reported in [3], leading to an optimum efficiency of around 10nm for the intrinsic a-Si layer. n-stripe, p-stripe and gap width were also optimized.

Figures 6 and 7 show that Jsc decreases when n-stripe width and gap width increases. As a consequence n-stripe and gap width have to be chosen as narrow as possible.

It is interesting to notice that Jsc increases and FF decreases when p-stripe increases as shown in Figure 8. The different evolution of Jsc and FF leads to an optimum for the efficiency of around 1mm for p-stripe width.

Conclusion

2D numerical simulations were performed in order to study and optimize IBC-SHJ solar cells. The impact of several geometrical parameters were studied and their impact was shown on the IBC-SHJ solar cell output characteristics. This gives the designer guidelines to achieve high efficiency IBD-SHJ solar cells.

References


Anode Shorts Layout Dependence of Bi-mode IGBT (BiGT)
On-state Characteristics

Reverse Conducting IGBT (RC-IGBT)
A new class of high-voltage semiconductor devices, known as a reverse conducting IGBT (RC-IGBT), has emerged in recent years from research efforts to diminish the usage of external anti-parallel free-wheeling diode chips for IGBT switching applications. The RC-IGBT device concept is based on the monolithic integration of a freewheeling diode into an IGBT chip. Hereby, an anti-parallel diode is formed through the embedment of an n+ region in an anode/collector region of the IGBT. Both the n+ region and the p+ anode are then shorted together by an anode/collector contact. Although the RC-IGBT has many advantages over the conventional IGBT, especially in terms of manufacturing cost, total chip size and reliability of power modules, it is detrimental to the snapback effect at forward conduction of IGBT mode.

Snapback Effect in RC-IGBT
In the on-state IGBT mode of an RC-IGBT, when electrons flow from a cathode/emitter contact through an n-buffer region (or an n-drift region in case of a non-punch-through IGBT) to an n+ region at the anode/collector contact, they forward bias the p+-anode /n-buffer junction. On grounds of reflection symmetry, the voltage drop across the junction has its maximum value in the middle of the p+ anode region. Only after a sufficiently high voltage drop has built up in response to an increase in the collector current does the p+ anode start injecting holes into the n- drain drift region, with the result that the drift region becomes less resistive by conductivity modulation. An increase in hole levels in the drift region above the doping concentration eventually gives rise to a voltage snapback.

Bi-mode Insulated Gate Transistor (BiGT)
The Bi-mode insulated gate transistor (BiGT) represents a further development of the RC-IGBT device concept, with the primary objective of alleviating the snapback effect in RC-IGBT. Recent research results have indicated that the snapback voltage in the RC-IGBT on-state characteristics decreases with the increase of the width of the p+ anode [1]. Accordingly, the BiGT device is built around the concept of incorporating an IGBT with a wide p+ anode, also referred to as pilot-IGBT, into the RC-IGBT structure as outlined in Figure 1.

Design Analysis and 3D Simulation with Victory Process and Device
Studies in [3] have shown that, in the on-state of the BiGT, the anode shorts layout design of the RC-IGBT portion affects the conductivity modulation of the entire BiGT, and therefore its on-state behavior. They attribute the cause of this layout-dependent device performance to the lateral spread of the electron-hole plasma from the pilot-IGBT into the RC-IGBT and suggest a possibility of snapback suppression by a radial layout design of anode shorts.

In order to verify the validity of the arguments and reproduce the results reported in [3], 3D device simulations with Victory Device have been performed in combination with process simulation with Victory Process. Figure 2 illustrates the simulation structure of the BiGT as well as the anode shorts layout designs under consideration.

It follows that there are two basic patterns for anode shorts layouts – stripes (designs S1, S2 and S3), with each having the same width of 100 µm but different orientations relative to the pilot-IGBT boundary, and square dots (designs D1 and D2), with each having squares whose all four sides equal to 100 µm and 224 µm respectively.

In the simulation domain with an area of 0.5 mm × 4 mm, the BiGT assumes a 100 µm-thick drain drift region, together with a 10 µm-thick SPT n+ buffer layer on a 2.5 µm-thick anode/collector region. For simplicity, the MOS cells on the emitter side are modeled with a 1 µm-thick heavily doped n-type layer of silicon, given the conducting state of the BiGT in the IGBT mode.
Simulation Results

Based on a transient simulation technique, in which the collector current is ramped from 0 A to 24 A at a constant rate over a period of time, Victory Device captures a number of small secondary snapbacks in simulated I-V characteristics in IGBT mode of design S1 and a large snapback in design S3 (Figure 3). On the other hand, there is no sign of a voltage snapback in designs S2, D1, and D2 (Figure 5).

During the current ramp-up Victory Device also outputs carrier density data for visual inspection of the detail of carrier expansion with TonyPlot in a cut plane defined along the z-axis at z = -40 µm (Figure 2a). Within the simulation domain comprising an area of 3 mm × 4 mm, the plan view of carrier density distribution in the device with different anode shorts design variants is displayed at specific values of collector current in Figure 4 and Figure 6.
**Analysis of Results**

In the case of design S1, injection from each 100 µm-wide anode segment occurs by progressive stages as the electron current flows perpendicularly through the p+ anode segments. This means that injection from each anode segment corresponds to each secondary snapback in the device with design S1.

By contrast, the radial configuration of anode segments in the S2 design enables the electrons from the pilot-IGBT to flow and forward bias the p+ anode/n-buffer junction along the entire stripe length. As a result, the portion of anode segments adjacent to the pilot-IGBT starts injecting carriers that later on spread smoothly and without causing a voltage snapback all over the entire device volume at a relatively low current, compared to the S1 design.

With regard to design S3, the orthogonally arranged anode segments are disconnected to the pilot-IGBT, so hole injection from the anode stripes triggers a voltage snapback at a higher current than design S1. Nevertheless, after the onset of snapback the anode stripes of design S3 rapidly supply the entire device volume with plasma, which thus renders the I-V curve behavior of design S3 at high current levels identical with that of design S2.

As far as the square dots pattern is concerned, the transition of the devices with the D1 and D2 designs into full conduction goes as smoothly as the case of radial layout design S2, except that the available anode segment area essentially determines the device IGBT mode on-state I-V characteristics. Figure 5 reveals that the radial stripe design S2 exhibits a slightly higher on-state voltage drop than the D1 design but incurs almost exactly the same conduction losses as design D2. This agrees well with the fact that the S2 design provides the entire device area with almost exactly the same plasma as design D2, as it can be seen in Figure 6.

**Conclusions**

Victory Process and Device proves to be capable of reproducing consistent simulation data with reference to [3]. It allows users to speed up the product design process and shorten the development timeline considerably.

**References**


Q: How can I compare the results of 2D and 3D breakdown simulations with Hatakeyama’s impact ionization model for 4H-SiC based power devices?

A: In a 4H-SiC crystal, the stacking sequence of a Si-C bilayer plane extends along the crystallographic c-axis direction, also referred to as the <0001> direction (see Figure 1). With regard to crystallographic orientation, avalanche breakdown process in 4H-SiC uniquely features anisotropy of avalanche breakdown field, i.e., impact ionization coefficients.

Victory Device has an option of an anisotropic impact ionization model based on the work of Hatakeyama, et al. [2]. In Hatakeyama’s impact ionization model, the ionization coefficients are strong functions of the strength and orientation of the electric field relative to the optical c-axis of the crystal. The orientation in 3D space of the optical axis can be defined with the ZETA and THETA parameters on a MATERIAL statement, as depicted in Figure 2.

Hereby, the ZETA parameter specifies the angle that the optical axis makes with the positive y-axis. The horizontal angular distance, measured clockwise around the y-axis, from the positive x-axis to the orthogonal projection of the optical axis on the x-z plane, is determined by the parameter THETA. By default the ZETA and THETA parameters are both set to zero, i.e., ZETA = THETA = 0 degrees, which implies the alignment of the <0001> direction of 4H-SiC with the y-axis.

In 2D device simulations, with the y-axes of the 2D structure being conventionally taken along the depth into the wafer, the default settings for the ZETA and THETA parameters ensure that the c-axis of the 4H-SiC crystal is normal to the wafer surface. This is in agreement with the fact that commercial 4H-SiC substrates are typically cut perpendicular to the c-axis. In the case of 3D simulations, however, the z-axis conventionally indicates the depth direction of the wafer from the surface. Hence, in order for 3D breakdown simulation results to be directly comparable with 2D ones, the <0001> crystal axis must be oriented such that it coincides with the z-axis. This can be achieved by setting ZETA = 90 degrees and THETA = 90 degrees, respectively.

Taken as an example, sicex11.in [3] compares the 2D and 3D breakdown simulation results computed with Hatakeyama’s model. The device under simulation illustrated in Figure 3 is a 4H-SiC power MOSFET with a trench gate structure, created by Victory Cell and simulated at a high precision level with Victory Device. The simulation setup is such that the optical axis corresponds to the height of both the 2D and 3D device structure. It is obvious from Figure 4 that the simulated 2D and 3D breakdown characteristics have turned out to be in excellent agreement with each other.
Figure 3. 2D (left) and 3D (right) 4H-SiC trench-gate power MOSFET.

Figure 4. Comparison of 2D and 3D breakdown characteristics of the 4H-SiC trench-gate power MOSFET.

References


