State of the Art 2D and 3D Process and Device Simulation of GaN-Based Devices

Introduction

Silicon has long been the semiconductor of choice for high-voltage power electronics applications. However, wide-bandgap semiconductors such as SiC and GaN have begun to attract attention because they are projected to have much better performance than silicon. In comparison with silicon, wide-bandgap semiconductors offer a lower intrinsic carrier concentration, a higher electric breakdown field, a higher thermal conductivity, and a faster saturated electron drift velocity.

Simulating GaN devices is more challenging compared to Silicon. Indeed very low intrinsic concentration combined with high doping values is usually detrimental to convergence. Since GaN is as wide a band gap material as SiC, we thus use the same simulation approach used for SiC and describe in details in http://www.silvaco.com/tech_lib_TCAD/simulationstandard/2013/jan_feb_mar/a1/state_of_the_art_3D_SiC_Process_and_device_simulation_a1.html

In the following paragraphs we will first review the physics involved and needed for accurate simulation of GaN based devices. We will then illustrate our simulation flow with few examples.

Physical Model Requirements

It is well known that AlGaN/GaN based HFETs exhibit two-dimensional electron gases (2DEG) contributing to outstanding performance without having to add doping to the structure. This 2DEG results from the also well-known combination of spontaneous (zero strain) and piezoelectric (strained) polarization. The computation of the 2DEG due to the polarization effect is performed automatically during the simulation thanks to our built-in model. From a practical point of view it means that the user do not have to specify any charges at a specific interface location between materials when changing the thicknesses or the composition fraction.

Validation of the model has been carried out in Atlas and Victory Device based on [1,2] and simulation results for an AlGaN/GaN structure as shown in Figure 1 and 2.

Mobility and impact ionization models are also GaN-specific. You can use a composition and temperature dependent low field model by specifying the FMCT:N and FMCT:P in the MOBILITY statement. FMCT stands for Farahmand Modified Caughey Thomas. This model was the result...
of fitting a Caughey Thomas like model to Monte Carlo data [3]. You can also choose to model low field mobility as a function of doping and temperature following the work of Albrecht et.al [4] by specifying ALBRCT on the MODEL statement or ALBRCT.N or ALBRCT.P or both on the MOBILITY statement for separate control over electrons and holes. You can finally select the nitride-specific high field dependent mobility model by specifying GANSAT.N and GANSAT.P on the MOBILITY statement. This model [3] is based on a fit to Monte Carlo data for bulk nitride and exhibits negative differential mobility as shown in Figure 3.

As far as Impact Ionization is concerned, using the tabular Selberherr model, we provide build-in tabular representations of results from several recent publications. We provide convenient access using different key words on the IMPACT statement. Figure 4 shows a comparison of the various tabular ionization rate models against the default models.

Performance of GaN devices can be altered by the presence of defects (traps and intraps) and also by self-heating. It is thus important to take these effects into account during simulation. Our simulators allow 2D and 3D simulation of self-heating effects. Models include heat generation, heat flow, lattice heating, heat sinks, and effects of local temperature on physical constants. Thermal and electrical physical effects are coupled through self-consistent calculations. IV characteristics are not always reproducible as a result of deep traps in the nitride material. A deep trap may be regarded as an impurity or crystal defect that captures a mobile charge carrier and keeps it strongly localized in the neighborhood of the trapping center. Deep traps can produce current collapse, a distortion of the device current-voltage (I-V) characteristic that is of particular concern because it ultimately limits the output power of the device. Discrete and continuous Traps and Interface traps are available in Atlas and Victory so that these effects can be taken into account.

The main concept of GaN-based power devices is to use epitaxial strain to create 2DEG. As mentioned above we provide a built-in model for that. On top of that, this built-in model also supports dependency on a loaded strain tensor resulting for example from a deposited stress-liner made of nitride on top of the AlGaN/GaN layers. The “intrinsic” stress resulting from this nitride layer is computed using Victory Stress and can be directly loaded in Atlas or Victory Device.

Applications

In this section we will review and show 2D and 3D simulations of different type of structures. We will compare simulation results with experiments and show different type of simulations including DC,Transient, AC and large signal.
A Normally-off GaN MISFET with High Vth uniformity

This example demonstrates the simulation of a GaN metal-insulator-semiconductor field effect transistor (MISFET) with Piezo Neutralization Technique (PNT) [5].

The first feature of the PNT structure is an AlGaN buffer layer to realize a normally-off operation. The polarization charges at the interface between the AlGaN buffer and the GaN channel act as virtual p-type doping and contribute to simultaneously increase Vt and charge density in the channel. The band diagram and IdVg shown in Figure 5 and in Figure 6 respectively demonstrate the impact of the buffer Al-concentration on the electron-channel energy beneath the gate and Vth respectively.

The second feature is an Al0.07Ga0.93N PNT layer having an identical Al composition with the buffer layer to realize high Vth uniformity. Since PNT and buffer layers have an identical Al mole fraction, the polarization charges formed between these layers are completely canceled, and hence a flat band condition occurs throughout the PNT layer.

Vth dependence on the AlGaN layer thickness under the gate electrode was simulated. For the GaN FETs with the PNT structure, the Vth is not affected by the variation of AlGaN thickness whereas it varies for the conventional Al0.15Ga0.85N/GaN single heterojunction FETs as as shown in Figure 7.

The last feature is the second supply layer at the region outside the gate electrode to reduce on-resistance of the GaN FET. Since the second supply layer is consisted of AlGaN with higher Al composition than that for the first supply layer, a large amount of 2DEG is produced both in the channel layer and the PNT layer as shown in Figure 8.

A Normally-off GaN HFET with p-type GaN gate

This example demonstrates simulation of a GaN HFET with p-type GaN gate [6] shown in Figure 9.

While a Schottky-type metal on the AlGaN barrier acts as a gate for normally-on HEMTs, a p-type doped semiconductor gate is able to deplete the transistor channel
when unbiased, thus yielding a normally-off device. The simulation of the transfert characteristic reveals a Vt of around 1.25V. The sub-threshold leakage current drops significantly immediately below the threshold voltage, however the drop slows down to around 4μA/mm at VGS=0V. The leakage current is determined by traps. The gate current in the on-state (defined as VGS=5V) is around 3μA/mm and thus around five orders of magnitude below the drain current as shown in Figure 10.

The output characteristic shows a negative differential resistance due to lattice heating and simulated by solving the lattice heating equation. The maximum drain current is approximately 0.4A/mm as seen in Figure 11.

The Breakdown Voltage of this device is 870V as seen in Figure 12, and the leakage current is controlled by the traps.

Enhancement-Mode N-Polar GaN MISFETs
This example demonstrates simulation of an Enhancement-Mode N-Polar GaN MISFET [7]. The structure is shown in Figure 13. There is a growing interest in high performance enhancement mode GaN channel devices because of single voltage operation and simpler circuit topologies. The advantages of enhancement mode GaN FETs fabricated on N-polar GaN include reduced source/drain access resistance and wide bandgap barrier layers used for a polarization-induced field allowing 2DEG depletion under the channel. Removal of the AlN layer from the access region recovers the 2DEG induced by the bottom AlN layer. Plots of the bang diagram under the gate and under the nitride sidewall reveal 2DEG under the access region but not under the gate as seen in Figure 14.
The simulation of the transfer characteristic reveals a $V_t$ of around 1V and a maximum $I_{ds}$ of around 0.7A/mm at $V_{gs}=5V$ as seen in Figure 15.

Electron injection from the channel to the gate is limited by the AlGaN/GaN heterojunction. As a consequence no current offset is observed at zero drain since gate current is very low. This device exhibits a threshold voltage around 1V, a maximum drain current at $V_d=10V$ and $V_g=5V$ of 200mA/mm and a breakdown voltage of 640V as shown in Figure 17, Figure 18 and Figure 19 respectively.

Normally-off AlGaN/GaN Transistor with Conductivity Modulation

This example demonstrates simulation of a normally-off AlGaN/GaN transistor with conductivity modulation resulting from hole injection from a p-AlGaN gate to the AlGaN/GaN heterojunction [8]. The p-AlGaN gate allows normally-off operation.

When the gate voltage increases and reaches the built-in pn junction voltage at the gate (around 3.5V) holes inject into the channel and generate the equal number of electrons increasing the 2DEG. Electrons with high mobility will reach the drain under the effect of the electric field whereas the holes will stay since their mobility is much lower than the electron. The current is thus modulated by the number of holes injected. It is also interesting to notice that this device exhibits a double peak in the transconductance curve, a second proof of hole injection as shown in Figure 16.

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Fe Bulk Doping Related Current Collapse Phenomenon

This example demonstrates simulation of the “Current Collapse” and “Current Recovery” phenomenon resulting from population and de-population of Intentional Iron (Fe) Doping Traps under the gate of a GaN FET as a result of Gate to Drain Electric Fields.

Many publications suggest that unintentional surface traps are the main cause of the GaN current collapse phenomenon. In this example, we show that sometimes this is not actually the case. Current collapse in this device is mostly caused by intentional iron doping, whose main purpose is to create a semi-insulating buried layer to reduce the buried layer source-to-drain leakage path.

The device structure in this example is based on [9]. Substrate leakage current is controlled by a graduated concentration of deep level iron acceptor traps located 1eV below the conduction band edge.

The device is first biased with 0v on the gate and 5v on the drain. After a microsecond at this bias, the device is field stressed for only one further microsecond at 25v on the drain and -4v on the gate as seen in Figure 20. After this short bias stress, the device was returned to its original bias of 0v on the gate and 5 volts on the drain. After only one microsecond of bias stress, the drain current is significantly reduced demonstrating the current collapse phenomenon as seen in Figure 21.
A comparison structure file plot of the pre and post-stress ionized Fe trap density shows that the cause of the current collapse is actually the change in charge state of the Fe doping deep in the substrate under the gate, and also on the drain side between the gate and drain contacts as seen in Figure 22.

For completeness, the unstressed bias remained on the device until the traps became depopulated with electrons and the drain current returned to its original value. Interestingly, it takes over one week for the device to recover, (6e5 seconds) as seen in Figure 23. This very long recovery time may be incorrectly interpreted as device degradation from field-induced traps which is an irreversible effect resulting from electric field-induced reverse piezo-electric stress.

2-6 3D AlGaN/GaN HEMT Including Intrinsic Stress Effect

The device under consideration is a 3D AlGaN/GaN HEMT shown in Figure 24. 3D stress distribution is simulated by Victory Stress. This example produces stress distributions via the stress-liner made of nitride as shown in Figure 24 and Figure 25. Note that the stressor in this example is used to illustrate strain polarization on top of piezo and spontaneous polarization.
After the initial solution is obtained, the drain voltage is ramped to 1 V, then the IdVg characteristic is extracted from Vg=-8 to Vg=1.0 V as seen in Figure 26. The effect of strain is seen on IdVg. Overlay of 2D simulation results with 3D simulation results obtained with width=1 validates our 3D implementation.

Influence of the Gate to Drain distance on the breakdown voltage

This example demonstrates the influence of the gate-to-drain distance on the breakdown voltage with and without silicon substrate [10].

The structure consists of 20nm AlGaN with xcomp=0.2 and 1um GaN buffer layer as shown in Figure 27. Donor and acceptor traps are included in the simulation. Gaussian profile acceptor traps are used with a peak concentration close to the bottom of the buffer layer to mimic the fact that the material quality improves toward the surface of the device.

Donor Interface traps at the AlGaN/Nitride interface and acceptor interface traps at the GaN/Silicon interface are also included during the simulation.

Forward characteristic simulation reveals a threshold voltage of around -2V. Slow transient simulation is used to simulate the breakdown voltage curve. The deck is parametrized so that we can vary the distance between the gate and drain (LGD). DeckBuild DoE capability is used to automate simulations of BV versus LGD with and without substrate.

We can observe in Figure 28 an almost linear increase of BV versus LGD when silicon substrate is not present. An increase of the gate current is observed in Figure 29 near breakdown, and the value is of the same order as the drain current. This result indicates that BV is defined by an avalanche phenomenon between the gate and the drain as shown in Figure 30.

BV does not depend significantly on LGD when a silicon substrate is present due to charge accumulation at the GaN/Silicon interface, related to the presence of interface traps, which screen the electric field.
GaN HEMT Thermal Optimization using Flip Chip Structure

This example demonstrates two-dimensional electro-thermal simulations with heat sink structures.

Although the superiority of GaN HFET device characteristics has been demonstrated, the self heating effect has hindered the production of high power and high speed GaN-based switching devices. This effect can be significantly reduced by the cost effective heat-sink approach. In this example, in order to understand and control the self heating effect, a GaN HFET with a flip chip concept is simulated, and device characteristics are compared versus a normal structure.

For HFETs, the GaN/AlGaN epitaxial layers have been grown on either sapphire or SiC substrates. Although sapphire has the advantage of lower cost and availability in larger wafer sizes, its poor thermal conductivity (0.3 W/cm-K) limits the achievable powers due to severe self-heating. The self-heating effect can be significantly reduced by flip-chip mounting the devices onto highly conducting substrates such as AlN (1.8 W/cm-K).

The typical GaN HFET flip chip structure in this example is a Al0.25Ga0.75 N-GaN HFET on a sapphire substrate. The structure consists of an AlN layer as a heat sink, a 2.7nm undoped AlGaN layer, and two GaN layers which includes 20nm doped 1e15 GaN and 1um undoped GaN as shown in Figure 31.

The self-heating is a local increase of crystal temperature due to dissipated Joule electric power, this effect can significantly reduce the electron mobility and degrade device performance.

DC, Transient and AC simulations are performed and compared with and without the flip chip structure as shown in Figure 32, Figure 33 and Figure 34 respectively. As expected the performance of the device is better using the flip chip architecture.
Large Signal Output Power Analysis

This example describes how to simulate typical 10 GHz large-signal measured performance quantities related to power output, such as power out versus power as shown in Figure 35, power gain as shown in Figure 36 and amplifier efficiency as shown in Figure 37 as the device is over-driven into high distortion. The example also plots in Figure 38 the output signal shape versus time for each

![Figure 35. Power out versus power in.](image)

![Figure 36. Power gain versus power out.](image)

![Figure 37. Power Output Efficiency versus Power out.](image)

![Figure 38. Drain and gate voltage large signal.](image)

![Figure 39. Structure under test.](image)

The structure under test is shown in Figure 39.

Ten large signal input amplitudes are defined. Each of these waveforms are applied to the gate in order of increasing amplitude. After each waveform simulation is complete, a number of large signal parameters are calculated. The peak input and output voltages are extracted, followed by the exact times at which these peak voltages occurred. Then the input and output currents are extracted at the same times as the peak voltages occur. It is important to extract the currents at the same time as the peak voltages in order to take account of the phase between current and voltage, so that the correct power values can be calculated.
Conclusion
GaN is a very promising material for high power switching applications. However, development cost is becoming a serious concern for GaN manufacturers. This is why TCAD is so important in order to reduce cost and help optimize device performance.

Silvaco's Process and Device solutions have all the capabilities (i.e. state of the art mesh, discretization, solvers and physical models) that we think are essential to accurately simulate GaN based devices in 2D and 3D.

References