Introduction
Silicon has long been the semiconductor of choice for high-voltage power electronics applications [1,2]. However, wide-bandgap semiconductors such as SiC have begun to attract attention because they are projected to have much better performance than silicon [3-7]. In comparison with silicon, wide-bandgap semiconductors offer a lower intrinsic carrier concentration (10 to 35 orders of magnitude), a higher electric breakdown field (4 to 20 times), a higher thermal conductivity (3 to 13 times), and a faster saturated electron drift velocity (2 to 2.5 times).

SiC exists in over 200 polytypes with different crystal structures with the same stoichiometry. However, only the 6H- and 4H-SiC polytypes are available commercially as both bulk wafers and custom epitaxial layers. Both of these polytypes have a hexagonal crystal structure and a bandgap in the neighborhood of 3eV. Of the two, 4H-SiC is now preferable due to the more isotropic nature of many of its electrical properties.

SiC 2D and 3D Simulations
Simulating SiC devices is more challenging compared to Silicon. Indeed very low intrinsic concentration combined with high doping values is usually detrimental to convergence. Silvaco’s 3D Process and Device solution can handle this situation thanks to state of the art mesh, discretization and solvers. In the following paragraphs we will explain what are the ingredients that we think are essential to accurately simulate these type of devices in 3D. Everything mentioned in these paragraph is implemented in Silvaco’s 3D Process and Device framework called Victory.

Mesh and Discretization
For faster and more accurate device simulation, it is best to start out with a mesh that has a perfect geometric dual and that dual is the Voronoi tessellation of the vertices. This means that the perpendicular bisectors of each tetrahedral mesh edge form a convex finite volume which does not overlap those of its neighbors. It is equivalent to saying the mesh is Delaunay (i.e. the interior of the circumsphere of each tetrahedron does not contain any vertices). The finite volume boxes should also not overlap any region or domain boundaries. When these two conditions are met, the finite volume discretization is relatively straightforward, and can be done without introducing extra cross coupling or discretization errors (which would degrade the convergence or accuracy). One way to achieve this is to simply create a finite difference style grid with Cartesian grid lines extending all the way through the domain. Unfortunately this tends to result in a relatively large number of grid points, an even larger Jacobi matrix, and a slow simulation (especially in 3D). Recent advances at Silvaco in mesh generation however have resulted in algorithms which can create and refine meshes whose finite volumes have these two important properties, without introducing excessive numbers of grid points. An example of Delaunay mesh is shown in Figure 1.

At the end of the process simulation, the device meshing algorithm creates a pure unstructured Delaunay remesh of the results of the process simulation. A Delaunay mesh of a particular set of points has certain special mathematical properties compared to any other mesh of the same points. One example of this in 3D is that the largest radius of the smallest sphere enclosing any tetrahedron is minimized for a Delaunay mesh; this leads to a high-quality mesh of compact elements.

Continued on page 2...
The Delaunay device mesh is conformal in the sense that a point sampling of the features of the process mesh is produced whose Delaunay mesh resolves those features. These features can be viewed as zero, one, two or three-dimensional and are defined recursively; these are the fundamental vertices, edges, polygons and polyhedra composing the structure. The conforming point sampling has the special property that the corresponding 3D Delaunay mesh has lower dimensional Delaunay meshes embedded in it; this property does not hold in general for arbitrary sets of 3D points.

The algorithm used to calculate the conforming point set has two main improvements over those commonly seen in the literature:

- The number of points required to generate the conforming point set is often considerably less than standard approaches. This allows fewer elements and finer control of those elements by breaking the usual relationship between local feature size within the structure and the element size in that region. This lower number of elements leads to decreased device simulation time.

- Features with acute angles are handled in a clean, general way compared to standard methods. This decreases the complexity of the implementation and represents the fundamentals of a fully general nD conformal Delaunay algorithm.

The conformal Delaunay algorithm also supports a general framework for producing arbitrarily locally refined meshes. Refinement schemes are implemented as plug-ins outside of the core meshing code itself and any number of these can be applied in an arbitrary order to a given mesh. A number of TCAD-specific approaches to refinement have been implemented; these include steadily decreasing element size within semiconductor regions according to distance to the insulator region or the junction, refinement on the variation of net or total doping. All these refinements are fully automatic.

**Solver**

Mesh and discretization are only part of the overall problem. Fast and accurate simulation will also depend on the solver used during the simulation. A new solver have been developed to best fit the work done on the mesh and discretization.

The PAM solver is a domain decomposition type linear system's solver specifically designed for very large sparse linear systems. PAM solver is based on Yousef Saad's Parallel Algebraic Recursive Multilevel Solver pARMS [8]. The parallelization is done with MPI (Message Passing Interface). Each MPI process handles the solution of part of the linear system and the MPI processes run in parallel. After each MPI process finishes with its part of the linear system, each solution is broadcast back to the main MPI process, and the solution to the global linear system is formed and returned.

The main advantage of the PAM solver is the fact that the domain decomposition approach leads to fast solution of smaller sized linear systems which is carried out in parallel, thus significantly reducing the total solution time for very large sparse linear systems. It is also an accurate and robust solver.

Another advantage is that it is a very diverse solver allowing the use of several combinations of global and local preconditioners and two iterative solvers. It can be used for a wide variety of linear systems with both non-symmetric and symmetric matrices arising from different types of applications. It also supports extended precision; all computations can be done in 64, 80, 128, 160, 256 bit precision.
Extended Precision

In a device simulation, the calculation of the electrostatic potential depends on the space charge density, which includes the difference \((n-p)\) of the electron and hole concentrations. Simultaneously, the calculation of current conservation implicitly depends on the sum \((n+p)\) of these concentrations. Consequently, the convergence and accuracy of a device simulation requires the numerical resolution of the quantities \((n-p)\) and \((n+p)\).

To resolve these quantities, the calculations must be performed with at least

\[ P \geq \frac{\ln(n-p)}{\ln 2} \]

significant bits of arithmetic precision. From the theory of carrier statistics, we can then estimate that for a convergent and accurate simulation, we need to maintain a precision of:

\[ P \geq \frac{1}{\ln 2} \left( \frac{E_g}{kT} \right). \]

Therefore, the required precision \((P)\) depends on both the lattice temperature \((T)\) and on the bandgap \((E_g)\). In practice, the above inequality constitutes a loose upper bound, and we can frequently carry out a successful simulation with somewhat less precision than the relation indicates. This inequality also tells us that precision is more likely to be an issue with high-bandgap materials, and at low temperatures.

One way to skirt this issue is to consider only the majority carriers when solving the semiconductor equations. However, that option is unavailable if recombination is important, because recombination by definition involves both carrier types. In such a case, the most general solution is to carry out the simulation at a high level of precision.

When we discuss the precision of computer arithmetic, it helps to understand a little about the structure of floating-point numbers. Floating-point numbers are composed of three parts: the sign, the exponent, and the significand\(^9\). As its name suggests, the size of the significand corresponds to the number of significant bits in the number. In the above inequalities, \(P\) stands for the number of significant bits. The nominal precision of a floating point number is larger than the number of significant bits because it also counts the bits used for the sign and the exponent. In Victory Device and in Atlas, the various flags controlling the precision levels of the simulator and of the solver always refer to the nominal precision.

By default, Victory Device and Atlas use a nominal arithmetic precision of 64 bits. In order to support the simulation of high-bandgap materials in particular, these simulators can now run at several levels of extended precision as well. The level of precision is selected by means of a command-line flag (which in DeckBuild would be passed as one of the arguments to the SIMFLAGS parameter of the GO statement). The arithmetic precision levels currently supported by Victory Device and by Atlas are summarized in Table 1.

For well-converged solutions, the run-time increases with the precision. This increase is especially significant at the highest precision levels. A 256-bit solution may take twenty times longer than a 128-bit one! For example, a simulation that consumed 10 hours using 256-bit arithmetic might take just a half-hour using 128-bit arithmetic. Memory requirements also increase with the precision. On the other hand, certain simulations that have difficulty converging at the lower precision levels are likely to run faster if the precision level is increased. Accordingly, the optimum precision level for a particular problem is likely to be the minimum level that yields good convergence during the solution.

4H-SiC has a bandgap of 3.26 eV. The second inequality above suggests that a simulation of a device composed of this material may require a precision as high as 185 bits. From the table, we can see that to get at least 185 bits of precision we must resort to 256-bit arithmetic. Now, 185 bits is a rough upper limit, so in some cases we may be able to simulate SiC devices using only 128-bit arithmetic without doing anything special, even though the precision available from 128-bit arithmetic is only 104 bits. In general, however, we can expect to either have to employ higher-precision arithmetic, or to take steps to reduce the precision requirement.

One way to reduce the precision requirement is to limit the intrinsic concentration affecting Shockley–Read–Hall recombination to at least a minimum value \((N_I, \text{MIN})\). In heavy-doped regions, we can estimate the value of \(N_I, \text{MIN}\) necessary to bring the spread in carrier concentrations within the scope of the available precision \(P\):

\[ N_I, \text{MIN} = \frac{N_{\text{net}}}{\sqrt{P^{\frac{1}{2}}}}. \]

where \(N_{\text{net}}\) is the net doping. However, there is no reason to employ this limit if it is less than the nominal value of the intrinsic concentration,

\[ n_i = \sqrt{N_c N_v} \exp \left( \frac{E_g}{kT} \right). \]

where \(N_c\) and \(N_v\) are the densities-of-states at the conduction and valence band edges.
For SiC with $N_{net} = 1e19$ and $P = 104$, the above estimate works out to $NI.MIN = 2220$. Practical experience has been that one can often get by with values of $NI.MIN$ much less than this.

Raising $NI.MIN$ of course will tend to raise the leakage current. For many typical high-bandgap structures, however, the calculated leakage current is so low that it is non-physical. Since electrons and holes are quantum particles, we can only have an integer number of them. Thus a calculated leakage current of $1e^{-27}$ A corresponds to an average of one carrier crossing the device every five years. Most of the time, in this case, there will be zero current. If we increase $NI.MIN$ such that the leakage current here is raised by a factor of a million, to $1e^{-21}$ A, then that corresponds to an average of one carrier crossing the device every three minutes. Again, we can say that most of the time there is zero current.

On the other hand, raising $NI.MIN$ has little effect on the breakdown voltage calculated for a device. Consequently, if we are interested in determining the breakdown voltage, setting $NI.MIN$ to a judiciously chosen value can speed up the calculation significantly.

Here is an example illustrating these points.

Figure 2 shows the top section of a SiC power device. This device has a long drift region about 160 µm in extent, with low doping, giving the device a high breakdown voltage. The width of the device is here assumed to be 1 µm. There are two contacts at the top of the device, a gate to the left, and a drain contact at the bottom.

To determine the breakdown voltage of this device, we perform a simulation in which the bias on the drain is gradually raised until breakdown occurs. In this simulation, we use the model of Hatakeyama et al [10] for anisotropic impact ionization, with the $<0001>$ axis of the crystal oriented so that it is parallel to the long axis of the device. We also use the Shockley–Read–Hall [11, 12] model for recombination.

Figure 3 shows the results of this simulation, performed using various levels of arithmetic precision and various values for $NI.MIN$. As predicted for this material, 256-bit arithmetic is required when $NI.MIN=0$. With higher values of $NI.MIN$, we can reduce the precision of the arithmetic yet still obtain a converged solution. At $NI.MIN=1e2$ we can use 128-bit arithmetic, and the simulation takes only 5% of the time needed for a 256-bit calculation.

From $NI.MIN = 0$ to $NI.MIN = 1e2$, the voltage predicted for the onset of breakdown rises from 14000 to 14080 V, a difference of just 0.6%. The predictions for the leakage current
vary greatly, but even the highest value of $1 \times 10^{-18}$ A is too small to be measured in a real-world device. In real-world terms, then, the predicted leakage current is effectively zero and the predicted breakdown voltage is $1.40 \times 10^4$ V.

### Applications

In this section we will review and show 2D and 3D simulations of different types of structures using 3D Process and Device simulators. We will start to compare 2D and 3D breakdown voltage simulation of an identical structure in 2D and 3D for validation purposes. We will then show the simulation results of a Trench MOSFET. This particular structure will have a rounded bottom trench as well as a floating P region underneath the trench for improved blocking capability and thus increased breakdown voltage. We will then show also on a Trench MOSFET how we can optimize the breakdown voltage as a function of the trench shape. Finally, IGBT simulation exhibiting very high breakdown voltage will be demonstrated.

In order to create the 3D structure we used our 3D Process simulator, very suitable for 3D SiC power devices simulation since it is layout driven, accurate, fast and easy to use. After the process simulation is done a 3D structure is saved using a 3D tetrahedron mesh to ensure that any shape created during 3D process simulation is well conserved and transferred to the 3D Device simulator.

#### Comparison of 2D and 3D Simulation Using the Same Structure

The following example shows a comparison between 2D and 3D breakdown voltage simulation of a vertical SiC MOSFET.

Hatakeyama, et al. [10] have developed an anisotropic impact ionization model for materials with a hexagonal crystal structure, including 4H-SiC. The ionization coefficients in this model depend on the strength of the electric field and on the orientation of the field with respect to the optical axis of the crystal.

You can specify the orientation of the optical axis of the crystal in Victory Device by supplying values for ZETA and THETA parameters on a MATERIAL statement. ZETA defines the angle the optical axis makes with the y coordinate axis. THETA defines the angle that the projection of the optical axis onto the x-z plane makes with respect to the x-axis (measured clockwise around the y axis). The defaults are zeta=0 degrees and theta=0 degrees, making the <0001> direction parallel to the y-axis.

To make the optical axis parallel to the z-axis for 3D simulation so that the optical axis points toward the SiC surface for both 2D and 3D, we set ZETA=90 degrees and THETA=90 degrees on the MATERIAL statement.

Figure 4 shows the Net Doping in the 3D structure after process simulation. As shown in Figure 5, and as expected, the breakdown voltage is the same in 2D and 3D. Figure 6 shows the same impact ionization rate and location in the 2D structure and in a cutplane from the 3D structure, validating that breakdown voltage is the same for both 2D and 3D structures.

#### Comparison of 2D and 3D Simulation Using the Different Structure

The following example shows 3D simulation of a vertical DMOS where the bottom of the trench is rounded and with a floating P-type region under the trench to increase the breakdown voltage.
Because the structure in this case is 3D it is interesting to notice that doing 2D simulations will not allow accurate calculation of the breakdown voltage. Multiple 2D simulations were performed: one along the side of the device, another one along the diagonal, and finally one in between. All of them exhibit different breakdown voltage as shown in Figure 7, and also different from breakdown voltage from the 3D structure shown in Figure 8.

If we imagine the 2D structure as possessing a cylindrical symmetry about the X=0 axis, the area available for the lateral expansion of the depletion region is invariant under rotation about this axis. This will result in the same breakdown voltage in 2D and 3D. On the contrary, the 3D structure in this example does not possess such a cylindrical symmetry. In fact, the depletion region of the 3D structure can expand along the diagonal direction further than along the X and the Y direction. This leads to a higher breakdown voltage and has been verified by performing multiple 2D simulations.

In summary, the 3D structure provides a larger area for lateral depletion than the 2D one, and therefore exhibits a higher blocking capability. Therefore it has to be simulated in 3D.

Simulation results showing Electric Field, Impact Ionization Rate and Electron Current Density are shown respectively in Figures 9, 10, and 11.

It is interesting to notice that due to the presence of the P-type region underneath the trench, making a p-n junction, the maximum Electric Field and thus impact ionization rate is maximum at this junction location and not at the trench corner.
Breakdown Voltage Optimization Versus Trench Shape

The following example demonstrates the effect of the shape of a trench on IV and BV characteristics.

In this example we compare 3 different structures. One fully Manhattan (i.e. 90 degree layout and trench) versus 2 structures one having rounded trench edge and another one having rounded edge and angled trench.

In this example we did not focus only on breakdown voltage simulation but we also have simulated static performance of the structure. IdVg simulations shown in Figure 12 illustrate a 3D specific effect. Indeed a “hump” effect is observed on the IdVg characteristic as reported in [13]. This parasitic transistor results from current crowding at the edge of the trench as shown in Figures 14 and 15. In Figure 14 we can see current flowing along the edge of the trench when this trench is sharp, whereas we do not have any current when the trench rounded and angled. This “hump” effect is characterized in the IDVG curve as a parasitic transistor. This may be problematic in term of power consumption since it increases the off-current. To suppress this parasitic effect a non-Manhattan structure is used (including non 90 degree layout as well as angled trench).

In Figure 13, we clearly see the effect of the trench shape on BV characteristics. BV simulation reveals that the breakdown voltage can be increased by 30% using rounded trench edge and angled trench due to impact ionization occurring not anymore only at the corner of the trench as can be seen in Figures 16, 17 and 18.
Very High IGBT Breakdown Voltage Simulation

The following example demonstrates a 3D trench SiC IGBT simulation.

The particularity of this device is to have low doping long drift region of about 160um. This will lead to high breakdown voltage around 12KV. As expected and as mentioned earlier BV is affected by the shape of the trench. Maximum BV is obtained when the trench edge is rounded as shown in Figure 19 and 20.

Conclusion

Silicon based power devices are still dominant today in power electronics. However, wide bandgap semiconductors like SiC are now more and more used for high power, high-temperature applications because of superior thermal conductivity, lower intrinsic carrier concentration and better on-resistance compared to Silicon, which is a key figure of merit in power switching applications.

Silvaco anticipated the simulation needs years ago and is now able to provide a complete flow from process to device in 2D and 3D. The flow is now ready to address the increasing needs of accurate SiC based devices simulation, to develop and optimize this promising technology.

Figure 14. 3D distribution of electron current density in a sharp trench at Vg=12V VD=0.1V.

Figure 16. 3D Impact Ionization rate distribution showing that breakdown occurs at the corner of the trench when the structure is Manhattan.

Figure 15. 3D distribution of electron current density in a rounded and angled trench at Vg=12V VD=0.1V.

Figure 17. 3D Impact Ionization rate distribution showing that breakdown occurs at the corner of the trench even with rounded edge trench.

Figure 18. 3D Impact Ionization rate distribution showing that breakdown no longer occurs only at the corner of the trench when the trench is angled etch.
Acknowledgement

The authors would like to express their gratitude to the members of the Silicon Carbide Group of AIST for supplying valuable advices validating our Process and Device flow.

References

Single Event Gate Rupture (SEGR) Simulations in a Power MOSFET

Introduction

With the increasing interest in power devices as high power solid state switches for the electric and hybrid car industries, there is renewed interest in the investigation of power device failure modes. A Single Event Gate Rupture (SEGR) event is one such failure mode and the simulation of such an event is the subject of this article. While it is more likely to happen in space, where there is no protection from the atmosphere, an energetic particle can also cause a Single Event Upset (SEU) in terrestrial applications.

A Single Event Upset (SEU) event is caused by a high energy particle or photon interacting with the material constituents of a device. The particle or photon gradually loses energy as it passes through the device, transferring this lost energy to the material constituents of the device by ionizing the material. The net result is a high density ionized track created in the device which follows the usually straight line path of the primary particle or photon.

If the area of the device through which the ionizing particle or photon passes has no internal electric field, then the resulting high density of positive and negative charges will not be separated by any meaningful distance, and they will simply recombine.

However, if there is an electrical field in the device prior to the strike, the high density of negative and positive charges created by the primary particle or photon can become separated (if they are a mobile species), thus reducing the chance of recombination. Once the positive and negative charges have become separated, the electrical field in the device can be disturbed to a significant degree.

In a Single Event Gate Rupture (SEGR) event the field across the gate oxide for certain MOSFET device bias conditions has an additive relationship to the field created by the separation of mobile charges created by the primary ionizing particle or photon. The electric fields from the applied bias at the terminals, and the electric field from the separated ionizing track charges in this case, make the device especially sensitive to an SEU strike. This can create an electric field that temporarily exceeds the dielectric breakdown field strength of the gate oxide, resulting in a permanently damaged device.

Experiments have shown that there is a critical and almost constant electric field strength for gate oxides, which will result in dielectric breakdown and permanent damage to the device even if this electric field is only present for time-frames measured in pico-seconds. This critical electric field required for gate dielectric breakdown in the pico-second time-frame could be considered as the “intrinsic” breakdown field of the gate oxide. For typical, moderately thick, thermally grown silicon dioxide gate dielectrics, this “intrinsic” breakdown field strength is approximately $1 \times 10^7$ V/cm.

As an important note, this “intrinsic” breakdown field strength should not be confused with the lower breakdown field that would be measured for that same gate oxide if a sustained DC bias was applied for many seconds. A sustained applied gate oxide field will result in a lower measured breakdown voltage due to the slow movement of mobile ions and other slow effects, which does not occur in the pico-second time-frame of an SEU strike.

In order to model a Single Event Gate Rupture event in TCAD, therefore, all that is required is to monitor the gate oxide field during the SEU event, and if at any time, the electric field across the gate oxide exceeds the “intrinsic” breakdown electric field, then the device can be considered to have suffered irreparable and permanent damage.

Simulations

The simulation strategy in this example was to reduce what would normally be a three dimensional problem into a two dimensional problem by using circular symmetry in the device simulations, and also to define the SEU strike to occur vertically at the center of the circular symmetry, so as not to incur any errors in the effective charge track shape.

Important Note:

A vertical SEU strike at the center of a circular symmetric device is the only problem which can be correctly reduced to two dimensions. If the ion strike was at an angle, or the location of the strike was anywhere except the center of circular symmetry, Silvaco’s full three dimensional process, device and SEU simulation tools would be required.

A process flow of a typical power MOSFET was created in Athena incorporating the fully coupled diffusion models and Monte-Carlo implants throughout. The resulting structure is shown in Figure 1.
For the device simulation, an SEU strike with an LET of 37.2 (corresponding to a Bromine Ion), is simulated, with the strike occurring at the center of the device (X=0). The syntax for creating the SEU strike is invoked using the “SINGLEEVENTUPSET” statement, where the basic parameters of the primary ion are defined, such as entry and exit points and LET etc. For this example, the statement is given below:

```
SINGLEEVENTUPSET entrypoint="0,0,0" \  
extpoint="0,8.5,0" radialgauss \  
b.density=$density pcunits radius=0.07 \  
t0=1e-14 tc=1e-15
```

The entry and exit points are defined as X,Y,Z points (Z=0 for a 2D device). The ion track charge density parameter, “b.density” is defined as a variable = (LET*0.011) when the charge has units of pico coulombs, specified by the parameter “pcunits”. The radius of the track and the Gaussian roll-off of charge density are defined by the parameters “radius” and “radialgauss” respectively. The primary ion strike time and duration are defined by the “t0” and “tc” parameters respectively.

At the time of the SEU strike, a bias of -13.9 volts is applied to the gate and 30 volts on the drain. This bias condition creates a near critical condition close to that required for a gate rupture event to occur.

The gate oxide field was probed near the strike, such that

gate oxide field versus time could be plotted before, during and after the SEU strike. The “probe” statement allows specific physical quantities in the structure file that are located at specified coordinates in the device, to be exported to a log file, such that these quantities can be continuously calculated during transient or DC simulations. The probe statement in this example is given by:

```
probe name=Strike_Field field dir=270 /  
ex=0.02 y=-0.02
```

The “name” parameter in the probe statement is what will appear in the plotting tool, TonyPlot, as the name of the quantity being plotted. The “field” parameter tells the statement which calculated quantity in the structure file is required to be extracted as a line graph. Since electric field is a vector quantity, the “dir” parameter defines the direction of the extracted vector as the number of degrees the vector deviates from the X-axis. Since the applied field across the gate is negative, specifying a normal vector direction of 90 degrees would result in negative field values being extracted. Specifying a field direction of 270 degrees adds a further 180 degrees to the extracted vector direction which reverses the extracted field polarity to a positive number which is simply done to create a more aesthetically pleasing graph.

After the SEU strike occurs, this critical reversed bias condition results in a peak gate oxide field that increases by over 3 times the field from just the DC bias condition alone. The peak gate oxide field versus time is shown in Figure 2. It can be seen that the peak oxide field is very close to the “intrinsic” breakdown field of the gate oxide, meaning that this device was close to suffering irreversible gate oxide damage.
The evolution of the hole concentration distribution was also monitored at the strike event and at 5, 50 and 150 picoseconds after the strike. The effect of the electric fields present before the strike on charge separation and subsequent transportation can be seen clearly in the time evolution snapshots shown in Figure 3.

The effect of the SEU strike on the drain current was also monitored over a longer time span and is shown in Figure 4. Just for completeness the breakdown voltage and unsaturated threshold voltage (for $V_d=0.1$ volts) were also simulated and are shown in Figures 5 and 6 respectively.

Conclusions

In conclusion, due to the nature of the near instantaneous breakdown characteristics of silicon dioxide, the simulation of Single Event Gate Rupture (SEGR) events is a fairly straightforward task of monitoring the peak electric field in the gate oxide during and immediately after the SEU strike. If the peak electric field across the gate exceeds the “intrinsic” value of approximately $1e7$ V/cm for thermal silicon dioxide, then it can be assumed that irreversible damage has occurred.
Empirical Low-field Mobility Models for III-V Compounds

One of the problems in drift diffusion based simulation of compound semiconductors is the lack of meaningful default material characteristics over the range of usable composition, doping and temperature.

Although the experienced user will eventually develop a set of defaults calibrated to his particular application, the path to calibration can be fraught with disappointment and extra effort due to the non-physicality of the initial default parameters for a given model.

Recognizing this difficulty the authors Sotoodeh, Khalid and Rezazadeh [1], have developed a methodology suitable to interpolate values of the Caughey-Thomas low field mobility model [2] to a wide range of materials, temperatures, dopings and compositions.

The following figures represent the ATLAS implementation of the Sotoodeh model compared to the references used by Sotoodeh to calibrate the model in the original paper. From these papers you should get a very good idea of the range of applicability and accuracy of this new model.

Figure 1. The ATLAS implementation of Sotoodeh (1). Variation of low-field electron mobility in In0.53Ga0.47As vs temperature with three different doping concentrations according.

Figure 2. The ATLAS implementation of Sotoodeh (1). This shows the variation of electron mobility vs. doping in GaAs.

Figure 3. The ATLAS implementation of Sotoodeh (1). This shows the variation of electron mobility vs. composition in AlGaAs.

Figure 4. The ATLAS implementation of Sotoodeh (1). This shows the variation of hole mobility vs. doping in GaAs.
Figure 5. The ATLAS implementation of Sotoodeh (1). This shows the variation of hole mobility vs. composition in AlGaAs.

Figure 6. The ATLAS implementation of Sotoodeh (1). This shows the variation of electron mobility vs. doping in InP.

Figure 7. The ATLAS implementation of Sotoodeh (1). This shows the variation of hole mobility vs. doping in InP.

Figure 8. The ATLAS implementation of Sotoodeh (1). This shows the variation of electron mobility vs temperature and doping in GaP.

Figure 9. The ATLAS implementation of Sotoodeh (1). This shows the variation of hole mobility vs temperature and doping in GaP.

Figure 10. The ATLAS implementation of Sotoodeh (1). This shows the variation of electron mobility vs doping in InGaP.
Call for Questions
If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department
Phone: (408) 567-1000 Fax: (408) 496-6080
e-mail: support@silvaco.com

Hints, Tips and Solutions Archive
Check our our Web Page to see more details of this example plus an archive of previous Hints, Tips, and Solutions
www.silvaco.com

References
JOIN THE WINNING TCAD TEAM

USA Headquarters:

Silvaco, Inc.
4701 Patrick Henry Drive, Bldg. 2
Santa Clara, CA 95054 USA

Phone: 408-567-1000
Fax: 408-496-6080

sales@silvaco.com
www.silvaco.com

Worldwide Offices:

Silvaco Japan
jpsales@silvaco.com

Silvaco Korea
krsales@silvaco.com

Silvaco Taiwan
twsales@silvaco.com

Silvaco Singapore
sgsales@silvaco.com

Silvaco Europe
eusales@silvaco.com

SILVACO