Simulation of Stresses and Mobility Enhancement Factors in 3D Inverter Cell

Introduction

The analysis and characterization of stress effects have become an integral part of semiconductor technology and device design. In a typical semiconductor process flow the stresses are generated primarily due to volume expansion or contraction of the adjacent materials during temperature variations. Stresses could also be generated during oxidation, silicidation, etching, and deposition processes or due to lattice expansion or contraction after introducing large doses of dopants. Simulation of process induced stresses is an important component of traditional TCAD analysis since these stresses could have adverse or positive effect on individual process steps or on final device characteristics.

It is even more important to accurately simulate and optimize so-called stress engineering processes. Stress engineering is a deliberate introduction of stresses into device structures with a goal to enhance carrier mobility and consequently device performance. The most common method of introducing desirable stresses into a transistor channel region is deposition of high tensile or high compressive films of nitride type materials [1]. This method is called the global stress engineering. Another method introduces stresses by formation of locally strained source/drain regions [2-5]. These local regions could be created, for example, by epitaxial growth of compositional Si:Ge or Si:C materials.

In this paper we use 3D simulator VICTORY Stress to analyze stress effects on carrier mobilities of individual n-FinFET and p-FinFET devices as well as on characteristics of an inverter cell consisting of one n-FinFET and two p-FinFETs. The stresses in a whole cell are analyzed in this paper for the first time. Typically stress simulations have been preformed just in separate devices. However, it appears that proximity effects may require simulation of the whole cell. Both global and local methods of stress engineering are considered for each device type.

Verification of VICTORY Stress

It is very difficult to reliably estimate absolute accuracy of a 3D stress simulation. We have performed numerous simulations for different device structures using VICTORY Stress and compared the results with simulations and conclusions of other authors [1] – [6]. We will discuss some details of these comparisons elsewhere. Here we just want to note that in most cases VICTORY Stress simulations correspond to measured and numerical results of these papers. As an example we would like to highlight comparisons with Micro-Raman Spectroscopy stress field measurements presented in [2]. VICTORY Stress simulation results shown in Figure 1a and Figure 1b quantitatively confirm conclusions of paper [2] that locally strained recessed Si$_{0.8}$Ge$_{0.2}$ S/D regions induce compressive stress in the MOSFET channels between them and that the absolute value of this stress increases with decreased spacing between these recessed regions and with increased thickness of these regions.

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Motivation for Stress Simulation in An Inverter Cell

Many papers on stress engineering (see, for example, [1]-[6]) used numerical simulation to analyze the effect of different stress implementation methods on carrier mobilities for various FET device configurations (classical CMOS, SOI, FinFET etc.). The conclusions of these simulations are actually fairly obvious: both thin film liners (compressed for p-type devices, tensile for n-type devices) and stressed S/D regions (compressed for p-type devices, tensile for n-type devices) implemented near the gate significantly increase corresponding carrier mobility of all types of devices. Simulations and measurements of electrical characteristics prove this conclusion. However, to our knowledge, there are no published stress simulation results for a cell consisting of several individual devices located in proximity of each other. We believe that it is important to know how stresses from different sources interact with each other in areas of interest, for example, under the gates of various devices in a cell. These interaction effects could be even more pronounced when CDs of individual devices and distances between them scale down. In order to investigate these effects, we used VICTORY Stress simulations in a FinFET inverter test structure.

The inverter cell consists of three FinFETs: one FinFET is of n-type and the other two are p-type devices located parallel to each other as shown on the layout (Figure 2). The resulting whole cell structure was obtained from this layout using VICTORY Cell 3D process simulator and shown in Figure 3. A partial “np-cell” consisting of one n-type FinFET and one p-type FinFET in sequence (see Figure 4) as well as individual n-type FinFET (Figure 5) and p-type FinFET (Figure 6) devices were also obtained by VICTORY Cell using corresponding portions of the layout.

Figure 1a. The XX-stress field and its profile along the cut at 30nm below Si surface for a test structure with series of recessed Si$_{0.8}$Ge$_{0.2}$ regions of 0.15 micron thickness and gate areas with varying gate lengths (8, 4, 2, 1, and 0.5 microns).

Figure 1b. The same as Figure 1a only with the recessed Si$_{0.8}$Ge$_{0.2}$ regions of 0.3 micron thickness.

Figure 2. Layout of the inverter cell.

Figure 3. 3D view of the whole inverter cell.
Simulation Results

The 3D stress distributions for all four structures were simulated with the following values of intrinsic stress: 1GPa (tensile) for liners and S/D regions in n-type device and -1GPa (compressive) for both types of stressors in p-type devices. This value of intrinsic stress roughly corresponds to compressive Si$_9$Ge$_{10}$ and tensile Si$_9$C$_{01}$ (Young modulus $E$=187 GPa and Poisson ratio $\nu$= 0.28 were used in these estimations). The elastic properties of the liners correspond to those of Si$_3$N$_4$. The elastic properties of silicon fins correspond to those of isotropic silicon. Though VICTORY Stress can take into account anisotropic elastic properties of silicon and other materials, this anisotropy has a very small effect in silicon because its tensor of elasticity varies insignificantly for different crystallographic orientations. However, the mobility enhancements noticeably depend on silicon crystal orientation because the tensor of piezoelectricity varies significantly for different crystallographic orientation. The following equations were used for the n- and p- mobility enhancement factors for (100)<100> and (110)<100> crystallographic orientations in silicon:

$$\begin{align*}
\mu_{n100} &= 1.0 - (-1.022\sigma_{xx} + 0.534\sigma_{yy} + 0.534\sigma_{zz}) \\
\mu_{p100} &= 1.0 - (0.066\sigma_{xx} - 0.011\sigma_{yy} - 0.011\sigma_{zz}) \\
\mu_{n110} &= 1.0 - (-0.311\sigma_{xx} - 0.175\sigma_{yy} + 0.534\sigma_{zz}) \\
\mu_{p110} &= 1.0 - (0.718\sigma_{xx} - 0.663\sigma_{yy} - 0.011\sigma_{zz})
\end{align*} \tag{1}$$

In these equations the stresses are in units of GPa and coefficients of piezoresistivity are in 1/GPa.

Tables 1 and 2 summarize the stress values $\sigma_{xx}$, $\sigma_{yy}$, and $\sigma_{zz}$, and mobility enhancement factors $\mu_{n100}$, $\mu_{n110}$, $\mu_{p100}$, and $\mu_{p110}$, which were averaged by integration of corresponding stress distributions along the cut 5nm below the fin-oxide boundary under the gate as shown, for example, in Figure 7. Table 1 shows results for liner stressors and Table 2 shows results for S/D stressors. Note, that “pl” corresponds to p-type device which is aligned with n-type device in the whole cell, while “p2” corresponds to the second p-type device.
From numerical data summarized in Table 1 it is clear that the stresses and mobility enhancements for each device in the whole cell (rows 1, 2, and 3) and in the np-cell (rows 4 and 5) noticeably differ from stresses and enhancements obtained by simulation of individual devices (rows 6 and 7). This happens due to interaction between n-liner and p-liner.

Table 2 doesn’t demonstrate significant difference between results obtained for cells and individual devices. This is apparently because of the local nature of S/D stressors in this test configuration. However, the interaction effect could be more pronounced for different S/D stressor configurations or for more dense cell layouts.

Conclusions

We demonstrated that a combination of 3D process simulator VICTORY Cell and 3D stress simulator VICTORY Stress allows fast and accurate stress analysis of complex cell structures. The largest structure in this study consisted of more than 4 million tetrahedra and it took just 10 – 20 minutes to simulate the formation of the structure and calculate stress fields in it. We clearly showed that in some cases it is important to simulate stresses not just in an individual device’s structures but in the whole cell. The exceptional speed of VICTORY Cell and VICTORY Stress allows the performance of detailed analysis and optimization of various stress engineering schemes by varying geometrical characteristics, orientation, CDs, and material composition of each device as well as by changing location and density of the individual devices inside the cell layout.

References


