Current Collapse Phenomenon in GaN HFETs resulting from Intentional Bulk Iron (Fe) Doping and Un-intentional Interface Traps

Introduction
The Gallium Nitride-based material family has fundamental material properties which make it an attractive candidate for semiconductor device fabrication.

These properties include:
1. High saturation velocities and breakdown field strength
2. Direct bandgap, allowing fabrication of light emitting devices
3. The ability to form hetero-structures using aluminum or indium
4. Large bandgaps allowing high temperature operation

Another stand-out feature of GaN based materials are their very high levels of spontaneous and strain induced piezo-electric charge. This material feature, however, has both advantages and disadvantages.

The advantage of an unusually strong piezo electric effect is that conduction channels or 2D electron gas regions can be formed without the need for doping. The lack of doping removes impurity scattering effects, thus allowing for intrinsic carrier mobilities and therefore low on resistance in conducting channels.

The disadvantage of strong piezo-electric effects is that not only does strain create charge accumulation and therefore electric fields at interfaces, but the reverse is also true. Applied electric fields during device operation also create strain and therefore the accumulation of strain-related defects. These strain-related defects can create permanent and irreversible degradation damage to the device.

Another disadvantage of using un-doped devices is that there is no intrinsic shielding of electric fields that originate from the population and de-population of interface and bulk traps that can change occupancy depending on applied bias. To further complicate this undesirable sensitivity to charge trapping and de-trapping, the large band-gaps of this material family mean that these traps can be at very deep levels, making some of the trapping and de-trapping events have time constants that can be approximately a week or more, or less than a few hundred microseconds for the same trap, depending on bias conditions. These deep traps at insulator interfaces and in the bulk from intentional iron (Fe) doping create the phenomenon of “current collapse” which is the subject of this article.

In essence, “current collapse” is an undesirable “memory” effect, since the conduction current of the device can depend quite strongly on the previously applied voltages, and also on how long these previously applied voltages were present.

Structure Creation
A quick literature search revealed numerous publications on current collapse, so a suitable simulation device structure was chosen from one of the many publications. In this particular example, the device reference was from the 2011 PhD thesis of Daniel Balaz from the University of Glasgow, entitled “Current collapse and device degradation in AlGaN/GaN heterostructure field effect transistors”.

The structure is created using ATLAS syntax and the spontaneous and piezo-electric charge concentrations are automatically calculated using the “substrate, polarization and calc.strain” parameters in the region statements.

Substrate leakage current is controlled by a graduated concentration of deep level iron (Fe) acceptor traps located 1eV below the conduction band edge using the doping statement and the key parameter “trap”. The iron (Fe) doping concentration was graded from 1e18/cm3 1um deep into the GaN substrate to a reduced concentration of 1e16/cm3 close to the surface.

The surface traps were created using the “intrap” statement. For analytical simplicity, only a single level interface acceptor trap located 0.8eV below the conduction band edge was used. A single trap energy which differs from the Fe trap energy, will make the contribution of the interface traps to the resulting transient curves much more pronounced, which is what was needed for this illustration.

The areal density of the interface traps used in this example was 9e12/cm2. This density was chosen to exaggerate any interface trap effect and represents the interface trap density required to approximately halve the conduction current of the device, compared to when no interface traps were present. In respect to the interface trap density and energy, the construction of the device departs from the one described in the Thesis, since in this article we aim to show the effect of interface and bulk traps on the conduction current rather than simply matching a measured device.

A zoomed-in diagram of the structure under test is shown in Figure 1.
Electrical Simulations and Results

The device was biased into 2 different conditions. Firstly, the device was biased into a “low stress” condition, with 5 volts applied to the drain and zero volts applied to the gate. This initial bias condition simulated the device in a steady state condition (dc bias ramp) as far as the interface trap and bulk iron (Fe) trap occupancies were concerned.

After continuing the initial equilibrium bias for 1 millisecond in transient mode, the device was pulsed into a high stress condition, 25 volts on the drain and -4 volts on the gate, for a further one millisecond, before being returned to its original bias condition with 5 volts on the drain and zero volts on the gate. The voltage pulse train on the gate and drain electrodes is shown in Figure 2.

The resulting drain current response of the bias train described above is shown in Figure 3.

Since we are modeling the reversible current collapse phenomenon and not irreversible current degradation, if the bias voltage of 5 volts on the drain and zero volts on the gate remains on the device, the traps should gradually return to steady state occupancy conditions. To test the validity of the simulation, therefore, the post stress bias was allowed to remain on the device for a further 10 million seconds (approximately 16 weeks). Figure 4 shows the resulting current transient response.

As can be seen from Figure 4, contrary to assertions from most publications, the majority of the current collapse phenomenon results from intentional iron doping that was put there to reduce bulk GaN substrate parasitic current leakage paths. The interface traps only accounted for a very small fraction of the overall effect. Also notice that the device takes approximately one week to recover.
back to steady state conditions, a time that is so long, it could be mistakenly concluded that the device was irreversibly damaged by the defect degradation mechanism described earlier in this article. This indicates that Characterization Engineers need to be very careful when making conclusions about what is actually going on.

To prove that the majority of the current collapse phenomenon was the result of intentional iron doping and not interface traps, the simulation was repeated, but the interface trap population was removed. The results are shown in Figure 5.

As can be seen from Figure 5, the form of the drain current transient is identical to when interface traps are present, except that the “hump” in the curve at approximately 30 seconds is missing since there are no interface traps in this simulation.

To further illustrate the magnitude of the effect of iron trapping, Figure 6 shows the ionized trap density of Fe traps before bias stressing and 1 millisecond after bias stressing was removed. The difference in occupancy shows that the device is most sensitive to iron trap density under the gate area and under the region between the gate and drain near the surface.

Figure 6 really highlights the disadvantage of devices with no doping. The effect on iron trap occupancy continues down to a depth of almost 1μm into the substrate, and approximately 1μm in the horizontal direction towards the drain contact. Distances are 4 times larger than the gate length.

**Conclusions**

In conclusion, we have shown the importance of using simulation to fully understand the physical phenomenon interplay between the effects of intentional iron doping and unintentionally introduced insulator interface traps. We have shown that intentional iron doping can play the major role in the undesirable “current collapse” phenomenon. We have also shown that the recovery time for the device to return to steady state conditions can be in the order of a week or more. These long recovery times could easily be mistaken for permanent degradation damage, which is a similar but different and permanent effect. This has served to illustrate how careful Characterization Engineers must be when distinguishing between these two similar but different effects.