Thermal Optimization on GaN HFET Using Flip Chip and Through Wafer via Structures

Introduction
GaN heterojunction field effect transistors (HFETs) have been under extensive investigation because of their projected superb performances as high-power RF devices. The inherently high breakdown field arising from the wide bandgap guarantees not only the high power input/output characteristics but also extreme device shrinkage which is a huge advantage for increasing the highest operation frequency. Two-dimensional electron gas (2-DEG) with the charge density ten times higher than that of GaAs-based HFET and the mobility well exceeding Si enables a very low on-state resistance indispensable to RF devices. Although the superiority of the device characteristics has been demonstrated, the self heating effect has hindered the production of high power and high speed GaN-based switching devices. This effect can be significantly reduced by the cost effective heat-sink approach (Flip chip or through wafer via)[1,2].

In this paper, in order to understand and control the self heating effect, GaN HFET with flip chip and through wafer via (TWV) structures were simulated, and device characteristics were compared using the ATLAS 2D device simulator.

Flip Chip Structure Simulation
For HFETs, the GaN–AlGaN epitaxial layers have been grown on either sapphire or SiC substrates. Although sapphire has the advantage of lower cost and availability in larger wafer sizes, its poor thermal conductivity (0.3 W/cm-K) limits the achievable powers due to severe self-heating. The self heating effect can be significantly reduced by flip-chip mounting the devices onto highly conducting substrates such as AlN (1.8 W/cm-K)[1].

Figure 1 shows the typical GaN HFET flip chip structure; the physical devices simulated are Al$_{0.25}$Ga$_{0.75}$N-GaN HFET on a sapphire substrate. The structure consists of an AlN layer as a heat sink, a 2.7nm undoped AlGaN layer, and 2 GaN layers which includes 20nm doped 1e15 GaN and 1um undoped GaN.

The space of the Source-Gate and Drain-Gate are 2.0um and 2.0um respectively, and gate length is 1.0um.

The spontaneous polarization of the interface of AlGaN/GaN is taken into account in ATLAS. The 2DEG was calibrated to 9e12cm$^{-2}$ using the polarization scaling factor.

The drift-diffusion transport model is used for this simulation with the Farahmand Modified Caughey Thomas (FMCT) mobility for low field, and the high field dependent mobility model is based on fitted Monte Carlo data for bulk nitride.[3]

The self-heating is a local increase of crystal temperature due to dissipated Joule electric power, this effect can significant can reduce the electron mobility and degrade device performance.

Figure 2 shows the current-voltage (Id-Vg) and transconductance (Gm) with thermodynamics model. Figure 3 shows the IdVd characteristics versus gate bias. Figure 4 shows the lattice temperature distribution. Figure 5 and 6 show self heating impact on transient performance. Figure 7 shows RF characteristics.
In Figure 2, simulations for the normal structure show significant degradation of transconductance compared to the case of flip chip structure.

In Figure 3, for a normal structure, we can clearly see significant degradation of output characteristics with pronounced negative differential output conductance (NDC) region and with relatively high temperature at the drain-side gate edge due to the self heating effect (Figure 4). Degradation of output characteristics in the case of flip chip is significantly improved.

The NDC depends on the thermal dissipation. The normal structure exhibits stronger NDC compared to flip chip structure, because the Sapphire thermal conductivity is smaller than AlN.

The presence of trapping centers in GaN HFETs has been considered as one of the main cause of gate lag effect [4]. In this paper, self heating impact on gate lag was also simulated.

In gate lag simulation, a turn-on step voltage (≤ 10 ns) is applied to the gate terminal (from $V_{BG} = -6$ to 0 V), maintaining a fixed drain bias of $V_d = 5$V. The drain–current transient versus time is analyzed. In Figure 5, simulation for the normal structure clearly shows significant current collapse compared to flip chip structure. This current collapse can be correlated to temperature effect due to self heating (Figure 6).

In Figure 7, simulations of RF characteristics are presented. Simulations indicate ~50% enhancement in $F_t$ and $F_{max}$ (GU) with a flip chip structure that is in good agreement with transconductance and output simulation data.
TWV Structure Simulation

Figure 8 shows the typical GaN HFET with through wafer via (TWV) structure. The TWV plays four important roles. First, it reduces the source interconnection resistance. Second, the source parasitic inductance is also significantly reduced because of the eliminated source wires and bonding. Third, the TWV relieves the electric field between the drain and gate since the grounded substrate acts as a backside field plate. Fourth, the TWV also acts as a good heat sink to relieve the self heating effect. [2]

The physical devices simulated in this paper are Al$_{0.25}$Ga$_{0.75}$N-GaN HFET on 4H-SiC substrate, and TWV size is 2.4um. The structure consists of a 2.7nm undoped AlGaN layer, and 2 GaN layers, which includes 20nm doped 1e15 GaN and 1um undoped GaN.

The space of the Source-Gate and Drain-Gate are 1.15 um and 2.3um respectively, and gate length is 0.4 um.

Other parameters and models followed flip chip simulation.

In Figure 9, for a normal structure, we can clearly see relatively high temperature of the hot spot and with the degradation of output characteristics (Figure 10). Degradation of output characteristics in the case of through wafer via is improved, and performance can be further improved by TWV size optimization.

In Figure 11, simulations of RF characteristics are presented. Simulations indicate ~40% enhancement in Ft and Fmax (GU) with through wafer via structure.
Conclusion

Understanding the self-heating and the temperature effect in GaN HFET is an important problem because this device is a promising candidate for ultra-high-power microwave systems, power electronics and high temperature applications. In this paper, two-dimensional (2D) electro-thermal simulations for the GaN HFET with heat sink structures are performed by ATLAS.

Reference


