Designing a High-Voltage IGBT Structure with TCAD

Introduction

The Insulated Gate Bipolar Transistor (IGBT), is a power device that combines the high-power characteristics of bipolar transistors with the fast-switching and voltage-drive characteristics of MOSFETs. It is used in a wide variety of applications, ranging from electric vehicles, industrial applications such as general-purpose inverters and switching power supplies, to consumer applications such as air conditioners and washing machines, making it a key device of the modern power electronics. From the viewpoints of lowering the loss and enhancing the efficiency of the application devices to which it is incorporated, the structure of the IGBT is being continuously improved. To illustrate the effectiveness of TCAD simulations in designing a power device structure, high-voltage structures of planar type and trench type, which are typical IGBT cell structure types, were designed using ATLAS 2D device simulator and then compared to each other.

Simulations

The following characteristics are needed for designing an IGBT structure.

1. Breakdown characteristics
2. $I_C-V_C$ characteristics
3. $I_C-V_C$ characteristics
4. Switching characteristics

To compare different types of cell structures like planar and trench, the structures should have a similar breakdown voltage and a similar threshold voltage. In other words, it is necessary to adjust the structures so that they have approximately the same breakdown voltage and threshold voltage. This corresponds to the simulations of above 1. and 2. From the simulation results of 3. and 4., the collector-to-emitter saturation voltage $V_{CE(sat)}$ and the fall time $T_f$ are obtained. The tradeoff between $V_{CE(sat)}$ and $T_f$ reveals a superior IGBT structure.
Simulation Results

1. Breakdown Characteristics
The target breakdown voltage in this design was assumed to be 900V or more. The required resistivity of the drift region, or epitaxial layer, to achieve the target was assumed to be 45Ω · cm. The breakdown characteristics were simulated using the thickness as a parameter. Figure 2 shows the result. It shows that both the planar and trench structures have 900V or more breakdown voltage, which is also approximately the same value. The substrate structure of this simulation (of the trench type) is illustrated in Figure 3. It can be said that it is reasonable that both cell structures have approximately the same breakdown voltage since they share a common substrate structure except for the surface neighborhood.

2. Ic-Vc Characteristics
Both the planar and trench structures were adjusted to have a target threshold voltage (V_th) of about 3.5V at Ic=1mA, and Ic-Vc characteristics were simulated. It was assumed that V_CE is 10V, and a base surface concentration was used as a parameter for adjusting the threshold voltage. Figure 4 shows the result. The waveforms show that, for both structures, the threshold voltage is adjusted to the targeted value, which is also approximately the same value. The structures are determined only after the conditions for the threshold voltage and breakdown voltage are both met. Otherwise, the simulations of 1. and 2. will be repeated until the conditions are satisfied.

3. Ic-Vce Characteristics
To calculate the saturation voltage of the planar and trench structures, the Ic-Vce characteristics were simulated at V_GE=15V. Figure 5 shows the result. The waveforms show that the trench structure has a lower saturation voltage. For example, the saturation voltage at Ic=10A is 3.15V for the planar structure and 2.35V for the trench structure.
4. Switching Characteristics

To calculate the fall time, a mixed-mode simulation of the switching characteristics was performed. The measurement circuit is shown in Figure 6. The fall time at peak current $I_{CP}=2.5\, \text{A}$ was measured under the major measurement conditions of $V_{CE}=300\, \text{V}$, $L=1.5\, \text{mH}$, and the device temperature of $125\, ^\circ\text{C}$. A compact model was used for $D_i$. Figure 7 shows the switching waveforms of the collector current obtained by the simulation. The fall time, defined as the time difference (the time at $I_{CP} \times 0.1$ minus the time at $I_{CP} \times 0.9$), was 510ns for the planar structure and 470ns for the trench structure, which are relatively close. Figure 8 shows the hole density distribution inside the device corresponding to points indicated by [A], [B], and [C] in Figure 7 for the trench cell structure. It shows that the number of holes decreases with time and as the collector current decreases, indicating a very close relationship between the hole density and tail current in the buffer layer.

5. Performance Comparison

Figure 9 shows the correlation of the tradeoff between the fall time and saturation voltage obtained by simulations 3. and 4., where the lifetimes are $6\times 10^{-7}$s, $1\times 10^{-6}$s, and $2\times 10^{-6}$s. The relationships similar to those of the actual devices were reproduced; the shorter the fall time the higher the saturation voltage, and the longer the fall time the lower the saturation voltage.

Conclusion

From the performance comparison about, it can be concluded that the trench type is the superior cell structure for the IGBT. The above simulation results from ATLAS proved that TCAD is highly effective for designing an IGBT structure. In this article, cell structures with different gate structures, planar and trench, were compared in terms of the design and performance, but any cell structures with different substrate structures, such as punch-through and non-punch-through types, can be compared in a similar manner.
Investigation of the SiGe Waveguide Photodiodes Using FDTD Method for High Speed Optical Communication

Introduction
Silicon as a photonic medium has unique advantages in telecommunication systems. It is transparent in the range of optical telecommunications wavelength (1.3 and 1.55 um) and has a high index of refraction. In addition, mature Si integrated circuit CMOS technology enables the implementation of dense silicon-based OEICs[1]. The development of SiGe photodetectors, and especially the first demonstration of high performance SiGe Avalanche photodiode(APD)[2], has drawn more attention to high speed SiGe APDs development for low cost optical communication.

In this paper, we present two high performance SiGe Waveguide PhotoDiodes[3], for high-speed applications. Both the waveguides and the photodiodes were simulated self-consistently using the vector helmholtz equation for mode calculation and Finite Difference Time Domain FDTD for light propagation analysis.

Device Structure and Models
3D FDTD is available in ATLAS but simulation time is quite significant because the mesh space should be smaller than at least, 1/5 times the wavelength along x, y and z directions. In this article, we consider x-y plane and optical mode coupling using the vector Helmholtz equation, and the y-z plane was considered using the two dimensional FDTD method.

Device Structure and Mode Analysis
Two types of waveguide photodiodes are considered for the light wave coupling. The butt-coupled and evanescent-coupled types shown in Figure 1 on SOI wafer. The evanescent-coupled device has a Ge absorber layer sitting on the top of a Si waveguide, while the butt-coupled device has the Ge absorber layer directly in contact with the Si waveguide output facet.

The Si waveguide thickness is 250nm the width is 450nm the Germanium thickness is 500nm and the length is 10, 30, 50 and 80 um to get the responsivity at 1.55um. These waveguides exhibit single-mode operation for both TE and TM-like modes and the calculated optical mode overlapped into the 2 dimensional structure, which is shown in Figure 2. [4]

Figure 1. Schematic structure of waveguide PDs of (a) Butt-coupled type (b) Evanescent-coupled type.

Figure 2 shows the optical fundamental mode on the waveguide of the x-y plane. The figure at the left (a) shows only the Si waveguide with 450nm width and 250nm thickness. The second figure (b) shows silicon on top of silicon waveguide. The last one (c) shows germanium on top of silicon waveguide. The butt-coupled modes combine with (b) and (c) and the evanescent-coupled modes combine with (a) and (c).

Figure 3 shows normalized optical field along the center of the 3 different structures shown in Figure 2. These field distributions show the mode-coupling between butt-coupled and evanescent-coupled waveguides.
Finite-Difference Time-Domain Method

The FDTD is a direct discretization of Maxwell's differential equations, where the differentials are replaced by finite differences. A well-known, efficient implementation is based on Yee's mesh, where the electric and magnetic field components are evaluated at different grids having the same pitch, but which have been shifted over half a grid spacing, both in space and in time. This is illustrated in the 2-dimensional case for TE waves (electric field in the plane of calculation) in Figure 4. The half step sizes have been introduced for obtaining accurate approximations of the derivatives; the algorithm proceeds with full step size. A very detailed and practical overview of the FDTD method is given in the book by Taflove [5].

Boundary Conditions

In order to obtain a finite-sized calculation, the number of grid points should be finite. At the spatial boundaries of the calculation domain, the electromagnetic field should satisfy conditions such that the space outside this domain is modeled in a desired way, e.g. a non-reflective continuation of the structure inside the calculation window, or free space.

Figure 3. The normalized mode distribution of the Vertical plane of the each center of structures.

Figure 4. Two-dimensional FDTD calculation grid for TE-waves. The E- and H-evaluations are shifted half a step-size in time.

As mentioned previously, the equations are solved in a 2D rectangular domain. You must specify boundary conditions to complete the problem description. FDTD has 3 types of boundary conditions: Perfect Electrical Conductor (PEC) boundaries, Perfectly Matched Layer (PML) boundaries, and source boundaries (plane and point)

The perfectly matched layer boundary is used to absorb outgoing light. This is useful when we want to simulate an unbounded domain. In other words, we try to absorb (rather than reflect) all outward bound waves. There are several main concepts for PMLs that you should know.

- PMLs are not really boundary conditions in the conventional sense. These boundary conditions have a thickness associated with them and are included in the mesh. We hope to select the absorption coefficient of the layer to allow absorption of the outgoing light to a specified minimum.
- A PMLs is terminated by a PEC. Thus, all light passing through the PML, after accounting for absorption, is reflected back into the simulation domain after making two trips through the PML.

Figure 5. 2D FDTD simulated Ex profiles for TE mode of (a) Butt-coupled waveguide and (b) Evanescent-coupled waveguide.
Simulation Results

Finite-different time-domain (FDTD) method was used to calculate the resonance modes of the coupling between the silicon waveguide and SiGe photodiode.[6]

a. Optical Characteristics

Figure 5 shows the cross-section of the mode field patterns obtained by the incidence of the guided modes at the 1.55μm wavelength.

The figure (a) is the butt-coupled type waveguide and (b) is the evanescent-coupled type waveguide. In Si and Ge media, the absorption loss is dependent to the wavelength.

The Silicon shows low absorption coefficient between 1.30μm and 1.55μm whereas germanium absorption coefficient is higher and wavelength dependent. So illuminating the structure with 1.30μm wavelength will give different results as shown in Figure 7.

b. Electrical Characteristics

The responsivity at 1.55μm is shown in Figure 8 for the butt-coupled and evanescent-coupled Photodiodes with SiGe waveguide lengths of 10 to 80μm. Here, the optical transmission loss and the optical coupling loss between lens fiber and the Si waveguide was ignored.

Conclusion

An electro-optic SOI high-index-contrast waveguide has been investigated using the 2D FDTD method and Vector Helmholtz equation for the mode analysis. Both optical and electrical properties of two types of germanium based waveguide photodiodes were investigated. FDTD gives more accurate results than ray-tracing because the ray-tracing method can not calculate properly the beam propagation along the coupled waveguides.

Reference

Simulating the Hysteresis effects of Si/SiO₂ Interface Traps

Introduction

The trap states at the interface of Silicon with Silicon Dioxide are usually divided conceptually into interface states and fixed oxide charges [1]. These trap states can cause the degradation of the performance of devices such as MOSFETs, when they are stressed into a regime where hot carriers are significant. This degradation is usually permanent and occurs for stress times of the order of 10³ seconds [2]. This phenomenon is well studied, and ATLAS has a degradation model for simulating these effects [3].

If a MOSFET is stressed so as to avoid significant hot carrier current, the threshold voltage \( V_t \) can show hysteresis effects on the sub-second time scale [4]. This can affect the settling time of circuits containing MOSFETs. It is proposed in [4] that the mechanism for the hysteresis is tunnelling of electrons directly from the channel into the fixed oxide traps, as well as indirectly, via the interface states. The experimentally observed dependence of hysteresis on measurement time is apparently predicted by the model of Heiman et al [5]. This model is implemented in ATLAS and can be used to simulate hysteresis effects due to oxide trapping. In the HEIMAN model, the values of SIGN and SIGP are assumed to depend on their distance into the insulator, \( d \), as

\[
SIGN(d) = SIGN e^{-\kappa d} \\
SIGP(d) = SIGP e^{-\kappa d}
\]

where

\[
\kappa_e = \frac{2m_e(E_c - E_f)}{\hbar^2}
\]

\[
\kappa_h = \frac{2m_p(E_v - E_f)}{\hbar^2}
\]

The tunnelling to the trap states from the conduction band edge in the channel \( E_c \) is modelled by the term with the evanescent wavevector \( \kappa_e \) for electrons. Tunnelling from the valence band edge \( E_v \) to the trap \( E_{tA} \) is modeled by the evanescent wavevector, \( \kappa_h \) for holes. The trap spatial density is assumed to be uniform up to a certain depth, and zero above that, and the traps are assumed to be monoenergetic. The capture cross-sections fall off exponentially with distance, and thus to significantly change the occupation state of a trap at depth \( d \) requires a simulation time depending exponentially on \( d \). This dependence of the capture-cross sections on depth leads to hysteresis effects on much longer timescales than can be accounted for by the surface states. Differences between \( \kappa_e \) and \( \kappa_h \) also increase differences between charging and discharge rates.

Model for Hysteresis Behavior of Traps

The equation for the transient behavior of acceptor-like interface traps is:

\[
\frac{dF_{tA}}{dt} = v_n SIGN \left[ n(1 - F_{tA}) - DEGEN.FAC F_{tA} \eta_e \exp\left( \frac{E_{tA} - E_c}{kT} \right) \right] - v_p SIGP \left[ pF_{tA} - \eta_h \exp\left( \frac{E_v - E_{tA}}{kT} \right) \right]
\]

where \( F_{tA} \) is the occupation probability, \( v_n \) and \( v_p \) are the thermal velocities for electrons and holes respectively and \( n \) and \( p \) are the electron and hole concentrations respectively. DEGEN.FAC is a degeneracy factor and \( E_c \) and \( E_{tA} \) are the intrinsic and trap levels respectively. The trap cross-sections for capture of electrons and holes are SIGN and SIGP respectively. The acceptor-like traps are electrically neutral when empty, and negatively charged when occupied by an electron. There is an equivalent expression for donor-like traps, although in this case we only consider acceptor-like traps[6].

The four distinct terms on the right hand side of this equation result in four different rates; a charging rate by conduction band electrons, a discharge to the conduction band, a discharge rate due to valence band hole capture, and a charging rate due to emission of holes to the valence band. These rates depend linearly on the cross-sections SIGN and SIGP, and which rate is dominant depends on the carrier surface densities, as well as the parameter values. Asymmetry of charging and discharging rates leads to hysteresis effects of fast interface states, but on a timescale much shorter than that considered here [4]. In order to get experimentally observed behaviour it is necessary to consider the interface states extending spatially into the oxide, with the values of SIGN and SIGP modified by the tunnelling mechanism needed for the carriers in the channel to interact with the buried traps. In the HEIMAN model, the values of SIGN and SIGP are assumed to depend on their distance into the insulator, \( d \), as

\[
SIGN(d) = SIGN e^{-\kappa_e d} \\
SIGP(d) = SIGP e^{-\kappa_h d}
\]

where

\[
\kappa_e = \frac{2m_e(E_c - E_f)}{\hbar^2}
\]

\[
\kappa_h = \frac{2m_p(E_v - E_f)}{\hbar^2}
\]

Examples

The first example is of a MOS Capacitor with acceptor-like interface traps.

It has a 20 nm thick oxide layer and the silicon region is uniformly doped with \( 1 \times 10^{17} \text{ cm}^{-3} \) acceptors. The interface traps are included in the ATLAS input deck with the INTTRAP statement

\[
\text{INTTRAP E.LEVEL=0.6 ACCEPTOR DENSITY}=1.0e12 \ S.I \ DEGEN=4 \ SIGN=1.0e-13 \ SIGP=1.0e-14
\]

which defines interface traps at a density of \( 1 \times 10^{12} \text{ cm}^{-3} \), 0.6 eV below the Silicon Conduction band edge. The capture
cross sections, SIGN and SIGP are also specified in units of cm$^2$. The gate is biased to 2 V in steady-state, which ensures that the traps are initially filled with electrons. The gate bias is ramped to -2 V, and then immediately back to 2 V. It is also possible to simulate a settlement time after the first ramp, but this is not considered here. Without the Heiman model enabled there is no hysteresis, and the gate-substrate capacitance obtained from small-signal analysis at 100 Hz is shown as a function of gate bias in Figure 1a. The capacitance of the MOS-C without interface traps is shown for comparison. The presence of the traps contributes significantly to the Capacitance over the Voltage range where the trap occupation is changing, with a maximum when the Fermi-level coincides with the trap energy. If we now enable the Heiman model, by adding the parameters

```
HEIMAN DEPTH=0.001 HPOINTS=10
```

to the INTRAPS statement, we use the SOLVE statement to carry out the bias ramps with the ramptime set to 0.1 seconds by using the TIMESSPAN parameter.

```
SOLVE VSTEP=-0.05 NAME=GATE VFINAL=-2.0 AC.ANAL FREQ=1.0e2 DIRECT TIMESSPAN=0.1
```

We then observe hysteresis effects. The HEIMAN model spreads the interface trap density over the specified depth, using the number of depth slices specified. In this case the uniform distribution is to a depth of 1nm, with 10 slices of 0.1 nm each. In Figure 1b the average trap occupancy is shown as a function of bias. On the sweep from 2V to -2V (red curve), the average occupancy decreases more slowly than the non-hysteresis case (blue curve). At -2V the deepest traps are not completely emptied and so the average occupancy is still finite. For the first part of the -2V to 2V sweep (green curve) the average occupancy is still decreasing because the Fermi-level is still below the trap level. The average occupancy then increases, lagging the case of no hysteresis because the deeper traps are slower to fill. The effect of hysteresis on the small signal capacitance is shown in Figure 1c. The capacitance is reduced because of the increased lifetimes of the deeper traps, and there is a voltage shift of approximately 0.5 V between the results for the two ramp directions. The surface Voltage also shows hysteresis effects as shown in Figure 1d.

The second example is a PMOSFET with a channel length of 0.25 microns. This is the same structure as in example 2 of the ATLAS Advanced MOSFET examples, but with acceptor-like interface traps placed along the channel part of the interface. The traps have the same parameters as in the above example, except that the density is reduced to $10^{11}$cm$^{-2}$ and

![Figure 1: Results for the MOS-C example.](image-url)
that the traps were assumed to extend a distance of 2 nanometers into the interface. The source-drain bias was set to 0.5 Volts quasistatically and then the gate voltage was ramped to turn on the device. The source-drain bias was kept low in order to avoid the regime where hot electrons are important, and so that the drift-diffusion approximation was valid.

The threshold voltage was defined as the current required to achieve a source-drain current of 10 microamperes per vertical micron. The gate bias was linearly ramped to 3 V in a set time (ramptime), and $V_t$ obtained from the curve of drain current versus gate bias. The device was allowed to settle in the on-state for a long enough time to attain a steady-state. The gate bias was then linearly de-ramped back to zero Volts in the same set time, and $V_t$ obtained from the curve. The sequence of ATLAS SOLVE statements is

```
SOLVE VGATE=0.0 VSTEP=0.1 NAME=GATE
VFINAL=3.0 TIMESPAN=$RAMPTIME
SOLVE PREV
SOLVE VGATE=3.0 VSTEP=-0.1 NAME=GATE
VFINAL=0.0 TIMESPAN=$RAMPTIME
```

The $V_t$ obtained for the ramp, minus the $V_t$ for the deramp, is shown in Figure 2a as a function of ramptime. This hysteresis in the $V_t$ can be explained as follows. The interface traps are initially empty of electrons, but as the gate bias is ramped they fill with electrons and so shift the $V_t$ to a higher value. The charging rate depends linearly on the density of channel electrons as well as the the capture cross-section. The capture cross-section decreases rapidly with depth, and for shorter ramptimes the deeper traps are not filled with electrons. This reduces the interface charge and thus reduces the $V_t$. After the interface charge is allowed to attain its steady state value, the gate bias is deramped. The discharging is mainly by electron emission to the conduction band because the hole density is too small for significant hole capture. The traps do not discharge significantly until the gate bias is below threshold, and so there is no ramptime dependence of $V_t$. This is illustrated in Figure 2b, where we see the average occupancy of the interface trap halfway between the source and drain. The ramptime is 1 millisecond and the quasistatic solution is shown for comparison. The ramp from 0V to 3V on the millisecond timescale shows that the trap occupancy significantly lags the quasistatic case. The deramp from 3V to 0V shows that the trap occupancy is the same for the quasistatic and 1 millisecond cases above $V_t$ (which is around

Continued on page 11 ...
Q How do I convert ISE files into a Silvaco format?

A. Use the DBINTERNAL translate.ise command.

The various forms of this command are

1) TRANSLATE.ISE TONYPLOT
   PLT.FILE=ise.plt
   OUT.FILE=silvaco.log

   This command converts the ISE file “ise.plt” into the
   SILVACO file “silvaco.log”. The resultant “silvaco.log” is
   displayed in TonyPlot.

   This form of the TRANSLATE.ISE command is used to
   convert 1D output files (such as IV curves and S-Parameters
   as a function of frequency).

2) TRANSLATE.ISE TONYPLOT
   GRD.FILE=ise.grd DAT.FILE=ise.dat
   OUT.FILE=silvaco.str

   This command converts the ISE file pair “ise.grd” and
   “ise.dat” into the SILVACO file “silvaco.str”. The resultant
   “silvaco.str” is displayed in TonyPlot.

   This form of the TRANSLATE.ISE command is used to
   convert 2D output files. The “ise.grd” file contains the
   description of a mesh. The “ise.dat” file contains data
   (such as doping, potential, mobility) at the node points.

   If the “ise.dat” file contains only doping information this
   pair of files corresponds to a device description before
   simulation (such as the output from MDraw). The resultant
   “silvaco.str” file could then be used normally in an
   ATLAS simulation, for example

   ```
   go atlas
   mesh infile=silvaco.str
   ```

3) TRANSLATE.ISE DEVEDIT
   BND.FILE=mdraw.bnd CMD.FILE=mdraw.cmd
   OUT.FILE=devedit.in

   This command converts the MDraw file pair “mdraw.
   bnd” and “mdraw.cmd” into the DevEdit input deck
   “devedit.in”. A child DeckBuild is spawned which runs
   the translated input deck.

   If the OUT.FILE is not explicitly mentioned then DBIn-
   ternal will automatically generate one. This will be of
   the form

   ```
   pp<#>_ded.cmd
   ```

   “pp” indicates this is a post-processed file, the <#> is a
   node number (chosen by DBInternal to be 1 bigger than
   the biggest node that currently exists in the directory).
   “ded” indicates the program the file was translated for
   is DevEdit.

4) TRANSLATE.ISE ATLAS
   CMD.FILE=dessis.cmd
   OUT.FILE=atlas.in

   This command converts the Dessis command file “des-
   sis.cmd” into the ATLAS input deck “atlas.in”. A child
   DeckBuild is spawned which runs the translated input
   deck.

   If the OUT.FILE is not explicitly mentioned then DBIn-
   ternal will automatically generate one. This will be of
   the form

   ```
   pp<#>_atl.cmd
   ```

   Identical to the filename generated by TRANSLATE.ISE
   DevEdit except that “ded” is replaced by “atl” (to indicate
   that the file was translated for ATLAS).

   DBInternal understands the standard “plot” variables
   that can occur in the “dessis.cmd” file, e.g

   ```
   plot {
     grid = @grid@
     doping = @doping@
     plot = @dat@
     current = @plot@
     log = @log@
   }
   ```

   Any other variables that are used in the command file,
   for example

   ```
   #if @"@SimType" == "IV"@@
   ```

   must be defined with VARIABLE commands (one vari-
   able per command), e.g

   ```
   variable name=SimType value=IV
   translate.ise atlas cmd.file=dessis.cmd
   out.file=atlas.in
   ```

   In order to properly translate the Dessis input deck
   DBInternal will need to read the device or devices that
   the “dessis.cmd” deck is simulating. Thus the @grid@ and
   @doping@ files should exist when translating “dess-
   is.cmd”.

Hints, Tips and Solutions

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Summary
The general form of this command is

```
go internal
translate.ise <Silvaco product> <ISE files>
[out.file=<filename>] [!execute]
```

The “Silvaco product” is the product that we are translating the files for. Products recognized at the moment are “tonyplot”, “devedit”, and “atlas”.

The “ISE files” are the alien files that we want to convert into a Silvaco format.

The “out.file” is the name of the file we save the translation to.

The “!execute” command stops DBINTERNAL from running the Silvaco product on the translated file. Normally the TRANSLATE.ISE command automatically runs either TonyPlot (to view a translated data file) or DeckBuild (to run a translated command file). If you just want to generate the translated file without doing anything else with it use IEXECUTE on the TRANSLATE.ISE command.

Conclusions
ATLAS is capable of simulating the hysteresis effects of interface traps. The mechanism of the hysteresis is tunnelling to and from traps located inside the oxide. This results in a spread of charging times as well as greater asymmetry between charging and discharging times. These effects differ from hot carrier degradation effects because they are not permanent, and occur on a shorter timescale. The effect on small signal ac parameters can be modelled, and fully transient large signal analysis can also be carried out. For an example MOSFET, the hysteresis in the threshold voltage has been shown to depend on the logarithm of the measurement time over a range. This agrees qualitatively with experimental observations [4].

References
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