Simulating the Effects of Stress/Strain on a 50 nm Silicon FinFET

1. Introduction

In modern semiconductor devices, the effects of physical lattice strain are playing an increasingly important role. One reason for this is that as device dimensions have shrunk, strains due to lattice mismatch or differences in thermal expansion have become more prevalent. Another is that strain has become an important tool in modifying and enhancing the electrical properties of the semiconductor materials [1]. Large strain induced gains in both electron and hole mobilities have been reported [2][3]. In this article, we will show how SILVACO tools can be used to simulate the creation of a 3D FinFET using VICTORY CELL, calculate the internal strains using VICTORY STRESS, and analyze its electrical characteristics using VICTORY DEVICE.

2. VICTORY CELL

VICTORY CELL was used to generate the FinFET structure based on specifications provided in a mask layout file. VICTORY CELL uses fast, robust and accurate geometrical etch/deposition for Manhattan type structures and fast physical isotropic and anisotropic etch for spacer creation etc. This simulator is perfectly suitable for quick simulation of process parameter variation and design of experiments.

![Figure 1. The FinFET structure generated by VICTORY CELL. The Si$_3$N$_4$ layer is shown transparent in order to display the Silicon Fin and Polysilicon Gate underneath.](image)

We used VICTORY CELL to build up a FinFET structure with a 50x50 nm fin, 1µm in length. The fin was deposited on a SiO$_2$ base layer and a 2 nm gate isolation layer separated it from the 50 nm polysilicon gate crossing it at right angles. A 100 nm Si$_3$N$_4$ capping layer was deposited on top of the structure.

We adjusted the mesh spacing to 5 nm in the active region of the device and made it progressively coarser elsewhere. The final structure is shown in Fig 1.

3. VICTORY STRESS

The structure created by VICTORY CELL was imported into VICTORY STRESS, which was used to perform a stress analysis over the whole FinFET device structure. The Si$_3$N$_4$ capping layer (see Fig 1) was set to have uniform hydrostatic tensile stress of 1 GPa. The bottom, left, and right surfaces of the FinFET were constrained at zero displacement. Stress analysis was performed for a fin oriented along <100> direction on the wafer (100) surface, i.e., in this particular work FinFET orientation is (100)/<100>. Fig 2 shows the XX component of the strain tensor in a cut plane along the center of the device.

VICTORY STRESS accounts for all isotropic and anisotropic properties of the materials, boundaries, and initial conditions. The evaluation of mobility enhancement factors along the fin is based on a full 3D piezoresistive model. Stress effects repopulate the electron conduction bands, resulting in the observed change in effective mobilities. The relative mobility enhancement along the fin

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(XX tensor component) is shown in Fig 3. The center of the active region (Fig 3 inset) shows a mobility enhancement of up to 100%.

4. VICTORY DEVICE

The structure, along with the stress/strain and mobility enhancement data, was then loaded into VICTORY DEVICE for electrical simulation and analysis. Source and drain electrodes were defined at either end of the Silicon fin, the Polysilicon region was defined to be the gate, and we put a substrate contact at the bottom of the device. We also set the workfunction of the gate to 4.17 eV.

Aside from the standard silicon models (cvt, consrh, etc), we used the strain dependent mobility enhancement models (nhance and phance) for this simulation. The mobility enhancement models apply the second order mobility enhancement tensor (calculated by VICTORY STRESS, see Fig 3) directly to the low field mobility. This results in directionally dependent (anisotropic) electron and hole mobilities.

To get an idea of the cut off behavior of the device, we first performed a sweep of the gate voltage from 0 to 3 Volts. The results show a significant increase in drain current when strain is considered in the calculation (see Fig 4).

Next, we swept the drain voltage from 0 to 3 Volts for gate voltages of 1, 2 and 3V. Once again the effects of the mobility enhancement due to stress are clearly visible. Note the improvement both in drain currents and onset of saturation.

5. Conclusion

We have shown how SILVACO tools can be used to simulate the creation of a FinFET and analyze its internal stress/strain as well as their effects on the electrical characteristics. A subsequent electrical simulation and analysis showed the effects of stress/strain have resulted in current increases up to 40%, which demonstrates their importance in device simulation.

References


Introduction
Crosstalk is one of the main parameters that critically affect the resolution of detector arrays. It results in a reduction in image clarity, thus degrading system performance. There are two types of crosstalk; optical crosstalk and electrical crosstalk. Optical crosstalk includes the effect of photon refraction, reflection at boundaries, and external and internal scattering in detector arrays. Electrical crosstalk is attributed to carriers that are photogenerated under one detector, diffusing and being collected by another detector in the array.

As the photodiode size and the pitch (distance between photodiodes) of the detector array get smaller, there is a greater probability of crosstalk influencing system performance since the probability of a generated carrier being collected by a neighboring junction increases. In Focal Plane Arrays (FPAs), a number of parameters will affect the amount of crosstalk. These include the photodiode size, pitch of the detector array, InSb buffer layer thickness, and the epilayer thickness.

There are some published works which use mathematical approaches [1-2] or Monte Carlo simulation [3] to study the crosstalk in InSb array. Here, a commercial semiconductor device simulator, ATLAS, will be used to study the crosstalk and also the quantum efficiency of a 5 x 5 InSb detector arrays in the three dimensional domain. The software includes a comprehensive set of physical models such as drift-diffusion equations, heterojunctions, recombination models, light absorption and photogeneration models, etc. that can accurately predict the crosstalk and quantum efficiency of the InSb detector arrays.

In this work, we will study the dependency of the photodiode size, pitch of the detector array, epilayer thickness and InSb buffer layer thickness on the crosstalk, and quantum efficiency of the InSb detector array.

Simulation Structure
Figure 1 shows the simulation structure of the 5 x 5 InSb detector array. The structure consists of InSb photodiodes fabricated on top of the InSb buffer layer. The p+ regions were doped with acceptor concentration of $1 \times 10^{19}$ cm$^{-3}$ and the buffer layer was doped with donor concentration of $1 \times 10^{15}$ cm$^{-3}$. The contacts on these photodiodes are ohmic and they are named as anode 1, anode 2, up to anode 25 in the simulation. For the cathode, it was formed on top of the buffer layer surrounding the photodiodes. In the figure, L is the size of the photodiode, d is the pitch of the array, T1 is the InSb buffer layer thickness, and T2 is the InSb epilayer thickness. These four parameters will be varied to study the crosstalk effect. The InSb material properties used in the simulation are as shown in Table 1.

In Figure 1(a), the center photodiode as indicated in black will be back illuminated by an illumination source. Under illumination, the incident photon will result in the generation of electron-hole pairs. Most of these electron-hole pairs will be “collected” at the center photodiode and contribute to an external current, while some will diffuse and will be “collected” by the nearby photodiodes in the detector array. The crosstalk at each neighboring diode is defined as the current collected at the neighboring diode divided by the current collected at the center diode.
Table 1. InSb material properties.

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobility of Electron (cm² v⁻¹ s⁻¹)</td>
<td>4.77x10⁵</td>
</tr>
<tr>
<td>Mobility of hole (cm² v⁻¹ s⁻¹)</td>
<td>850</td>
</tr>
<tr>
<td>Carrier lifetime (s)</td>
<td>5x10⁻¹⁸</td>
</tr>
<tr>
<td>Permittivity</td>
<td>16.8</td>
</tr>
<tr>
<td>Temperature (K)</td>
<td>77</td>
</tr>
<tr>
<td>Thermal conductivity (watt cm⁻¹ c⁻¹)</td>
<td>0.18</td>
</tr>
<tr>
<td>Radiative recombination coefficient (cm³ s⁻¹)</td>
<td>5x10⁻¹¹</td>
</tr>
<tr>
<td>Electron effective mass (m₀)</td>
<td>0.014 m₀</td>
</tr>
<tr>
<td>Hole effective mass (m₀)</td>
<td>0.43 m₀</td>
</tr>
</tbody>
</table>

In this simulation, a multi-spectral source will be used and the source will be a black-body radiator operating at a temperature of 2000 Kelvin. The spectral power distribution of a black-body radiator can be expressed in terms of wavelength λ (in meters) and temperature T (in Kelvin) as described by Planck’s formula [4] below:

\[
M_e = \frac{c_1}{\lambda^5 \left( e^{\frac{c_2\lambda}{kT}} - 1 \right)} \quad W \cdot m^{-3}
\]

where

\[
c_1 = 2\pi hc^2 \quad W \cdot m^2
\]

\[
c_2 = \frac{hc}{k} \quad m \cdot K
\]

\[
c = 2.99792458 \times 10^8 \text{ m} \cdot \text{s}^{-1} \quad \text{(Velocity of light)}
\]

\[
h = 6.626172 \times 10^{-34} \text{ J} \cdot \text{s} \quad \text{(Planck constant)}
\]

\[
k = 1.380662 \times 10^{-23} \text{ J} \cdot \text{K}^{-1} \quad \text{(Boltzmann constant)}
\]

To define the black-body radiation in the simulation, we computed the spectral power density at 2000 Kelvin for different wavelengths in an external ASCII file. This is a text file that contains a list of pairs defining wavelength and spectral power density. This ASCII file is then specified in the “POWER.FILE” option in the BEAM statement.

Simulation Results and Discussion

Figure 2 shows the simulated current density contour plot of the 5 x 5 InSb photodiodes array back illuminated by a multi-spectral black-body radiator (2000 Kelvin) at the center photodiode. Each photodiode size is 40 x 40 µm² and the pitch of the array is 20µm. The thickness of the InSb buffer layer is 10µm and the InSb epilayer is 5µm.

From the contour plot, high current density is observed at the center photodiode and lower current density is found at the nearest neighboring photodiodes surrounding the center photodiode. Very low current density is observed at the second nearest neighboring photodiodes.

This shows that the nearest neighboring photodiodes act as guards, preventing carriers from diffusing past them to the second nearest neighboring photodiodes. To observe the crosstalk effect more clearly, Figure 3 shows the quantitative analysis of the 5 x 5 InSb photodiodes array. Here, the current collected by each photodiode is indicated as shown in Figure 3.

From Figure 3, it can be seen that a substantial current of 2.0mA is collected at the center photodiode from the illumination. The current collected at the nearest neighboring photodiodes (vertically and horizontally) is approximately 66mA, and current collected at the diagonally nearest neighboring photodiodes is about 7.5mA. Since crosstalk is defined as the ratio of collected current by the photodiode to the collected current by the center photodiode, this translates the crosstalk at nearest vertically and horizontally photodiodes to be 3.3% and 0.375% at nearest diagonal photodiodes. Outside the 3 x 3 nearest neighboring photodiodes, the crosstalk drops off to nearly zero.
Thus, the total crosstalk for the 5 x 5 array (summation of all crosstalk values at the neighboring photodiodes) is 15%. In addition, the simulated available photocurrent is 2.7mA and the quantum efficiency (defined as the total current collected at all photodiodes divide by the available photocurrent) is 83%.

Next we will investigate the effect of photodiode size, pitch of the array, InSb buffer layer thickness, and InSb epilayer thickness on the total crosstalk and quantum efficiency of the InSb array.

Figure 4 shows the effect of the photodiode size on the total crosstalk and quantum efficiency. In this simulation, the pitch of the array is 20μm, thickness of the InSb buffer layer is 10μm and InSb epilayer thickness is 5µm. Figure 4 shows that total crosstalk reduces with the increase in the photodiode sizes, and quantum efficiency increases with the increase of the photodiode sizes. For photodiode size of 20μm, the total crosstalk of the InSb array is 34%. When the photodiode size increases to 55µm, the total crosstalk reduces to 9%. The quantum efficiency increases from 69% to 84% when the photodiode size increases from 20µm to 55µm. This is because increasing the photodiode dimensions increases the junction sizes as well. This allows more excited charge carriers to be collected at the junction while reducing the number of carriers crossing to neighboring photodiodes. Therefore, the total crosstalk effect is reduced and the quantum efficiency of the InSb array is increased. This shows that photodiode size has a significant impact on the crosstalk and quantum efficiency of the InSb array, and should be considered when optimizing the dimensions of the photodiodes.

Figure 5 shows the effect of the pitch on the total crosstalk and quantum efficiency of the InSb array. In this simulation, the pitch varies between 10μm and 80µm with the photodiode size, InSb thickness, and InSb epilayer thickness is kept constant at 40μm, 10μm and 5µm respectively.

From the graph, the total crosstalk is 27% when the pitch is 10μm, and reduces to less than 2% for a pitch value greater than 60μm. The same trend is observed in the quantum efficiency curve, which starts from 84% (pitch = 10μm) and is reduced to 72% (pitch = 60μm). Above pitch value of 60μm, any increase in the pitch of the InSb array will have a negligible effect on both the total crosstalk and quantum efficiency.

The InSb buffer layer thickness may vary over the array, or from array to array, due to a non-uniform thinning process. It is also important to study the effect of the InSb buffer thickness on the crosstalk and quantum efficiency of the InSb array. Figure 6 shows the simulation of the InSb array with buffer thickness varying from 7μm to 14μm. Here, the photodiode size is 40μm, pitch is 20μm and InSb epilayer thickness is 5µm. The graph shows that both crosstalk and quantum efficiency are linearly proportional to the thickness of InSb buffer layer. As the buffer thickness increases from 7μm to 14μm, the quantum efficiency decreases from 87% to 71%, due to in-
increased recombination in the bulk and the total crosstalk increases from 10% to 24%. Therefore, a non-uniformity thickness of ±1 µm results in a non-uniformity response of about ±2%.

Finally, the effect of the InSb epilayer thickness on the total crosstalk and quantum efficiency is shown in Figure 7. It shows the same linear response as in Figure 6. The quantum efficiency decreases from 83% to 75% and total crosstalk increases from 14% to 19% when epilayer thickness increases from 4 µm to 7 µm. Therefore, a ±0.5 µm difference in epilayer thickness will result in ±3% change in quantum efficiency and ±0.8% change in total crosstalk.

Conclusion

We have presented the use of a 3D semiconductor device simulator, ATLAS, to simulate the quantum efficiency and total crosstalk of a back-illuminated InSb detector array. Results from the simulation showed that the quantum efficiency and crosstalk have a strong dependency on the array dimensions such as the photodiode size, pitch of the array, InSb epilayer and buffer layer thickness. Thus, it is important to take care of these parameters when designing and optimizing the resolution of detectors arrays.

REFERENCES


Abstract

SOI MOSFETs can exhibit a kink in their $I_d/V_d$ curves, which is caused by impact ionization, floating potentials, and other effects. One way of suppressing this kink effect is to supply the device with a body contact. With a body contact, however, the geometry of the device becomes fully three dimensional. In this paper, we show how an SOI MOSFET with a body contact can be simulated in VICTORY DEVICE. 3D visualizations from the VICTORY DEVICE results illustrate how the body contact acts to suppress the kink effect.

Motivation

Silicon-on-Insulator (SOI) technology continues to see application in state-of-the-art CMOS designs, because of the performance advantages it offers compared to devices on a silicon substrate. These advantages include higher switching speed, lower power consumption, smaller size, resistance to latch-up, reduced temperature sensitivity and lower substrate noise. On the other hand, SOI devices may experience history effects, greater self heating, and the possibility of improper circuit operation due to parasitic bipolar currents [1,2].

One complication in SOI MOS structures is that the body of the device floats electrically, being insulated from the substrate by the buried oxide layer. If the device is biased in the saturation region and the drain-to-source bias is larger than the bandgap of silicon, impact ionization near the drain end of the gate contact results in the generation of a large number of electron/hole pairs. The excess holes first migrate towards the buried oxide below the gate, raising the potential of that region. From there, they migrate towards the source and recombine with source electrons. Meanwhile, the excess electrons from the impact ionization migrate to the drain, increasing the drain current. The combination of these effects leads to an anomalous increase in the drain current, known as the kink effect because it produces a kink in the $I_d/V_d$ curve [2,3].

Since the kink effect is often undesirable, various techniques have been developed to suppress it [3,4,5]. One of these is to supply the device with a body contact, which provides a path for holes to leave the device without going through the source. With a body contact, the geometry of an SOI MOSFET becomes fundamentally three-dimensional, since the body contact does not lie in the vertical plane defined by the source, gate, and drain. Consequently, an SOI MOSFET with a body contact can only be simulated properly by a 3D device simulator.

In this paper, we will show how an SOI NMOSFET with a body contact can be simulated using Silvaco’s VICTORY DEVICE application.

Methodology

DevEdit was used to create structures representing SOI NMOSFETs with and without body contacts. Overall, both devices were 3 µm wide by 4 µm long. The silicon body was 200 nm thick, on top of a buried oxide layer 400 nm thick. Boron doping at a concentration of $2.0\times10^{17}$ was applied to the body as a whole, while the wells below the source and drain were doped with arsenic at a concentration of $1.0\times10^{20}$. The source and drain contacts were each 50 nm thick and 400 nm wide, and were modeled as aluminum. Gate oxide thickness was 17 nm, while the gate itself was 33 nm thick. Both gate and gate oxide were 1 µm wide. In DevEdit, the gate contact material was specified as aluminum, but in VICTORY DEVICE it was simulated using the workfunction and thermal properties corresponding to n-type polysilicon.
In the device with the body contact, the source and drain contacts were each 1 µm long, but the gate contact was 2.5 µm long and the gate oxide was 3.5 µm long. Located at the end of the gate oxide, the body contact was 50 nm thick, 1 µm wide, and 500 nm long. In the device without the body contact, the gate oxide and source, drain, and gate contacts all extended the full 4 µm length of the device. The resulting structures are shown in Figures 1 and 2.

These two structures were then simulated in VICTORY DEVICE. Carrier mobility was treated using the Lombardi CVT model: a general purpose mobility model including concentration, temperature, and electrical field dependence. Impact ionization was treated using Selberherr’s model [6]. Other physical effects that were modeled include Shockley–Read–Hall recombination, Auger recombination, and bandgap narrowing in the presence of heavy doping.

Two simulations were run for each structure: One simulation with lattice heating, and one without. In each case, the gate bias was raised to 3V, then an I_d/V_d curve was generated by ramping the drain bias from 0.2V to 4V. For the simulations that included lattice heating, the substrate was maintained at a temperature of 300K.

Simulation Results

Figure 3 displays the I_d/V_d curves from the four simulations. As the figure illustrates, the presence of a body contact suppresses the kink effect. Suppression of the kink effect also reduces the effects of lattice heating.

Figures 4 and 5 illustrate the difference in the impact ionization patterns caused by the presence of a body contact. These figures correspond to the conditions when the gate bias, \( V_g = 3V \), and the drain bias, \( V_d = 4V \). The maximum generation rate in both cases is \( 10^{30} \) electron-hole pairs/(cm^3·s).

Figures 6 and 7 show contours of the hole concentration on the surfaces of the silicon and oxide regions. The scale in these figures is logarithmic, so the maximum concentration shown in each case is \( 10^{20} \) holes/cm^3. Again, \( V_g = 3V \), and \( V_d = 4V \). In the device without the body contact, the hole concentration is relatively high throughout the region between and underneath the source and gate contacts. On the other hand, in the device with the body contact, the hole concentration is relatively high only near the body contact and near the buried oxide layer beneath the gate.

Figure 8 shows the recombination rate, for the device without a body contact. Most of the recombination takes place at the edge of the gate contact, where holes created by impact ionization encounter electrons coming from the source. The equivalent figure for the device with the body contact is not shown, because the recombination rate for that device is negligible in comparison.

Figure 9 shows a front view of the hole current vectors, for the device without a body contact. These vectors are all parallel to the plane of the paper. The largest hole currents originate in the impact ionization zone near the right end of the gate contact. From there they first drift towards the buried oxide, then turn horizontal and head towards the source. The hole current diminishes in the recombination zone, below the left edge of the gate.
Figure 6. Hole concentration contours when body contact is absent.

Figure 7. Hole concentration contours when body contact is present.

Figure 8. Recombination rate contours when body contact is absent.

Figure 9. Front view of hole current vectors when body contact is absent.

Figure 10. Top view of hole current vectors when body contact is present.

Conclusion

When a body contact is used to suppress the kink effect in an SOI NMOSFET, quantities including the impact ionization, the hole density, and the hole current vectors all take on a three-dimensional structure. Simulation of such a device in VICTORY DEVICE permits these 3D effects to be accurately accounted for and visualized.

References


