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# Simulating the Effects of Stress/Strain on a 50 nm Silicon FinFET

## 1. Introduction

In modern semiconductor devices, the effects of physical lattice strain are playing an increasingly important role. One reason for this is that as device dimensions have shrunk, strains due to lattice mismatch or differences in thermal expansion have become more prevalent. Another is that strain has become an important tool in modifying and enhancing the electrical properties of the semiconductor materials [1]. Large strain induced gains in both electron and hole mobilities have been reported [2][3]. In this article, we will show how SILVACO tools can be used to simulate the creation of a 3D FinFET using VICTORY CELL, calculate the internal strains using VICTORY STRESS, and analyze its electrical characteristics using VICTORY DEVICE.

## 2. VICTORY CELL

VICTORY CELL was used to generate the FinFET structure based on specifications provided in a mask layout file. VICTORY CELL uses fast, robust and accurate geometrical etch/deposition for Manhattan type structures and fast physical isotropic and anisotropic etch for spacer creation etc. This simulator is perfectly suitable for quick simulation of process parameter variation and design of experiments.

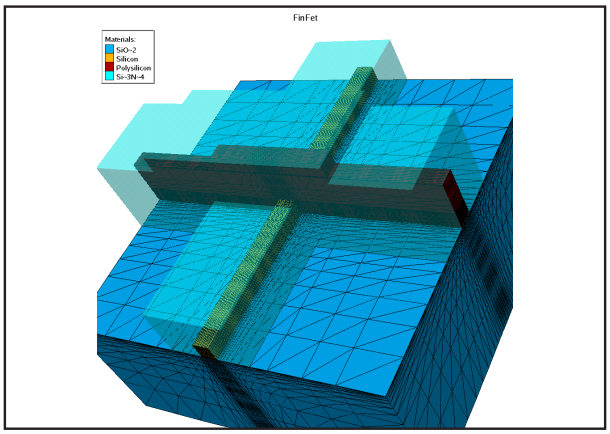


Figure 1. The FinFET structure generated by VICTORY CELL. The $Si_3N_4$ layer is shown transparent in order to display the Silicon Fin and Polysilicon Gate underneath.

We used VICTORY CELL to build up a FinFET structure with a 50x50 nm fin, 1$\mu$m in length. The fin was deposited on a $SiO_2$ base layer and a 2 nm gate isolation layer separated it from the 50 nm polysilicon gate crossing it at right angles. A 100 nm $Si_3N_4$ capping layer was deposited on top of the structure.

We adjusted the mesh spacing to 5 nm in the active region of the device and made it progressively coarser elsewhere. The final structure is shown in Fig 1.

## 3. VICTORY STRESS

The structure created by VICTORY CELL was imported into VICTORY STRESS, which was used to perform a stress analysis over the whole FinFET device structure. The $Si_3N_4$ capping layer (see Fig 1) was set to have uniform hydrostatic tensile stress of 1 GPa. The bottom, left, and right surfaces of the FinFET were constrained at zero displacement. Stress analysis was performed for a fin oriented along <100> direction on the wafer (100) surface, i.e., in this particular work FinFET orientation is (100)/<100>. Fig 2 shows the XX component of the strain tensor in a cut plane along the center of the device.

VICTORY STRESS accounts for all isotropic and anisotropic properties of the materials, boundaries, and initial conditions. The evaluation of mobility enhancement factors along the fin is based on a full 3D piezoresistive model. Stress effects repopulate the electron conduction bands, resulting in the observed change in effective mobilities. The relative mobility enhancement along the fin

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***INSIDE***

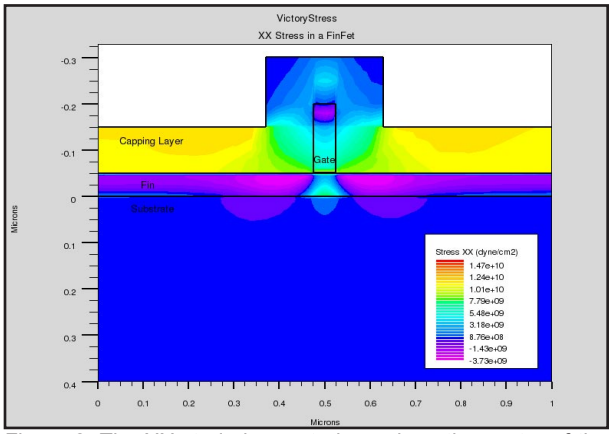


Figure 2. The XX strain in a cut-plane along the center of the device.

(XX tensor component) is shown in Fig 3. The center of the active region (Fig 3 inset) shows a mobility enhancement of up to 100%.

## 4. VICTORY DEVICE

The structure, along with the stress/strain and mobility enhancement data, was then loaded into VICTORY DEVICE for electrical simulation and analysis. Source and drain electrodes were defined at either end of the Silicon fin, the Polysilicon region was defined to be the gate, and we put a substrate contact at the bottom of the device. We also set the workfunction of the gate to 4.17 eV.

Aside from the standard silicon models (cvt, consrh, etc), we used the strain dependent mobility enhancement models (nhance and phance) for this simulation. The mobility enhancement models apply the second order mobility enhancement tensor (calculated by VICTORY STRESS, see Fig 3) directly to the low field mobility. This results in directionally dependent (anisotropic) electron and hole mobilities.

To get an idea of the cut off behavior of the device, we first performed a sweep of the gate voltage from 0 to 3 Volts. The results show a significant increase in drain current when strain is considered in the calculation (see Fig 4).

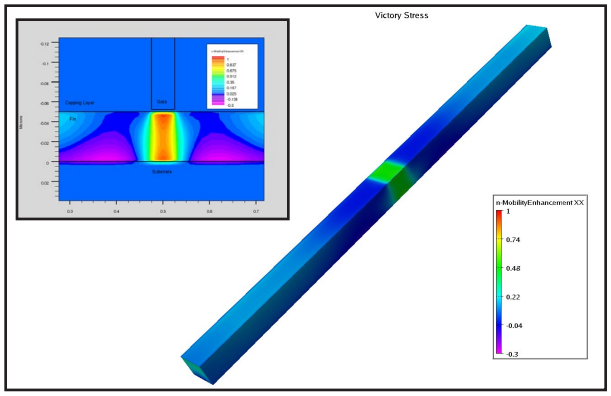


Figure 3. The Mobility Enhancement in the XX direction, along the axis of the silicon fin. Insert: The XX Mobility Enhancement in a cut plane through the active region.

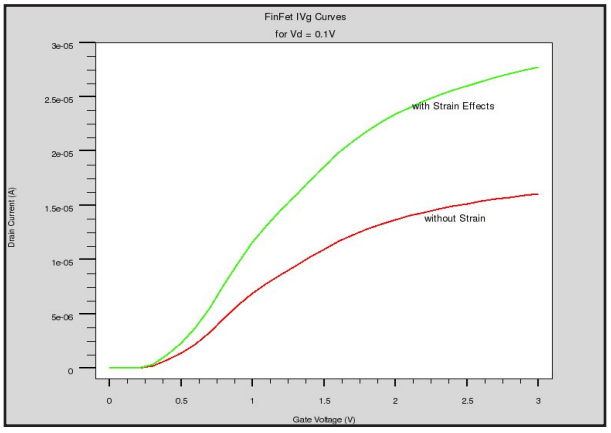


Figure 4. The drain current of the FinFET at Vdrain=0.1V for gate Voltages ranging from 0 to 3V.

Next, we swept the drain voltage from 0 to 3 Volts for gate voltages of 1, 2 and 3V. Once again the effects of the mobility enhancement due to stress are clearly visible. Note the improvement both in drain currents and onset of saturation.

## 5. Conclusion

We have shown how SILVACO tools can be used to simulate the creation of a FinFET and analyze its internal stress/strain as well as their effects on the electrical characteristics. A subsequent electrical simulation and analysis showed the effects of stress/strain have resulted in current increases up to 40%, which demonstrates their importance in device simulation.

### References

[1] S.E. Thompson, et al., "Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap", IEEE Trans. Electron Devices, Vol 53, No 5, May 2006.

[2] S.H. Olsen, et al., "High-Performance nMosfets using a novel Strained Si/SiGe CMOS Architecture", IEEE Trans. Electron Devices, Vol 50, No 9, September 2003.

[3] L. Washington et al., "pMosfet with 200% Mobility Enhancementinduced by multiple Stressors" IEEE Electron Device Letters, Vol 27, No 6, June 2006.

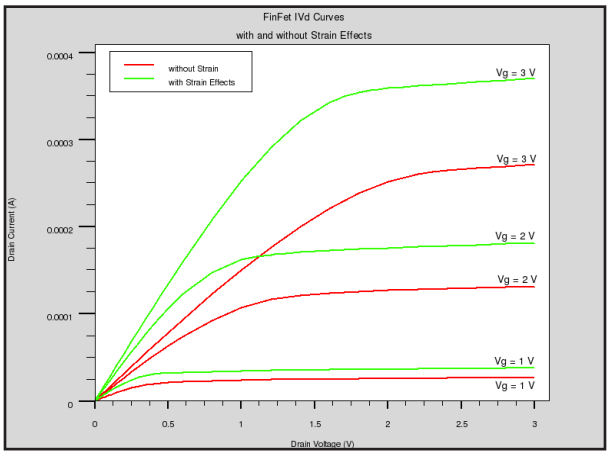


Figure 5. The IV curves for the FinFET simulated with and without strain effects.