Modeling of GaInP/GaAs Dual Junction Solar Cells
Including Tunnel Junction

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Abstract
This paper presents research efforts conducted at the IESUPM in the development of an accurate, physically-based solar cell model using the general-purpose ATLAS device simulator by Silvaco. Unlike solar cell models based on a combination of discrete electrical components, this novel model extracts the electrical characteristics of a solar cell based on virtual fabrication of its physical structure, allowing for direct manipulation of materials, dimensions, and dopings. As single junction solar cells simulation was yet achieved, the next step towards advanced simulations of multi-junction cells (MJC) is the simulation of the tunnel diodes, which interconnect the subcells in a monolithic MJC. The first results simulating a Dual-Junction (DJ) GaInP/GaAs solar cells are shown in this paper including a complete Tunnel Junction (TJ) model and the resonant cavity effect occurring in the bottom cell. Simulation and experimental results were compared in order to test the accuracy of the models employed.

Index Terms: Multi-Junction Solar Cells, Tunnel Junction, Simulation

1. Introduction
LEDs, LASERs and Multi-junction Solar Cells can all employ tunnel junctions to improve performance. Calculating the effects of this junction is tricky, but there are ways to accurately simulate chip characteristics and cost-effectively optimize the structure's design. After the successful simulation of III/V single junction solar cells [1], and the recent development of a nonlocal tunneling model, room was opened to Dual-Junction solar cell modeling. In this paper we present the first results obtained by IESUPM regarding MJC simulation using Silvaco ATLAS. We show that when correctly adjusted, the software allows a good fit between simulation and experimental results for both Tunnel Junction and Dual-Junction solar cell.

2. Tunnel Junction Model
The local band-to-band tunneling models use the electric field value at each node to give a generation rate at that point due to the tunneling. In reality, the tunneling process is nonlocal and it is necessary to take into account the spatial profile of the energy bands. It is also necessary to take into account the spatial separation of the electrons generated in the conduction band from the holes generated in the valence band [2].

A model for this process has been created for ATLAS [3]. It assumes that the tunneling can be modeled as being one dimensional in nature so that it can be calculated using a special rectangular mesh superimposed over and coupled to the ATLAS mesh. This mesh needs to include the junction region of interest and the direction of the band-to-band tunneling, which is generally perpendicular to junction interface.

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In order to explain how the tunneling current is calculated, let us consider an energy band profile along each slice in the tunneling direction when applying a reverse bias across the junction. Figure 1 shows a schematic of this, together with the allowed range of valence band electron energy for which tunneling is permitted.

At moderate doping levels, a tunneling effect can be seen in reverse bias, but if the junction doping levels are high enough, then this energy range may also exist in forward bias and tunneling effect can also be appreciated. If we consider only elastic scattering mechanisms, then electrons from anywhere in the permitted energy range can tunnel from the valence band to the conduction band. ATLAS considers each energy in the allowed range and determines the spatial start and end positions for the tunneling at each energy, $E$, which we label $x_{\text{beg}}$ and $x_{\text{end}}$, respectively, the contribution to tunneling current for an electron in the energy range from $E\Delta E/2$ to $E+\Delta E/2$ (where $\Delta E$ is a small energy increment) is

\[
J(E) = \frac{-qkT}{2n^2\hbar^3} \tau(E) m_e^* \ln \left( \frac{1 + \exp\left(\frac{E_{fl}^* - E}{kT}\right)}{1 + \exp\left(\frac{E_{fr}^* - E}{kT}\right)} \right) \Delta E
\]

where $\tau(E)$ is the tunneling probability, $T$ the temperature, $E_{fl}^*$ and $E_{fr}^*$ are defined on Figure 1 and

\[
\begin{align*}
m_e^* &= m_0 \sqrt{\frac{m_e}{m_h}} |x_{\text{beg}}| \sqrt{|x_{\text{end}}|} \\
m_h^* &= m_0 \sqrt{\frac{m_e}{m_h}} |x_{\text{beg}}| \sqrt{|x_{\text{end}}|}
\end{align*}
\]

In equilibrium, $E_{\text{eq}} = E_{fl}^*$ and the current is zero as expected. This contribution to the tunneling current is calculated and coupled into the mesh at $x_{\text{beg}}$ and $x_{\text{end}}$. ATLAS uses a transmission matrix method to calculate the tunneling probability for direct quantum tunneling simulations through an insulator. In the case of band-to-band tunneling, however, a carefully applied Wenzel-Kramers-Brillouin (WKB) method was found to give equivalent results and is computationally more efficient.

### 3. TJ: comparison with experimental results

In order to calibrate the nonlocal tunnel model, an isolated p"GaAs / n"GaAs tunnel diode was grown by MOVPE. The nominal thicknesses and doping concentrations are listed in Figure 2.

The tunnel diode consists of the tunnel junction itself made by two degenerately doped n" and p" GaAs layers as well as two enclosing barrier layers with the purpose to minimize dopant diffusion [4]. The cap layer and the substrate have been included in the simulation. For the purpose of this paper, a tunnel diode with a sharp uniform doping profile was modeled.

Local and nonlocal Trap Assisted Tunneling (TAT) mechanisms have been included in the models involved in tunneling effects because of their influence on the simulated IV curve.
Figure 3 resumes how the TAT works in the case of tunnel junction. It is indeed divided in two different effects: the local one affecting mainly the peak current and the decreasing slope of the IV curve and the nonlocal one, affecting the current after the valley and increasing its value.

Figure 4 shows the very good fit obtained as a result of the tunnel junction simulation made with Silvaco ATLAS software including the nonlocal and local tunneling model described before. Results have been obtained after adjusting the material parameters affecting the tunneling effect such as the effective mass for both holes and electrons, the trap concentration and the limits of the superimposed mesh. In this case, a high specific contact resistance was put in evidence, reaching actually the value of 0.3e3 mohm.cm² in the case of the tunnel junction presented in figure 4 but reaching sometimes the value of 1.5e2 ohm.cm². We still have to investigate if this very high value is due to the metal/semiconductor contact, to the layer structure, or to how the measurement were done. We also have to note that the real doping profile, which has been measured for others tunnel junction, is important to allow a faster fit between experimental and simulation data.

4. Dual-Junction solar cell simulation

Once we are able to simulate the TJ, the next step is the modeling of a complete Dual-Junction solar cell. We will focus in this paper on the External Quantum Efficiency (EQE), the IV curve at 1 sun and the dark IV curve.

4.1. External Quantum Efficiency

In a GaInP/GaAs dual-junction solar cell, GaAs bottom cell suffers oscillations of its External Quantum Efficiency because of the resonant cavity effect occurring between the top cell BSF and the bottom cell window layer. In this case, using traditional ray-tracing is useless because reflected rays in each layer should be set to a very large number and simulation time increases exponentially with the internal reflection number. The only way to achieve a good accuracy is to use the Characteristic Matrix Method or the Transfer Matrix Method.

Silvaco ATLAS uses the Characteristic Matrix approach that relates total tangential components of the electric and magnetic fields at the multilayer boundaries. The structure of a multilayer completely determines the characteristic matrix of this multilayer. The transfer matrix also contains information about the media on both sides of the multilayer.

<table>
<thead>
<tr>
<th>Name</th>
<th>Material</th>
<th>Thickness</th>
<th>N [cm⁻³]</th>
</tr>
</thead>
<tbody>
<tr>
<td>topfsf</td>
<td>AlInP</td>
<td>50 nm</td>
<td>3.0 x 10¹⁷</td>
</tr>
<tr>
<td>tophem</td>
<td>GaₓIn₁₋ₓP</td>
<td>170 nm</td>
<td>1.8 x 10¹⁸</td>
</tr>
<tr>
<td>topbase</td>
<td>GaₓIn₁₋ₓP</td>
<td>800 nm</td>
<td>1.0 x 10¹⁷</td>
</tr>
<tr>
<td>topbsf</td>
<td>AlGaInP</td>
<td>100 nm</td>
<td>3.0 x 10¹⁷</td>
</tr>
<tr>
<td>phighTD</td>
<td>GaAs</td>
<td>50 nm</td>
<td>5.0 x 10¹⁹</td>
</tr>
<tr>
<td>nhighTD</td>
<td>GaAs</td>
<td>50 nm</td>
<td>3.0 x 10¹⁹</td>
</tr>
<tr>
<td>botfsf</td>
<td>AlₓGa₁₋ₓAs</td>
<td>50 nm</td>
<td>2.0 x 10¹⁸</td>
</tr>
<tr>
<td>botem</td>
<td>GaAs</td>
<td>100 nm</td>
<td>1.0 x 10¹⁰</td>
</tr>
<tr>
<td>botbase</td>
<td>GaAs</td>
<td>3500 nm</td>
<td>2.0 x 10¹⁷</td>
</tr>
<tr>
<td>botbsf</td>
<td>AlₓGa₁₋ₓAs</td>
<td>100 nm</td>
<td>2.0 x 10¹⁸</td>
</tr>
<tr>
<td>subs</td>
<td>GaAs</td>
<td>300 μm</td>
<td>2.0 x 10¹⁸</td>
</tr>
</tbody>
</table>

Table 1. Nominal thicknesses of the Dual-Junction solar cell.
Table 1 describes the layer structure of the simulated Dual-Junction solar cell. The results in Figure 5 show a good agreement with experimental data. The small mismatch is probably due to the differences between nominal thicknesses (introduced in the simulation) and real values which were not measured exactly. We will further make an in depth characterization (Doping concentration and thicknesses) to perfect the fit between experimental and simulated results.

4.2. IV curve at 1 sun
If the EQE simulation agreed well with the measurement and then let us conclude that we can do a good J_{sc} estimation using a simulation software, it was necessary to achieve an IV curve simulation to see how the models can predict the V_{oc}, the Fill Factor and the efficiency of the solar cell.

As demonstrated before by the EQE simulation, we see a very good fit of the J_{sc} using the AM1.5 Low-AOD spectrum (see Figure 6), however, slight disagreements can be observed. Table 2 below resumes the main characteristics of the cell.

The DJ solar cell simulated had no Anti-Reflective Coating layers and was a low/medium solar cell which can explain the low efficiency at 1 Sun and shows that the models are not only able to reproduce high quality solar cells but also lower quality devices. Once again the simulation shows a very good fit with the experimental data on the V_{oc} prediction. However, some differences can be seen on the FF value and on the J_{max}, V_{max} and Efficiency.

<table>
<thead>
<tr>
<th>Experimental results</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>J_{sc} (mA/cm²)</td>
<td>8.4</td>
</tr>
<tr>
<td>V_{oc} (V)</td>
<td>2.12</td>
</tr>
<tr>
<td>J_{max} (mA/cm²)</td>
<td>7.9</td>
</tr>
<tr>
<td>V_{max} (V)</td>
<td>1.9</td>
</tr>
<tr>
<td>FF (%)</td>
<td>84</td>
</tr>
<tr>
<td>η (%)</td>
<td>15</td>
</tr>
</tbody>
</table>

Table 2: Parameters extracted from the experimental and simulated IV curve.

As good results were obtained before modeling single junction solar cells at IESUPM, we suspected the tunneling model used in the DJ solar cell. To be exact we suspected that the model doesn’t behave as it should under illumination, this is why we have simulated a dark IV curve to localize the origin of the differences under illumination.

4.3. Dark IV curve
In contrast with the other DJ solar cells simulations presented in this paper, the dark IV curve only relies on the electrical models as no light is input to the device.

As seen before with the IV curve under illumination, there is a mismatch between experimental and simulation data, especially for middle range voltage. If we compare Figure 6 and Figure 7, we also see the mismatch but the dark IV also shows a shunt resistance effect.

As in this case there is no light input to the device and differences can be observed, light interaction has nothing to do with this. However, viewing the results and the good results obtained before simulating single junction solar cells, we think the mismatch is due the tunnel model once introduced inside a complete dual-junction solar cell structure. More, we think this is due to how the tunneling model manage traps as we saw the kind of curve seen in Figure 7 in some structures with a very high traps concentration, with the difference that in our case the traps concentration cannot explain such a difference.

It is obvious that the revision of the tunnel model will be our priority, despite of the good results, we need it to be totally reliable.

5. Conclusion
It was shown that in contrast to local tunneling models the nonlocal tunneling model reproduces the measured IV curve of a tunnel diode structure in a large voltage range very well, especially in the decisive range of operation when applied to multi-junction solar cells.

Continued on page 7 ...
I. Introduction
GaN-based Hetero-Field Effect Transistors have been investigated in high power and high frequency electronics devices. However, such improved performance is still subject to influence of surface and buffer traps. The role and dynamics of traps and their effect on the GaN HFET have already been investigated [1]. In addition to the formation of the 2DEG, an adequate numerical model of device charge control implies proper modulation of the 2DEG in ATLAS [2].

In this paper, in order to understand and control the self-heating effect, the device was simulated including this effect on a 4H-SiC and a Sapphire substrate, and Id-Vd characteristics were compared using the ATLAS 2D device simulator.

II. Device Structure and Simulation Models
The physical devices simulated in this paper are Al0.25Ga0.85N-GaN HFET on either semi-insulating 4H-SiC or Sapphire substrates. The structure consists of a 0.5um AlN layer and undoped 3um GaN, and 3 Al-GaN layers, which includes 3nm undoped AlGaN and 10nm doped 1e18 n+AlGaN and 10nm undoped AlGaN as shown Figure 1.

The Gate, Source and Drain electrode are on the top surface. The space of the Source-Gate and Drain-Gate are 2.0um and 4.0um respectively.

The strain-induced piezoelectric polarization and the spontaneous polarization of the interface of AlGaN/GaN are taken into account in ATLAS.

The 2DEG was adjusted to 8e12cm$^{-2}$ using the polarization calculation and scaling parameter.

The trap density and cross sections used in in Nitride materials have been chosen according to experimental observations and theoretical calculation [3]. Bulk traps with a trap density of 1.0e17cm$^{-3}$ a cross section of 1.0e-15 cm$^{-2}$ and energy position of 2eV below the conduction band have been used.

The drift-diffusion transport model is used for this simulation with the Farahmand Modified Caughey Thomas (FMCT) mobility for low field[4], and the high field dependent mobility model is based on fitted Monte Carlo data for bulk nitride [5].

III. Self-Heating Effects
Self-heating is a local increase of crystal temperature due to dissipated Joule electric power. Figure 2 shows the current-voltage (Id-Vg) and transconductance (gm) with thermodynamics model due to the substrate materials, 4H-SiC and Sapphire. Figure 3 shows the lattice temperature distribution on the 4H-SiC substrate with a hot spot...
visible at the drain-side gate edge. Table I shows the material parameters of the thermal conductivity of the GaN based HFETs devices.

To estimate the full thermal characteristics, it is important to calibrate the lumped external thermal resistance, $R_{th}$ in K/Wcm$^2$. In this simulation, the substrate layer was chosen as 100um thick which fully considered the vertical thermal spreading of the substrate, the $R_{th}$ was chosen as 1.25e-4. K/Wcm$^2$.

Figure 4 shows the $I_dV_d$ characteristics versus gate bias. Fig 4 (a) is on the 4H-SiC substrate and (b) is on the Sapphire substrate.

Figure 4 and Figure 5 clearly show that the self-heating effects reduce the electron mobility at the drain-side gate edge, thus degrading the device performance and causing the Negative Differential Conductance (NDC) in the $I_dV_d$ curves. This decrease can be correlated to the localized hot spot (Fig. 3).

The NDC depends on the substrate material. The Sapphire substrate exhibit stronger NDC compared to 4H-SiC, because the Sapphire thermal conductivity is smaller.

The self-heating effects can be eliminated or significantly reduced by the conventional heat-sink approach in the packed power devices.

<table>
<thead>
<tr>
<th>GaN</th>
<th>AlGaN</th>
<th>AlN</th>
<th>4H-SiC</th>
<th>Sapphire</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.30</td>
<td>2.86</td>
<td>4.0</td>
<td>4.9</td>
<td>0.33</td>
</tr>
</tbody>
</table>

Table I. Thermal conductivity of materials (Unit : W/cmK).

Figure 5 shows the peak hot spot temperature versus gate and drain bias. Fig 5. (a) shows that the peak temperature can reach 360 K on the 4H-SiC substrate whereas in Fig 5. (b) the peak temperature rises 472 K on the Sapphire substrate.

**IV. Conclusion**

The negative differential conductance due to the self-heating effect was demonstrated for different substrate materials. The effect of lattice heating on GaN HFET IV characteristics was investigated using ATLAS.
We also proved the validity of the model, which coupled with an adequate optical modeling method, allows to reproduce very well the EQE of a DJ solar cell, making the Jsc prediction accurate. Regarding the IV curves, despite the good results obtained on Voc estimation, we detect a problem affecting the values of the FF and the efficiency, we think this problem is due to the tunneling model behavior and a revision of it has to be done.

However, this paper shows that solar cells simulation under a TCAD environment is possible and can be predictive for single junction solar cells as well as for DJ solar cells. Room is open for Multi-Junction solar Cells simulation as we now know the critical part of this structure, the tunnel junction, is well managed.

The future works at the IESUPM will be the enhancement of the simulated structure to triple junction solar cells and the inclusion of real operation conditions as it can strongly change the optimization of the cell and is a logical to improve the efficiency of these cells.

6. Acknowledgements

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7. References

3D Simulation of Ion Milling for Mass Storage Applications

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Introduction
The ion milling process is used extensively in the Hard Disc Drive industry, particularly in the manufacture of thin film magnetic heads. Ion milling is used to pattern many metal and dielectric materials including alloys comprising of Fe, Co and/or Ni transition metals which are commonly found in a thin film magnetic read-write transducers. This paper presents new results for ion milling and redeposition of gold on photoresist patterns at different milling angles and compared with 3D process simulation results.

Ion Milling Process
The basic principle of ion milling involves bombarding a target with energetic ions or neutral atoms accelerated and formed into an ion beam [1, 2]. Material is sputtered from the specimen resulting in thinning of sheet film samples or patterning selectively masked structures. The etch rate is usually highly sensitive to mill angle and is dependant upon the element or alloy being sputtered. Argon or another inert element is typically used for the milling beam. A reactive element can also be introduced into the plasma to adjust the relative selectivity or etch rate of materials being removed.

3D Process Simulation Model
To accurately reproduce such a process in 3D, a novel algorithm with a stable and robust representation of the evolving geometry and an accurate multilayer representation has been implemented in Silvaco VICTORY PROCESS software [3]. This generic 3D process simulator offers objective adaptive meshing to automatically resolve smaller geometries and C-functions to incorporate user defined physical models.

The ion mill yield as a function of beam angle to the surface normal with rotation has been measured for planar substrates at Seagate (Figure 1). Apart from the experimental setup of the initial structure geometry and the beam angle, the data obtained from these basic measurements were the only input needed for the simulation software.

Three important factors are considered in simulating the ion milling of any surface segment:

First the direct etch rate due to the primary flux (ion beam), expressed as a function of impact angles and other parameters is taken into account. Several flux functions have been implemented via the C-Interpreter interface of VICTORY PROCESS. The most comprehen-

![Figure 1. Etch rates as a function of the angle between the ion mill beam and the normal to the surface for various materials considered in this study.](image)

![Figure 2. Au redeposition rate as a function of the angle between the ion mill beam and the normal to the surface of Gold.](image)
The simulation describes a rotating ion beam (equivalent to a rotating substrate) with a divergent ion flux. A number of feature combinations have been implemented to reduce calculation time if, for instance, the beam divergence is neglected, or if the beam is not rotating. The divergent static beam is modelled via a 2D von Mises distribution function while a beam rotation is modelled by removing the $\theta$ dependence from the von Mises function [4].

A secondary flux caused by the redeposition of primary material has been considered (Figure 2).

To predictively account for the angular dependence [5] of the process, the milling efficiency (efficiency as a function of angle of incidence) has been measured for several materials. A table based representation of these functions is part of the C-Interpreter models.

The final local etch rate, is affected by two competing processes of ion milling and re-deposition at each surface point. The effective etch rate is calculated for all surface points using:

$$R_{\text{tot}}(\mathbf{x}) = S(\mathbf{x}, F_{\text{prim}}(\mathbf{x}), F_{\text{redep}}(\mathbf{x}, F_{\text{prim}}(\mathbf{x})))$$

$R_{\text{tot}}$ is the effective local milling rate, $S$ is the surface reaction function, $F_{\text{prim}}$ is the primary flux function (direct ion flux), $F_{\text{redep}}$ is the re-deposition flux coming from other parts of the surface (depends on previously calculated $F_{\text{prim}}$). Note that the total rate $R_{\text{tot}}$ can be negative (when the surface is etched away) or positive (when the flux of re-deposited material exceeds the etch rate).

Comparison to Measurements

Although the results presented in this work are essentially 2D for convenient comparison, the software performs the calculations in 3D. Apart from the milling of resist stripes, the etch effects on the corners of rectangular resist apertures have also been demonstrated.

The results shown in figures 4 and 5 illustrate a good agreement between the observed cross-sectional SEM micrographs of the resist stripes and the simulation. Some features have not been reproduced which could be due to the rounding of the initial structure as well as the divergence of the milling beam. Figure 6 shows ion milling of a resist cone with shadowing and redeposition.
Figure 6 (a) A demonstration conical photoresist shape on a gold substrate. (b) shows the ion milling process for 60 seconds at 30° degrees off the vertical with a rotation (sweep) angle of 45°. (c) Obtaining a cut plane from the 3D structure. (d) a 2D cross section along the 45° rotation plane.

Conclusion

A 3D simulation algorithm has been implemented in VICTORY PROCESS to model ion milling of complex topographies. A reasonable match between measured ion milled resist on gold profiles and simulation results based on basic material parameters have been obtained in this study to demonstrate the predictive capability of the algorithm.

References

3D Simulation of Oxidation Induced Stress Using Cartesian Meshes with Adaptive Refinement

The formation of isolation trenches is one of the key process steps used in power device fabrication. Also the intensive scaling of modern semiconductor devices requires significant stress engineering to enhance carrier mobilities and avoid extended defect formation. Simulation results from complex 3D trench and lateral isolation structures are presented together with the inbuilt oxidation induced mechanical stress in the grown oxides. Fast transition of compressive to tensile stresses has been obtained for concave-convex surfaces with internal hydrostatic pressures ranging from 0.04 to \(-0.04\) N/\(\mu m^2\).

A previous publication [1] introduced a new simulation framework (VICTORY PROCESS, Silvaco’s 3D TCAD tool) based on using Cartesian meshes with adaptive refinement. Unlike unstructured tetrahedral meshes, this approach makes use of the level set method on fixed Cartesian meshes and does not involve re-meshing algorithms that represent a major obstacle in modelling 3D processes. VICTORY PROCESS also uses finite difference numerical schemes to solve the oxidation modelling equations. The implementation of general-type boundary conditions at arbitrary implicit interfaces and the approximation of the equations at the interface between fine and coarse Cartesian meshes are major milestones. Novel, in-house finite-difference schemes were developed and successfully implemented in a commercial simulation framework to overcome these issues. This paper demonstrates the capability and versatility of the Cartesian framework to simulate and analyse oxidation-induced stress.

To quantify the accuracy of the novel numerical schemes, the stress distribution produced by 3D VICTORY PROCESS was compared with results from ATHENA (Silvaco’s 2D TCAD tool based on SUPREM IV) as seen in Figure 1. Both tools used an incompressible viscous model for oxide and nitride to simulate the LOCOS (Local Oxidation of Silicon) process. Figure 1 shows the mean of the diagonal stress components (pressure); \(p = -0.5(S_{xx} + S_{yy})\). Good quantitative agreement between the two simulators has been obtained. As expected, the simulation reveals compressive pressure on the concave oxide/silicon interface and tensile pressure on the convex interface [2].

An important issue in stress engineering is to model the stress behavior when an interface changes its curvature in complex 3D corners. To investigate this question, a 3D LOCOS structure incorporating a 90° bend was simulated (Fig. 2), while maintaining the rheological material model and the process conditions from previous example. A cutplane parallel to the substrate, that captures the changes of the curvature of the silicon/oxide interface (concave - convex - concave) after oxidation, is shown in Fig. 2. Figure 3 shows the extracted 1D pressure contour along the interface. As a result of the curvature changes, the high compressive pressure rapidly decays and reverses to a peak of tensile pressure near the mask corner illustrated by the trough near 0.5μm. Figure 4 shows the oxidation of a vertical trench isolation structure. After 75 minutes

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**Fig. 1.** Distribution of pressure resulted from simulation of LOCOS process (wet oxide, \(T = 1000^\circ C\), time = 30 min). Left panel- ATHENA (2D SUPREM IV), right panel - VICTORY PROCESS (3D).
wet oxidation at 1000°C the data show the accumulation of compressive stress at the bottom Si/SiO2 edges while the tensile stresses are located in the upper Si/ SiO2 edges and a complex mix at the edge corners.

In conclusion, this paper presents true 3D calculations of oxidation induced stress behaviour in complex 3D lateral and vertical trench isolation structures using quantified-state-of-the-art finite difference numerical methods and Cartesian meshes.

References

Fig. 2. 3D LOCOS modeling. Left panel shows 3D isosurfaces of 0.03N/µm² pressure contours and the cutplane extracted from that shows a 2D contour map of the pressure around the oxide/silicon corner.

Fig. 3. Pressure distribution along the oxide/silicon interface. The compressive pressure in concave regions near the structure edges decays to tensile values towards the centre due to compensating curvatures.

Fig. 4. 3D trench oxidation modeling. (a) shows the initial trench corner structure with thin oxide and nitride layer on the surface, (b) shows the structure evolution after 75 minutes of wet oxidation at 1000°C. (c) shows the hydrostatic pressure contours along the outside bottom corner along the Si/SiO2 interface. (d) shows the hydrostatic pressure contours along the inside bottom corner along the Si/SiO2 interface. Once again the fast transition between the tensile and compressive strain can be seen as the complex curvatures meet in the bottom edge corners.
Minimization of Well-Proximity Effect by Means of 2D and 3D Monte Carlo Simulation of Retrograde Well Implantation

Introduction
The formation of deep p- and n-wells using high-energy implantation has become an integral part of CMOS technology process flow. The high energy and high dose implantation into the cleared area of a thick photoresist mask generates retrograde profiles. These profiles have a relatively high peak concentration usually at the depth of approximately 1 micron and a very low surface concentration. From the first glance this process achieves its primary goal to isolate NFETs from PFETs without affecting surface areas where the transistors are formed. Unfortunately for both technology and circuit designers, this relatively simple process step brings about an unwanted Well Proximity Effect (WPE) [1] exhibited by a strong dependence of threshold voltage $V_t$ on transistor location and even orientation within the well.

Origin of WPE
The WPE is caused by an extra non-uniform doping at the surface of the well area by ions scattered within photoresist and emerged from the mask edge at different angles. Figure 1 clearly illustrates this phenomenon. It shows that many of the 2000 boron ion trajectories, simulated by MC Implant Module of the process simulator ATHENA [2], terminate not inside photoresist but at different locations within PWELL. This extra doping near the surface may shift $V_t$ by as much as 100 mV. However, the worst consequence of the WPE is the fact that the value of the shift $V_t$ depends strongly on transistor gate position inside the well. Moreover, it is not easy to quantify and control the $V_t$ pattern within layout. Therefore, even cumbersome compact transistor models attempting to account for the WPE (see, e.g. [3]) appeared to be very impractical.

How to Minimize WPE
Polischchuk, et.al, [4] experimentally showed that it is possible to reduce the WPE by altering mask thickness and shape as well as by introducing an extra screen layer under the mask. The goal of this work is to use Monte Carlo implant simulation for optimizing masking conditions in order to greatly reduce or even eliminate consequences of the WPE in most cases. Figure 2 illustrates the main idea of such optimization. Majority of trajectories of high-energy ions impacted in a single point are confined within a distinctive cone which height and slope are determined by ion type and energy as well as density and composition of the amorphous photoresist material. If the mask is slightly thicker than the height of the imaginary cone and the mask edge slope is slightly larger than the slope of the cone then most of the ions will stop within the mask. The same is valid for ions impacting the mask slope. In the case shown in Figure 2, only 4 out of 2000 simulated trajectories have emerged from the sloped mask edge, which suggests that the WPE could be considerably suppressed.
2D Simulation Results and Analysis

To confirm that using the sloped mask edge could indeed minimize the WPE, full 2D Monte Carlo simulations were performed for both vertical (Figure 3) and sloped (Figure 4) mask edges. To obtain a reasonable accuracy of profiles near the PWELL surface, 15 million 300 keV boron trajectories were simulated using parallel version of the MC Implant [2]. It took approximately 10 hours on a multiple CPUs Linux workstation. Figure 5 compares lateral boron profiles right under the surface. It clearly shows that using mask edge with optimized slope decreases boron surface concentration by at least one order of magnitude. This means that the Vt shift measured near the sloped mask edge will be as small as the Vt shift measured as far as 1µm from a vertical edge. Figure 6 compares the vertical profiles for unmasked implant with profiles obtained for vertical and sloped masks. It clearly shows that in the case of vertical mask edge the surface concentration of ions scattered out of the mask could be as high as that of Vt adjust implant. The sloped mask decreases this extra concentration by the order of magnitude. Figure 7 and Figure 8 illustrate effect of a screen layer. Figure 7 shows that if a 0.1 µ screen photoresist layer is used in attempt to further reduce the WPE then the 400 keV boron implantation should be used to maintain the same depth and retrograde shape of the profile obtained for 300 keV implant. Figure 8 shows that the screen layer by itself could not sufficiently reduce the
WPE, while combination with the sloped mask edge can practically eliminate the WPE.

3D Simulation Results and Analysis

To further analyze 3D corner effects we performed a full 3D Monte Carlo implant simulations in a L-shaped mask with the same mask edge settings as in Figures 3, 4. Figure 9 and 10 show shallow surface boron distributions obtained by simulation of 100 million 300 keV boron trajectories. The simulated distributions demonstrate pronounced corner effects in a L-shaped implant window. These two surface contour plots also unequivocally show that implantation into the mask window with optimally sloped mask edges provides a considerable gain of area.
Q: How can I get a CV curve of a MOSFET? And how can I get the current on all terminals?

A: There are two methods to get the CV curve of MOSFET, Small Signal analysis and Large Signal analysis. From the charge conservation, the sum of charge in the device must meet the charge neutrality relationship given by:

\[ Q_g + Q_d + Q_s + Q_{sub} = 0 \]

so the Capacitance should be

\[ C_{ij} = \frac{dQ_i}{dV_{ij}} \quad i \neq j, i = G, D, S, SUB \]

\[ C_{ij} = -\frac{dQ_i}{dV_{ij}} \quad i = j \]

The small signal analysis method applies AC sinusoidal bias to a DC condition. For example, if the small signal is only applied to gate electrode, then

solve vgate=-2.0 vstep=0.1 vfinal=2.0 ac freq=1e6 aname=gate

The results can be seen in Figure 1.

The large signal analysis method consists of a Transient simulation with DC offset condition. To define a sinusoidal bias offset of 0.01V to the gate bias the following syntax should be used:

```
set vg=-2.0
solve vgate=$vg local
log outf=vg$"vg"-ac.log
solve trans.analysis freq=1e6 vgate=$vg+0.01 tstop=2e-6 tstep=1e-8 cycle=2
log off
```

the resulting currents are shown in Figure 2.

To convert current to capacitance \( i = C \frac{dv}{dt} \), the extract statement was used as follows:

```
evaluate name="Cdg" y.val from curve(time, i."drain"/(2*3.14*1e4)) where x.val=5e-7
evaluate name="Cgg" y.val from curve(time, i."source"/(2*3.14*1e4)) where x.val=5e-7
evaluate name="Csubg" y.val from curve(time, i."substrate"/(2*3.14*1e4)) where x.val=5e-7
evaluate name="Cgsg" y.val from curve(time, i."source"/(2*3.14*1e4)) where x.val=5e-7
```

Figure 1. CV Curve of MOSFET by Small Signal Analysis.

Figure 2. Current of MOSFET by Transient analysis at gate bias -2.0V.
The capacitance is then extracted at $t=5e^{-7}s$ using the following formula:

$$C_{dg} = \frac{idrain \times 1}{(2 \times \pi \times freq) \times (vss)} = \frac{idrain}{(2 \times 3.14 \times 1e6 \times 0.01)}$$

To get the CV curve as in Figure 1, the internal simulator was used as follows:

```
  go internal
  load infile=Large-Cap.in (1)
  sweep param=vg type=linear range="-2.0, 2.0, 41" (2)
  save outfile="largesig-cap.dat"
  quit
```

(1) Large-Cap.in is a file that contains the transient simulation described before.
(2) The sweep command will vary vg from -2.0V to 2V with 41 points.

The results are shown in Figure 3.

```
...continued from page 15

with low near surface concentration. This way, the corresponding area inside the well without critical Vt shift greatly expands toward mask edges.

Conclusion

Comprehensive 2D and 3D simulations of high energy boron ion implantation are used to investigate the origins of the Well Proximity Effect as well as possible methods to avoid negative consequences of this effect. It is shown that WPE could be greatly decreased and practically eliminated if the right combination of process parameters and shape of the resist mask is selected by careful analysis of ion trajectories and results of full 2D/3D implant simulations.

References
