Simulation Standard

Connecting TCAD To Tapeout

A Journal for Process and Device Engineers

TCAD Simulation of a SONOS Device with Silvaco's new FNONOS Model

Introduction

Erasable programmable read-only memory (EPROM) devices include amongst others, floating gate technology and SONOS (Polysilicon-Oxide-Nitride-Silicon) technology. Floating gate technology involves charge being stored in the polysilicon floating gate as a continuous spatial distribution of free carriers in the conduction band. In contrast, SONOS gate stack structures involve charge being stored in spatially isolated deep level traps within the nitride layer. Floating gate technology faces a number of challenges with respect to scaling cell-size and program/erase voltages. The relatively thick tunnel oxide layer present in floating gate devices, whilst providing good data retention, yields problems with operating voltage requirements in that the voltages can exceed voltage limits of scaled CMOS devices. The desire for low power and low voltage memory devices has lead to the proliferation of SONOS devices for high density EPROMs. SONOS is desirable for its low programming voltages, endurance to erase/program cycling and compatibility with CMOS technology. SONOS devices are also able to show a 2-bit/cell storage scheme that utilizes different physical locations to store programmed charge.

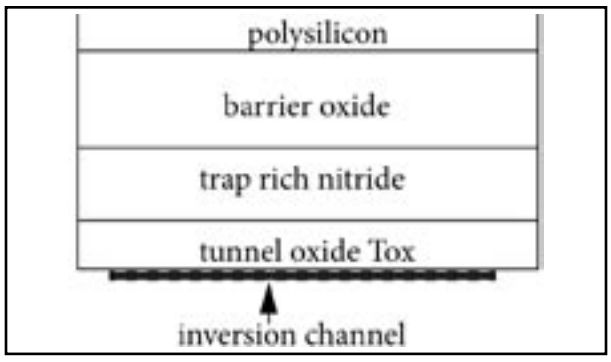

Figure 1. Schematic diagram for gate stack.

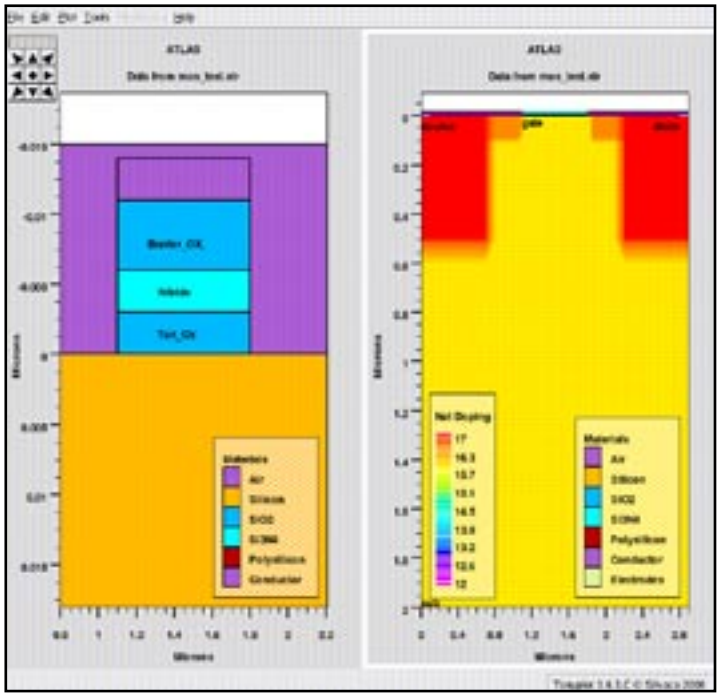

Figure 2. Left: device gate stack, Right: Entire device with doping profile.

Figure 1 shows a typical SONOS gate stack present in a SONOS MOSFET memory cell. The semiconductor (S) channel that forms has a thin layer of oxide (O), typically 2nm, grown onto it. This layer is called the tunnel oxide layer. Following this is a thin layer of silicon nitride

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INSIDE

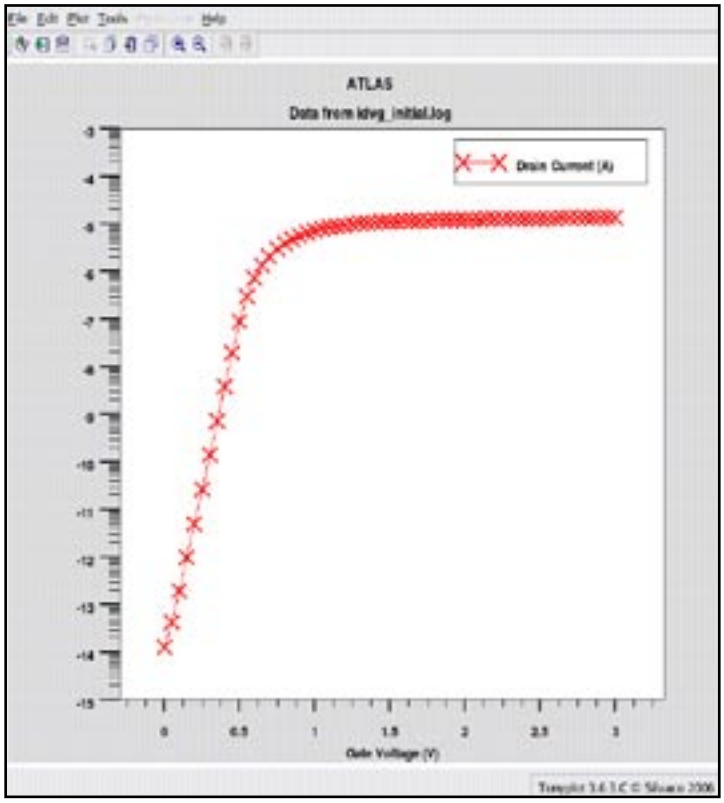


Figure 3. Drain current vs. gate voltage.

J_n is the tunneling current, E is the electric field, DV is the potential drop across the tunnel oxide layer (which is calculated automatically by ***ATLAS***) and `BH.FNONOS` is the barrier height. If `BH.FNONOS` is not specified ***ATLAS*** will also automatically calculate it. The above formulas make use of the WKB theory for the tunneling co-efficient through a trapezoidal barrier.

In the above, if `DV>BH.FNONOS`, factor1 and factor2 are both set to be unity. In this case equation (1) reduces to the expression for Fowler-Nordheim tunneling.

The `FNONOS` model also includes a capture efficiency factor, `ETA.FNONOS`, where the calculated tunneling current given by equation (1) is multiplied by `ETA.FNONOS` before it is added to the nearest floating electrode. The model also allows the efficiency itself to depend on the charge state of the floating electrode. This is enabled by setting the `NT.FNONOS` parameter on the model statement to a positive value. The efficiency is modified by:

$$1.0\text{-}Q_{floating}\ /(q\ \texttt{NT.FNONOS}) \qquad (4)$$

where Qfloating is the floating gate charge density.

(N), typically 4 to 5 nm thick. Following this is a thicker layer of oxide (O), typically 5 to 6nm thick. This layer is called the barrier or capping layer. Finally we have a semiconducting polysilicon (S) gate layer. The nitride layer is made up of trap rich nitride so that is has trapping levels located within it. The nitride-oxide band offset allows charge to be accumulated in the nitride layer.

FNONOS model

Silvaco's ***ATLAS*** device simulator has a new model specifically created to allow the charge-erase behavior of SONOS structures to be simulated. For each point in the channel oxide interface the nearest distance to the nitride layer is calculated. The tunneling current for this point is then calculated as:

$$J_n = \texttt{F.AE}\ \ E^2\ /(factor1\ exp\ (\texttt{-F.BE}\ \ factor2\ /\ \ \texttt{E}) \quad (1)$$

where:

$$factor1 = \left[1\text{-}(\mathbf{1}\texttt{-DV/BH.FNONOS})^{\frac{1}{2}}\right]^2 \qquad (2)$$

and

$$factor2 = \left[1\text{-}(\mathbf{1}\texttt{-DV/BH.FNONOS})^{\frac{3}{2}}\right] \qquad (3)$$

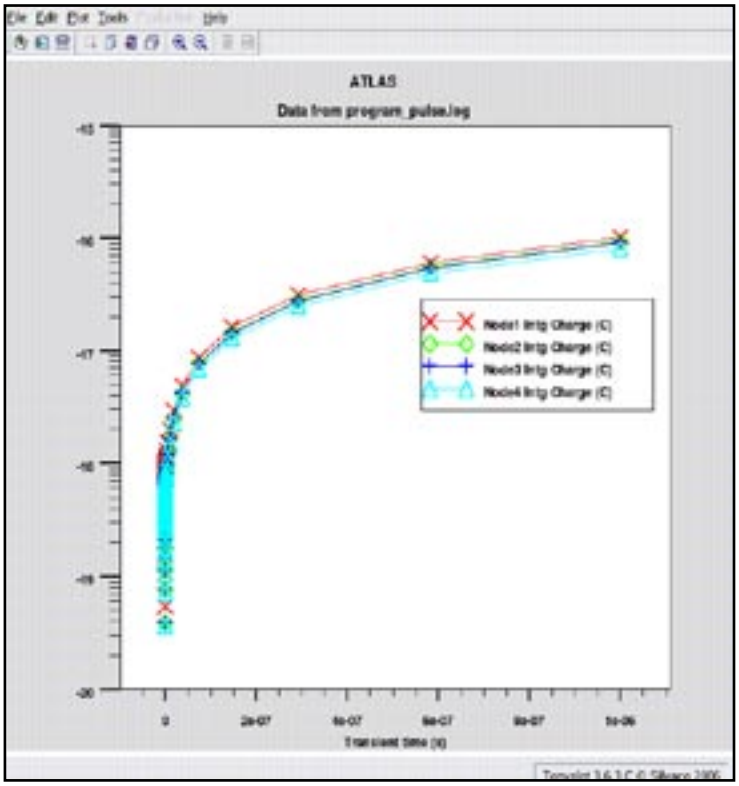


Figure 4. Internal charge for the four floating gates.

Device Simulation

The device is created using Silvaco's device simulator ***ATLAS***. It is also possible however to use Silvaco's process simulator ***ATHENA*** to create the device using a physical process. The device SONOS gate arrangement structure is seen in Figure 2 (left) together with the net doping profile and the entire device structure Figure 2 (right). Currently the FNONOS model requires you to either set the nitride layer as a floating contact or to embed floating contacts in the nitride layer. It is possible to set up a number of floating contacts within the nitride layer, in this way some spatial information about the tunneling current can be obtained. The device in this simulation incorporates several floating contacts in the nitride layer.

Figure 3 shows the IdVg curve for the device under initial conditions, i.e. not programmed or erased. To program the device 12V was applied to the gate and the drain contact was ramped to 8V over 1ns and then held there for 1us. The internal charge for each of the floating nodes in the nitride layer is shown in Figure 4. The IdVg data for the programmed device was then obtained. Finally, to erase the device the gate was set to -10V and the drain was ramped to 8V over 1ns and then held for 1us. Figure 5 shows the IdVg curves for the three different states. The middle curve is for the unprogrammed-unerased state, the right curve is for the programmed state and the left curve is for the erased state. For the program conditions applied, a shift in the Vt of the device is obtained. It is evident in Figure 5 that it is also possible to simulate an overerase where the curve for the erased device is to the left of the middle curve.

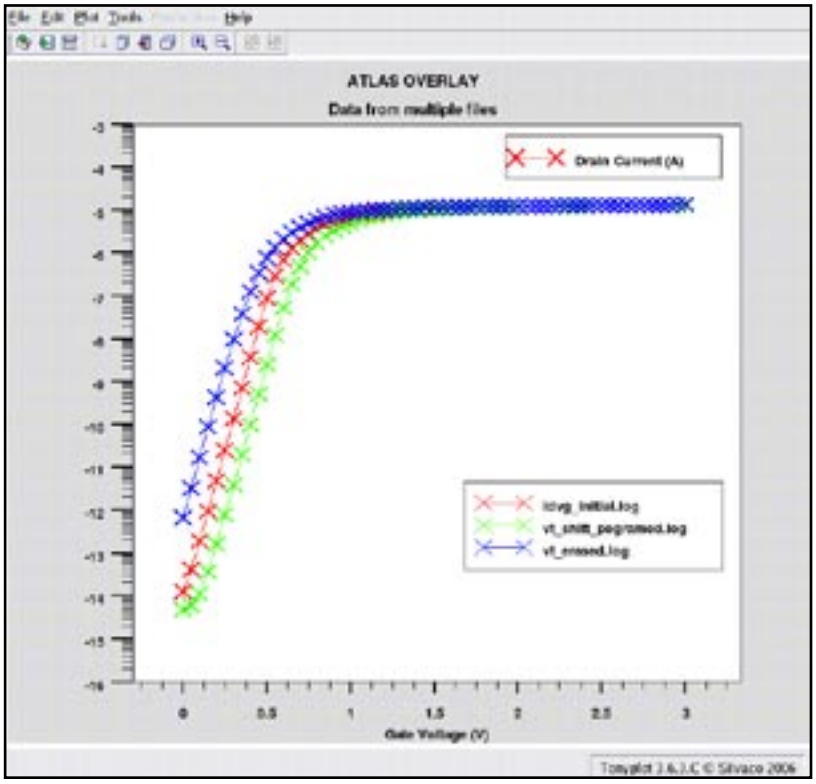


Figure 5. IdVg curves for the unprogrammed, programmed and erased states.

Conclusion

Silvaco's device simulation framework has been used to simulate the program-erase of a SONOS device structure. The device structure was modeled using ***ATLAS*** syntax. In this simulation several floating electrodes were placed throughout the nitride layer in order to obtain information regarding the spatial distribution of trap charge. The phenomena of overerase can also be simulated. The FNOSOS model can be used to accurately tune program/erase conditions for SONOS device structures and hence optimize device structures.

Advanced Quantum Effects Simulation in *ATLAS*

Introduction

The trend toward smaller MOSFET devices with thinner gate oxide and greater doping is resulting in the increased importance of quantum mechanical effects, which are observed as shifts in threshold voltage and gate capacitance. Predicting these quantum effects requires solving the Schrodinger equation. This article presents the Poisson-Schrodinger solver and recent enhancements implemented in ***ATLAS*** from Silvaco.

Schrodinger-Poisson

To model the effects of quantum confinement, ***Quantum*** allows the self-consistent solution of the Schrodinger equation with Poisson's equation. Poisson's equation is solved in two dimensions over the entire device while Schrodinger's equation is solved in one dimensional slices across the device.

These solutions provide calculations of the bound sate energies (Eigen energies), the carrier wave functions (Eigen functions), and carrier concentrations in the presence of quantum mechanical confining potential variations.

Considering ml, mt1 and mt2 the electron longitudinal effective mass and the electron transverse effective masses respectively, the electron density is written as:

$$n(x) = \frac{2k_B T}{\pi\hbar^2} \left\{ \sqrt{m_l m_{t1}} \sum_i |\Psi_{li}(x)|^2 \ln\left[1 + \exp\frac{E_F - E_{li}}{k_B T}\right] + \sqrt{m_l m_{t2}} \sum_i |\Psi_{ti}(x)|^2 \ln\left[1 + \exp\frac{E_F - E_{ti}}{k_B T}\right] + \sqrt{m_{t1} m_{t2}} \sum_i |\Psi_{t2i}(x)|^2 \ln\left[1 + \exp\frac{E_F - E_{t2i}}{k_B T}\right] \right\}$$

where x is the position along a vertical slice (normal to the gate oxide), Ψ_{li}, E_{li} (resp. Ψ_{i}, E_{ti}) are the i-th longitudinal (resp. transverse) eigenvector and eigenvalue, k_B is the Boltzmann constant, T is the temperature, h is the Planck constant and E_F is the Fermi level. For the holes, a similar expression is obtained with the light and heavy holes effective masses.

	2D Poisson 1D Schrodinger	2D Poisson 2D Schrodinger	3D Poisson 2D Schrodinger
Regular Grid	X	X	X
Unstructured Grid	X		
Post Processing	X		
Non-Equilibrius	X	X	X
Strained Silicon	X	X	X
Radiative Models	X		X

Table 1. Schrodinger Poisson Operational Modes

Operational Modes

In ***Quantum***, solutions to the Schrodinger-Poisson system are used in various modes to accommodate various applications. The table above summarizes these modes.

Table 1 shows that ***Quantum*** offers three basic operational modes of solutions to the Schrodinger-Poisson system of equations: one-dimensional Schrodinger "slices" embedded in a two-dimensional Poisson solution mesh, two-dimensional Schrodinger solutions on the same two-dimensional Poisson solution mesh and two-dimensional Schrodinger "plane slices" embedded in a three-dimensional Poisson solution mesh.

For the rectangular grid approach, the grid points used for the Schrodinger solution exactly coincide with the grid points used in the Poisson solution. These solutions have the best self-consistency since they involve no interpolation between the Schrodinger and Poisson solution grids. Conversely, the unstructured grid approach requires a separate grid definition for the Schrodinger solution from the Poisson grid. This requires interpolation between the grids, but offers the advantage of allowing self-consistent S-P solutions for unstructured meshes such as are generated by the process simulator ***ATHENA*** or the interactive general purpose structure creation tool ***DevEdit***.

The post-processing approach does not solve Schrodinger's and Poisson's equation self-consistently. Instead Poisson's equation is solved self-consistently with the electron and hole continuity equations in the standard drift-diffusion approach. The Schrodinger solutions are then obtained using the classical Poisson solutions. This has the advantages of providing fast solutions and solutions can be taken far from zero bias (i.e. with currents flowing).

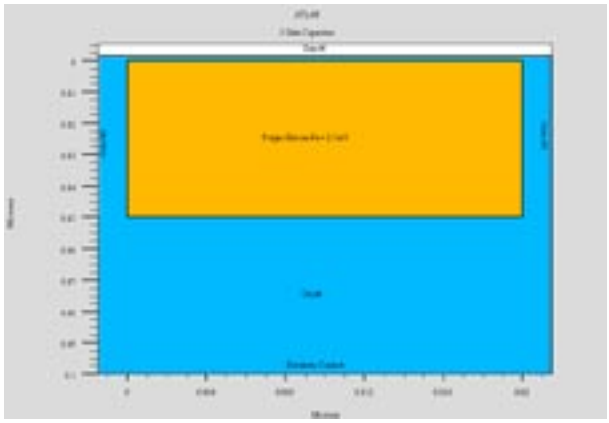


Figure 1. 3 gate capacitor.

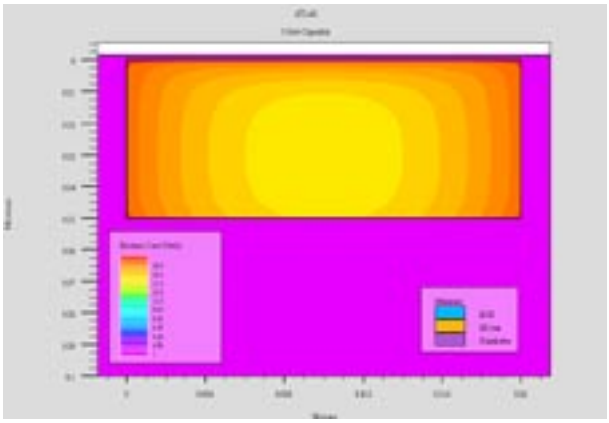


Figure 3. Classical electron concentration.

In the non-equilibrium mode, ***Quantum*** first calculates the self-consistent solution of Poisson's equation with the electron and hole continuity equations as in the standard drift-diffusion model. The Schrodinger-Poisson solutions are then calculated self-consistently using the quasi-Fermi levels from the classical solutions to estimate the non-classical carrier concentrations. This has advantages similar to the post-processing approach but gives self-consistent S-P solutions.

The strained silicon model provides for strain induced splitting in the conduction and valence bands in the solution of Schrodinger's equation.

For radiative modeling, ***Quantum*** provides Schrodinger-Poisson solutions to obtain bound state eigen energies which are used in the calculation of the momentum matrix elements. The Schrodinger-Poisson solutions also give the wave functions which can be used to calculate overlap integrals. The momentum matrix elements and overlap integrals are used in the calculation gain spectra (for lasers) and spontaneous emission spectra (for all light emission devices).

Two-Dimensional Schrodinger-Poisson Example

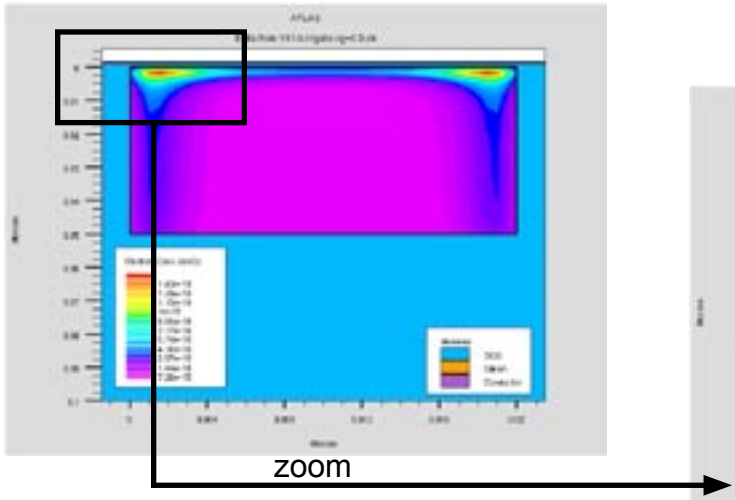
To demonstrate the two-dimensional Schrodinger-Poisson solver we constructed a simple 3 gate capacitor to demonstrate charge confinement in two dimensions. The device, shown in Figure 1, is composed of a heavily doped p-type silicon region completely embedded in silicon dioxide. Gates are placed at the top and either end of the silicon region. A substrate contact is at the bottom.

Figure 2 shows a contour plot of the electron concentration when the gates are biased to 0.5 V. In the figure and the zoomed inset the effects of quantum confinement can be clearly seen.

This can be contrasted with the classical solution shown in Figure 3.

Conclusion

The ***ATLAS*** Quantum model offers a variety of operational modes to accommodate a range of applications to address the effect of quantum confinement.



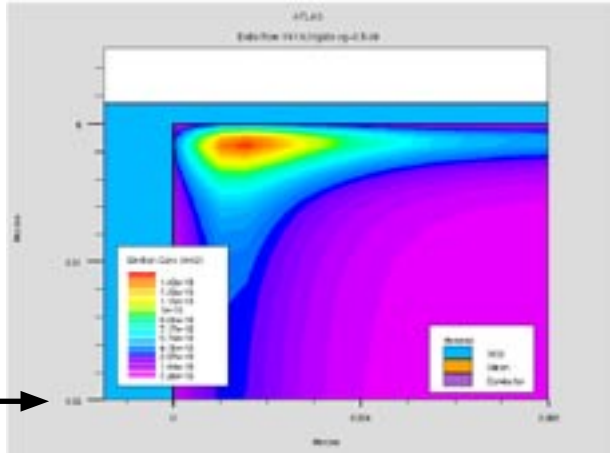


Figure 2 show electrons concentration in linear scale at Vgate=0.5V

Design Rules and Trends for Dummy Metal Filling Using *EXACT, CLEVER* and *STELLAR*

I- Introduction

The physical verification is becoming the most complex phase raised by the Deep SubMicron (DSM) technology. More than 50% of the design time is dedicated to the verification. With the shrink of transistors size, the interconnect delay is dominant versus gate delay. Hence the challenge in the DSM technology depends primarily on how to provide accurate characterization of these interconnects. This is especially the case when dummy metals are present.

Floating dummy metals which are inserted to assist planarization of multi-dielectric layers by chemical-mechanical polishing (CMP) process, have created serious problems because of increased interconnect capacitance. We study in this article dummy filling methods to reduce the interconnect capacitance. These techniques include three ways of filling: 1) square 2) parallel lines, and 3) perpendicular lines. For that purpose, we use parameterized layouts allowing, very easily, the variation of dummies geometrical parameters. We then calculate capacitance by using two types of field solver described below. Finally a capacitance model, depending on the dummies geometry is created in order to perform the optimization of the dummies geometry and number.

II- Parameterized Layout

For this study, we consider a very simple layout consisting of a line over a ground plane surrounded by dummy metals. We wanted to study the impact of dummies geometry and their number on the capacitance between the line and the substrate. For that we use a parameterized layout generator including in our ***EXACT*** [1] tool.

```
i = 0;
LOOP
BEGIN
        i=i+1;
        a = "DUM1_"&i;
        b = &a&"_id";
        y1 = (i-1)*(lD+sV) + sV/2;
        y2 = y1 + (lD);
        b = (set_net
                /name=(a) );
        set_wire
                /layer=(layer1_id)
                /net=(b)
                /width=(wD)
                /name=(a);

        add_point /x=(x1dumLeft) /y=(y1)
                /name="p1";
        add_point /x=(x1dumLeft) /y=(y2)
                /name="p2";

        if (i GTR (nD-1)) then (Leave Loop);

END;
```

Figure 2. Dummy generation in LISA language

Figure 1. Layout Variables definition in Exact GUI.

The parameterized structure layout generator, within ***EXACT***, provides the user with the capability to define their test structures. This is what was done in this experiment. One combines graphical user interface of ***EXACT*** with proprietary scripting language ***LISA*** from SILVACO. All the variables are defined within the GUI as shown in Figure 1 as long as a part of the layout. The dummies are defined using the scripting language ***LISA*** as shown in Figure 2. It generates one column of dummies at a fixed x-ordinate. In this study, 4 columns have been defined. Therefore this piece of script appended to the layout file saved by the GUI of ***EXACT***.

We have designed the layout so that the dummy density remains constant (the average density of materials oxide and metal is kept constant) since our main interest is to study the impact of dummies geometry on the capacitance rather than the density which is imposed by the CMP process. As the total size of the layout is fixed by the ground plate and constant, and the size of metal line is also fixed, the "constant density" condition is traduced by a constant total surface of dummies (nD×lD×wD=Cste). That's why one defines 2 variables: number of dummies nD and their width wD, and so

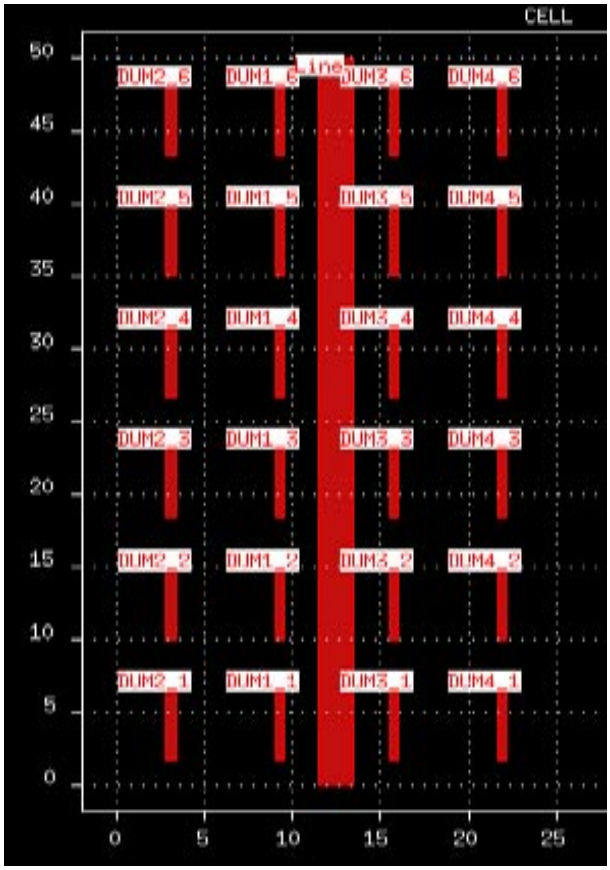


Figure 3. Typical "parallel" line layout under investigation.

their length lD is a function of both according to the equation above. Depending on the combination (nD, wD), we can see, in Figures 3 and 4, different automatically generated layouts: the "parallel" line configuration, the "perpendicular" and "square" ones.

Another variable, s0 defining the spacing between the line and the nearest neighbour dummies, has been defined. This variable defines the minimum spacing between the line and the dummies (DRC rules) and also serves to avoid very high coupling capacitance between the line and the dummies which may cause troubles when analysing the results.

In this way 64 layouts are generated automatically within ***EXACT*** according to Table 1.

	nD	wD	s0
Min	4	0.5	0.8
Max	10	4.0	2.0
Step	1	8	2

Table 1. Layout parameters variations.

Note also that these layouts can be automatically distributed on a multi-cpu machine (one layout per cpu) for capacitance calculation.

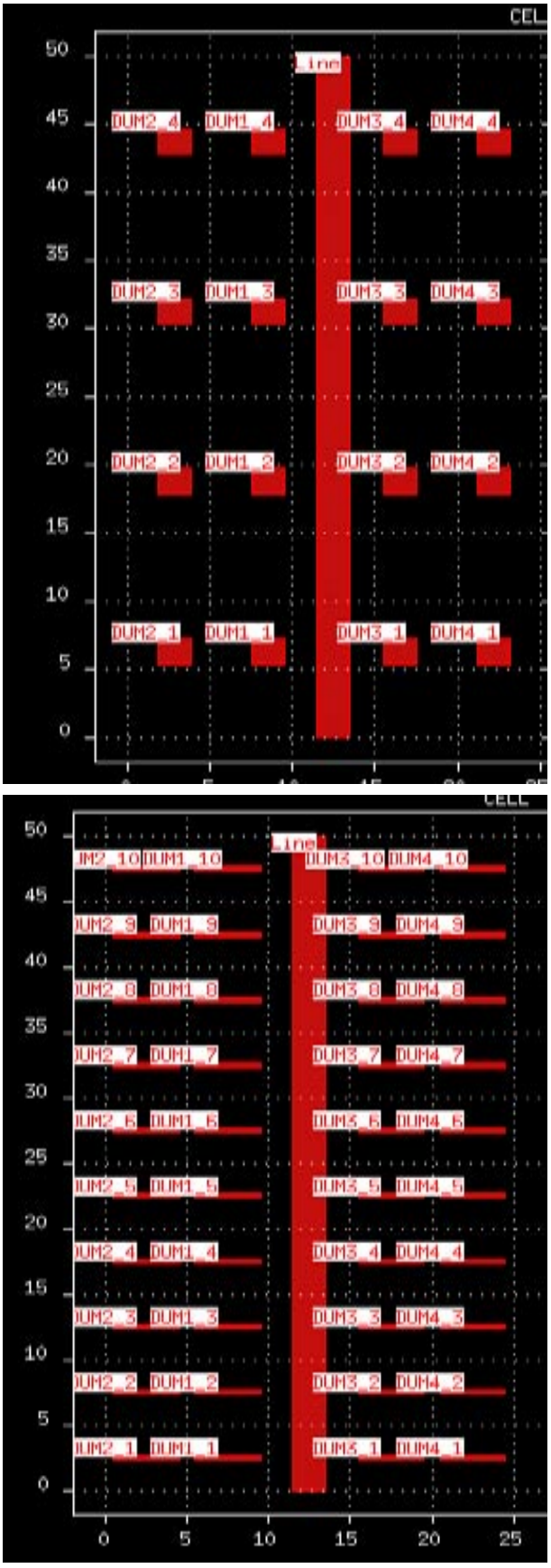


Figure 4. Typical "square" and "perpendicular" lines layouts under investigation.

III- Capacitance Calculation

SILVACO parasitic extraction tools keep the same famous in-house trends so-called TCAD driven CAD which means that as a fundamental core a 3D process simulator is coupled to a 3D field solver in order to accurately extract parasitics.

SILVACO has recently released a new interconnect analysis tool to meet the demands of state of the art cell, circuit and chip design. Indeed based on the very deep success of ***CLEVER*** [2], SILVACO wanted to provide to customers a tool with the same accuracy but dedicated to bigger layouts. This is the role of ***STELLAR*** [3].

Capacitances are calculated from the distribution of charge density on the surfaces of conductors. Classically one can solve partial differential equation on the potential which can be done using finite difference or finite element methods. The normal derivative of the potential on the surfaces gives the charges requested for capacitances calculation. The resultant matrix is sparse but large because the whole dielectrics volume is discretized. A very good 3D tetrahedral mesh is thus needed to solve this problem. Thanks to that, arbitrary conductor shapes and non-homogeneous structure can be handled. This is typically how ***CLEVER*** is built.

In ***STELLAR***, a new method [4] called Fictitious Domain is used. Indeed the meshing of a complex 3D domain is avoided by the use of two different meshes: a regular 3D grid on the whole domain and a surface mesh on the conductors. Thanks to this specific grid (volume + surface) the resultant matrix is sparse and a fast solver can be used to solve this system at low memory cost.

STELLAR allows the computation of structures with floating conductors [5]. They are directly taken into account in the differential formulation of the Fictitious Domain method. This original method is particularly efficient when there are many floating conductors as in dummy metal processes. A "floating conductor" is defined to have a constant potential and a global charge equal to zero. As the surface distributions of charge are internal unknowns of the Fictitious Domain Method, these conditions may naturally be introduced in the matrix system.

CLEVER allows also the computation of structures with floating conductors. No special boundary condition is applied on dummy metal as in ***STELLAR***. All capacitances between conductors are computed by ***CLEVER***. Then a post-processing procedure is used to reduce the matrix of capacitances (see appendix A for more details) taking into account dummies.

V- Results and Design Trends

64 layouts describe in Table 1, are simulated using CLEVER. For geometrical analysis purpose we have decided to plot the capacitance between the line and the substrate versus the parameter α:

$$\alpha = \frac{lD}{wD} - 1$$

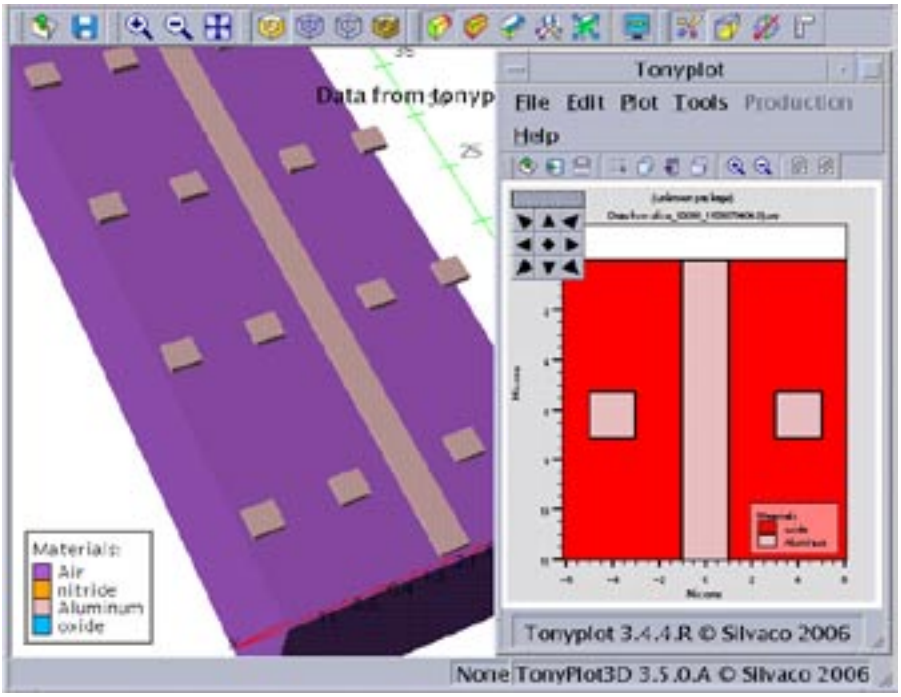


Figure 5. Layout having α parameter around zero

It means that if α is negative then the dummies exhibit a "perpendicular-like" shape whereas if α is positive, the dummies exhibit a "parallel-like" shape. Finally α equal to zero means that the dummy has a square shape as shown in Figure 5.

Figure 6 shows the results obtained by ***CLEVER***: the capacitance Line-Substrate in fF is plotted depending on α, s0 and nD. The orange horizontal line is the value of the capacitance without dummy. One clearly notes 2 families of curves depending on s0, the smallest value of s0 giving the highest capacitance. Finally the 4 different colors correspond to the different values of nD (see legend).

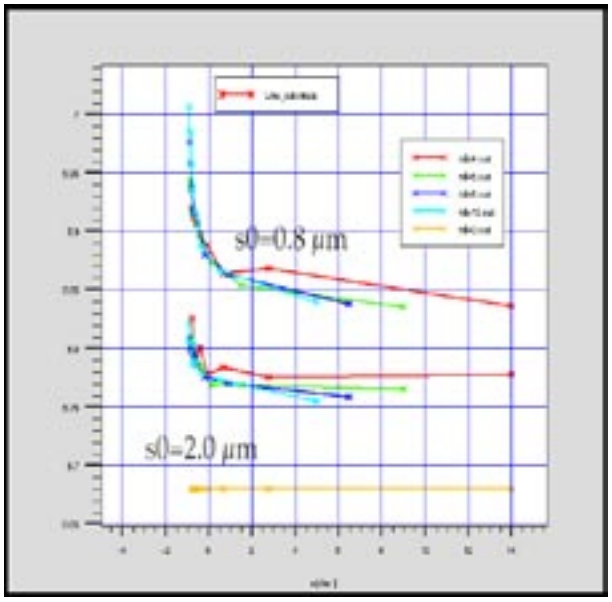


Figure 6: Capacitance (fF) simulated using ***CLEVER*** as a function of the parameter α = (lD/wD)-1, nD and s0.

The 1st interesting point is the distribution of the values. For s0=2.0 μm, the difference between the minimum and maximum of capacitance is only 1% whereas it is 2.5% for s0=0.8 μm. Compared to the value without dummy, the capacitance varies from 1.2% to 5%. The 2nd conclusion is that the capacitance increase is minimum for α positive or close to zero. It means the capacitance is more important when the dummies exhibit a "perpendicular-like" shape. Or reciprocally, the coupling is reduced when the dummies are long and parallel to the line.

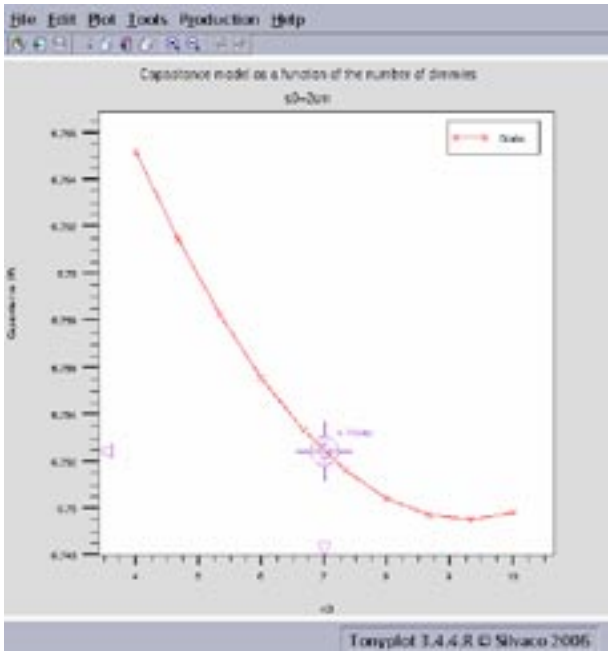


Figure 8. Capacitance value (fF) as a function of nD (number of dummies) for s0=2µm

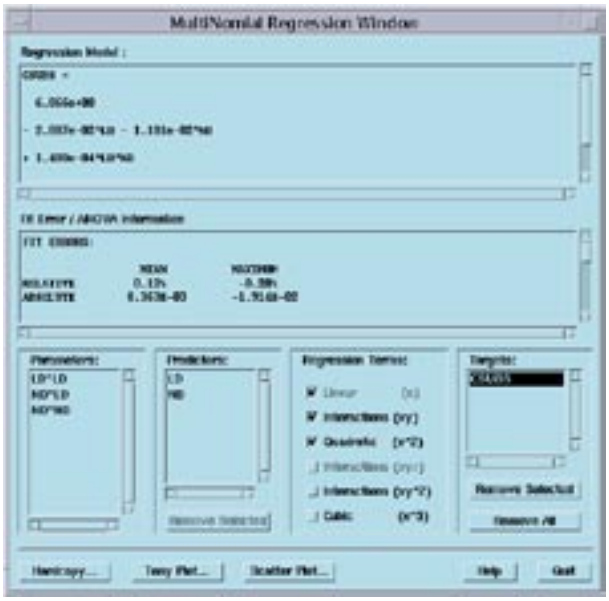


Figure 7. Quadratic capacitance model done in ***SPAYN***. The capacitance is modeled as a function of nD (number of dummies) and lD (length of the dummies) for s0=2µm

EXACT has powerful scripting utilities for manipulating the final capacitance data and variables. Indeed simulated data can be fitted to polynomial expressions using a scripting utilities or statistical analysis like ***SPAYN***. A detailed description of script syntax is available in the ***EXACT*** *User's Manual*. The idea is to load the capacitance database and make various selections resulting in a table of variables and data that we wish to work with.

We then define an equation that will be used to fit the data by using an optimizer. Usually a quadratic model as shown in Figure 7 is generated allowing the designer to explore, verify and optimize his design.

By using this model it is very interesting to notice that the capacitance decreases as the number of dummies increases as can be see in Figure 8.

We have verified, using the quadratic model that the minimum increase of capacitance exists for "parallel like" shape. Indeed, as shown in Figure 9, a local minimum for capacitance value exist as a function of nD and lD. This minimum corresponds to lD=4.65μm, nD=10 and wD=1.3μm (nD×lD×wD=Cste=60) thus corresponding to a "parallel like" shape.

Based on those observations, one can thus estimate that in a real circuit, where signal lines form angles between them (there is obviously not only straight line as in this case under study), the small square shape is probably the most favorable case in order to minimize the increase of parasitic capacitance.

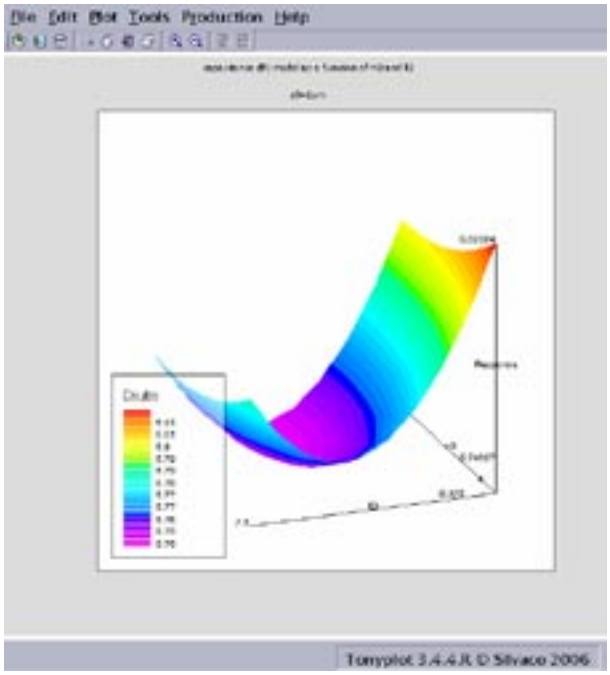


Figure 9. Capacitance value (fF) as a function of nD (number of dummies) and lD (dummy length) for s0=2µm

VI- Explanations of the Results

In the previous part different conclusions have been made and some of them are not obvious. For instance the fact the capacitance decreases with the number of dummies and their length. We will try to explain this below.

By using the mathematical description made in Appendix A, it is possible to find a relationship between the capacitance Line/Substrate when all pieces of metal are treated as conductors and when they are all treated as dummies. With some simple assumptions we can write a simple formula:

$$C_{12}^{dum} = C_{12}^{cond} + \Delta C_{12} \qquad \text{(eq.1)}$$

where indices 1 and 2 stand for Substrate and Line respectively as shown in Figure 10. This means that the capacitance calculated between a line and a substrate is higher when pieces of metal around the line are dummies (constant potential and a global charge equal to zero) as compared to conductors. We will call this effect the dummies effect.

We now want to express C^{cond}_{12} (capacitance of a system with conductors) as a function of C^{∞}_{12} the same capacitance without conductors. In a system with a Line (2) over a Substrate (1) and another conductor (3) far from the Line (see figure 10) we can write this formula:

$$C_{12}^{cond} = C_{12}^{\infty} - C_{23} \qquad \text{(eq.2)}$$

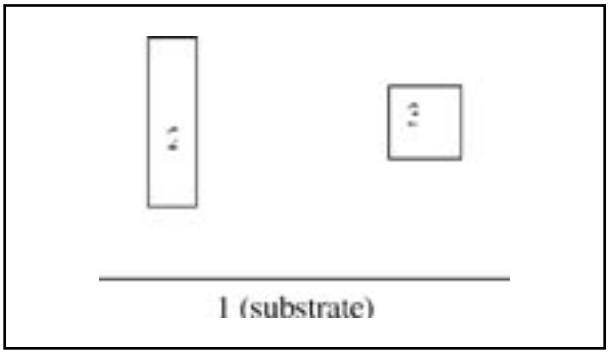


Figure 10: scheme of a Line (2) over Substrate (1) with a conductor (3).

This equation is not really valid when the spacing between the Line and the conductor (3) is small but the trend is always correct: the capacitance Line/Substrate decreases when a piece of metal is placed near the line. This is the screening effect. The electric field lines between the Line and Substrate are blocked by conductor (3), and since the Gauss law gives:

$$C \propto \iint_S \vec{E}\,\vec{n}_s\,dS$$

the capacitance C12cond is reduced. Equations (1) and (2) give:

$$C_{12}^{dum} = C_{12}^{\infty} - C_{23} + \Delta C_{12} \qquad \text{(eq.3)}$$

So equation 3 shows two counter-effects: an increase by dummies effect and a reduction by screening effect. They are shown in figure 11 depending on lD and nD for s0=2μm.

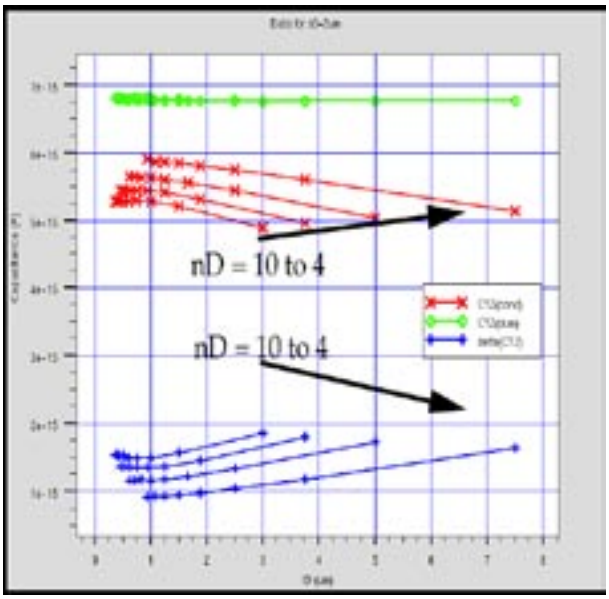


Figure 11. Capacitances (F) as a function of nD and lD for s0=2µm (ΔC12 in blue, C^{cond}_{12} in red, C^{dum}_{12} in green)

One notes C^{cond}_{12} decreases with lD due to the screening effect (eq.2). This screening effect is also more pronounced for a large nD shown in Figure 8 and Figure 11. Also the increase ΔC12 due to the dummies effect has exactly a contrary variation. However this increase doesn't compensate the decrease, resulting in a small decrease of C^{dum}_{12} (better shown in figure 6 than in figure 11). As a conclusion we would say that the screening effect is the dominant effect and is responsible of the decrease of the capacitance as a function of lD and nD.

If the term ΔC12 of equation 1 is developed, an interesting conclusion can be made. Indeed the increase of capacitance is mainly due to the capacitance between Line and the closest dummies. This result is verified by defining 3 different layouts (see figures 12 to 14):

- A layout with 4 dummies around the Line (Figure 12).
- A layout like the previous one with 4 additional dummies (Figure 13).
- A layout like the previous one where the 4 additional dummies have a rectangular shape (Figure 14).

The values of capacitance Line/Substrate calculated by CLEVER are respectively:

3.434 pF, 3.424 pF and 3.417 pF.

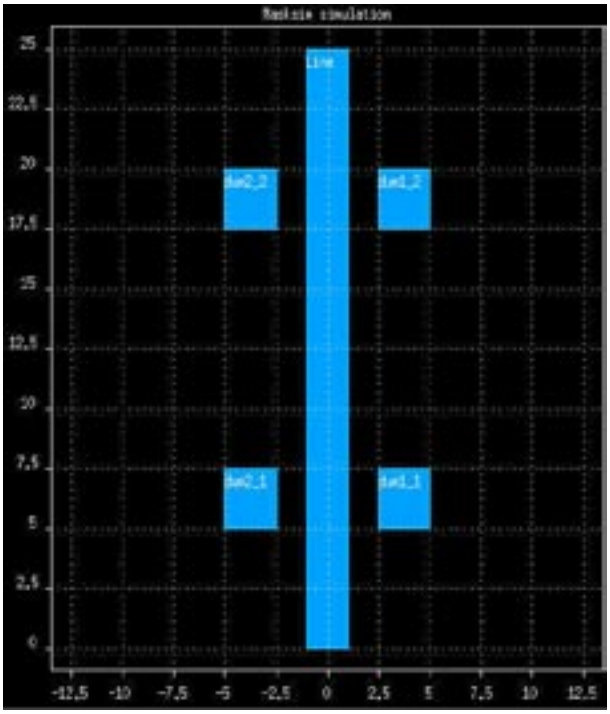


Figure 12: first layout with 4 dummies around the Line.

So it confirms the additional dummies have a negligible effect on the final capacitance. As a consequence the design of dummies not close to signal lines is quite free and so can follow the CMP requirements.

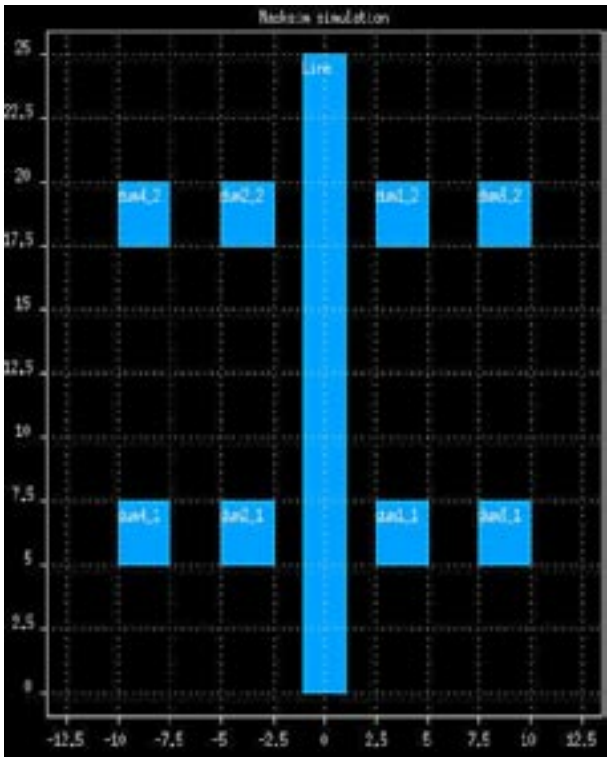


Figure 13: second layout with 4 additional square dummies.

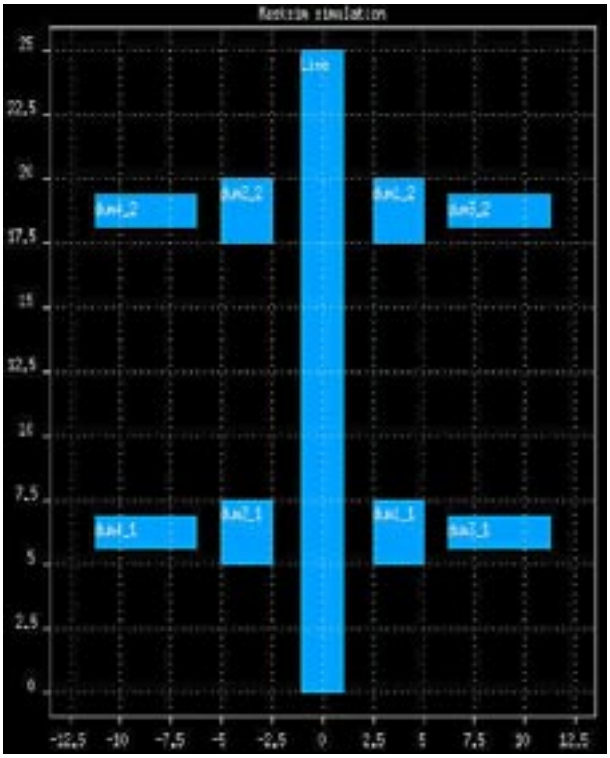


Figure 14: third layout with 4 additional rectangular dummies.

VII- 3D Field Solver Comparison

We have compared ***CLEVER*** and ***STELLAR*** results on 3 different layouts. The results are comparable and shown in Table 2. Layout 1 corresponds to Figure 3, layout 2 and 3 to Figure 4.

	CLEVER (fF)	STELLAR (fF)
Layout 1	6.765	6.615
Layout 2	6.778	6.617
Layout 3	6.281	6.659

Table 2. ***CLEVER*** results versus ***STELLAR***.

It is also important to notice that the simulation time is different between ***CLEVER*** and ***STELLAR*** due to the different numerical methods and the way to treat dummies. The average simulation time is a few seconds with ***STELLAR*** whereas it is a few minutes with ***CLEVER*** on a PC Linux 2.4 GHz AMD 64 bits processor. The observed average simulation time ratio, on the 64 layouts simulated, between ***CLEVER*** and ***STELLAR*** varies from 10 to 100.

VII- Conclusion

We have shown how capacitances calculation can be done taking into account dummy metal using two different field solvers: ***CLEVER*** and ***STELLAR***. By using ***EXACT*** framework, the geometrical analysis of the dummies geometry on the capacitance value, has been easily done thanks to the extreme flexibility of ***EXACT*** (parameterized process and layout by using ***LISA*** script language). We have concluded that the "square-like" geometry minimizes the increase of the capacitance and that additional dummies (on the left and right hand side of the line) have a negligible effect on the capacitance increase. We would to conclude on the simulation time difference between ***CLEVER*** and ***STELLAR***. ***CLEVER*** and STELLAR gave in this study the same results but with a ratio in simulation time from 10 to 100 in favor of ***STELLAR***. We wanted to remember that ***CLEVER*** is designed for capacitance extraction on medium cell size with a very precise description of the 3D back end process, whereas ***STELLAR*** is designed for blocks with a less precise description of the 3D back end process. The different numerical methods used by ***CLEVER*** and ***STELLAR*** are thus responsible of this simulation time difference.

References:

[1] EXACT: Interconnect Parasitic Capacitance Simulator from Silvaco, Simulation Standard Volume 13, Number 2, February 2003.

[2] Validation of CLEVER Interconnect Parasitics with 0.18um Process Measurements, Simulation Standard Volume 9, Number 11, November 1998.

[3] STELLAR – Process Based Parasitics Capacitance Extraction on Large Custom Cells: Overview and Features, Simulation Standard Volume 14, Number 4, March 2004.

[4] Calcul des Capacités Parasites dans les Interconnexions des Circuits Intégrés par une Méthode des Domaines Fictifs, Ph.D. Thesis, Sylvie Puteaux, 2001.

[5] An Efficient Algorithm for 3D Interconnect Capacitance Extraction Considering Floating Conductors, O. Cueto, F. Charlet, A. Farcy, pp.107-110, Proceedings SISPAD 2002.

APPENDIX A

Post-processing in ***CLEVER*** for dummy floating metal

Introduction

To treat the dummies (floating metal) in ***CLEVER***, the user could specify these dummies as made of a dielectric having a high permittivity. This solution is correct and works well in 2D for a limited number of dummies. But in 3D with a high number of dummies, the memory requirement becomes high and it makes this method inadequate.

So to overcome this limitation, another method considering dummies as regular conductor is presented here.

Physical and mathematical description

In a physical point of view, the problem solved by ***CLEVER*** can be wrote q = C.V

where q is the matrix of charges n x 1
C is the matrix of capacitances n x n
V is the matrix of voltages n x 1

n is the number of conductors labeled from 1 to n.

In the case of a conductor:
Vi is known and qi is unknown.
And for a dummy:
Vi is unknown and qi = 0.
Let's develop the matrix C:

$$C = \begin{bmatrix} C_{11} & -C_{12} & -C_{13} & \dots & -C_{1n} \\ -C_{12} & & & & \\ & & & & \\ -C_{1n} & & & & C_{nn} \end{bmatrix}$$

C is symmetrical and non-diagonal coefficients are negative.

CLEVER gives all coupling capacitances

$$C_{ij} \geq 0.0 \quad i \neq j \quad i = 1..n$$

The sum of coefficients for each line is zero:

$$C_{ii} = \sum_{\substack{j=1 \\ j \neq i}}^{n} -C_{ij}$$ (matrix C is singular).

So, once ***CLEVER*** has computed the matrix C, the problem to solve consists in changing the matrices q and V to account for dummies. After a mathematical development, this procedure looks like a reduction of the matrix C by suppressing lines and rows corresponding to dummies. In the following, for simplicity reason, we are going to consider a simple case.

Simplified Case

We propose here to develop the post-processing procedure for a simplified case where k real conductors (k<n) are considered in a system where the matrix C is the same as above. These k conductors are assumed to be labeled from i=1..k. The matricial system is decomposed in blocks:

k unknowns (n-k) zeroes

$$\begin{bmatrix} q^k \\ \dots \\ 0 \end{bmatrix} = \left[\begin{array}{c|c} C^1_{k\times k} & C^2_{k\times(n-k)} \\ \hline \left(C^2\right)^T_{(n-k)\times k} & C^3_{(n-k)\times(n-k)} \end{array}\right] \cdot \begin{bmatrix} V^k \\ \dots \\ \tilde{V} \end{bmatrix}$$

k unknown (n-k) zeroes

where the upper script T stands for the transposed matrix.

We split it in two systems:

$$\begin{aligned} q^k &= C^1 V^k + C^2 \tilde{V} \\ [0] &= \left(C^2\right)^T V^k + C^3 \tilde{V} \\ &\Rightarrow C^3 \tilde{V} = -\left(C^2\right)^T V^k \\ &\Rightarrow \tilde{V} = \left(C^3\right)^{-1} \left(C^2\right)^T V^k \end{aligned}$$

Then the problem is reduced into:

$$q^k = \left[C^1 - C^2 \left(C^3\right)^{-1} \left(C^2\right)^T\right] V^k$$

and the non-diagonal coefficients of matrix

$$\tilde{C} = C^1 - C^2 \left(C^3\right)^{-1} \left(C^2\right)^T$$

are the capacitances between the k real conductors when all others are dummies. They are the values searched. We can note that only one matrix inversion is needed. Moreover C3 is singular, so it can be easily inverted by a Cholesky decomposition making the inversion limited to the inversion of a triangular matrix. It means the extra cost required by this post-processing is negligible.

Hints, Tips and Solutions

Keunsam Rhee, Senior Applications and Support Engineer

Q. Is it possible to calculate the resistance components of a MOSFET (i.e. channel resistance, epi resistance, substrate resistance etc.) as a function of gate bias?

A. The resistance components of a MOSFET, Trench UMOS or LDMOS device can in general be obtained from the quasi-Fermi level potential and the terminal current.

To illustrate the resistance calculation, the standard example "mosfetex01.in" was used. A structure file is saved at a drain voltage of 0.1V and a gate voltage of 3V. In ***TonyPlot***, plot the Net Doping contour as well as the Electrodes. Using the Cutline tool, do a horizontal cut across the device along the channel from the source to the drain.

Then using the "Function" options create a function that is defined by the electron QFL divided by the drain bias at the operating point. The drain bias is a constant that can be taken from either the run-time output or a plot of the log file. Plotting this function will give the cumulative resistance along the channel from the source to the drain.

You may also want to determine the channel resistance as a function of gate bias. To do this you can use the EXTRACT and PROBE statements as follows:

First, use the EXTRACT statement to obtain the locations of the junction edges. The following lines show how to obtain the locations of the junction edges 0.01 microns below the oxide interface.

```
go atlas
# Find out the y location of the oxide in-
  terface
extract init infile="mos1ex010.str"
extract name="xj_y" min.bound y.pos
 material=Silicon" x.val=0.5 y.val=0.5
```

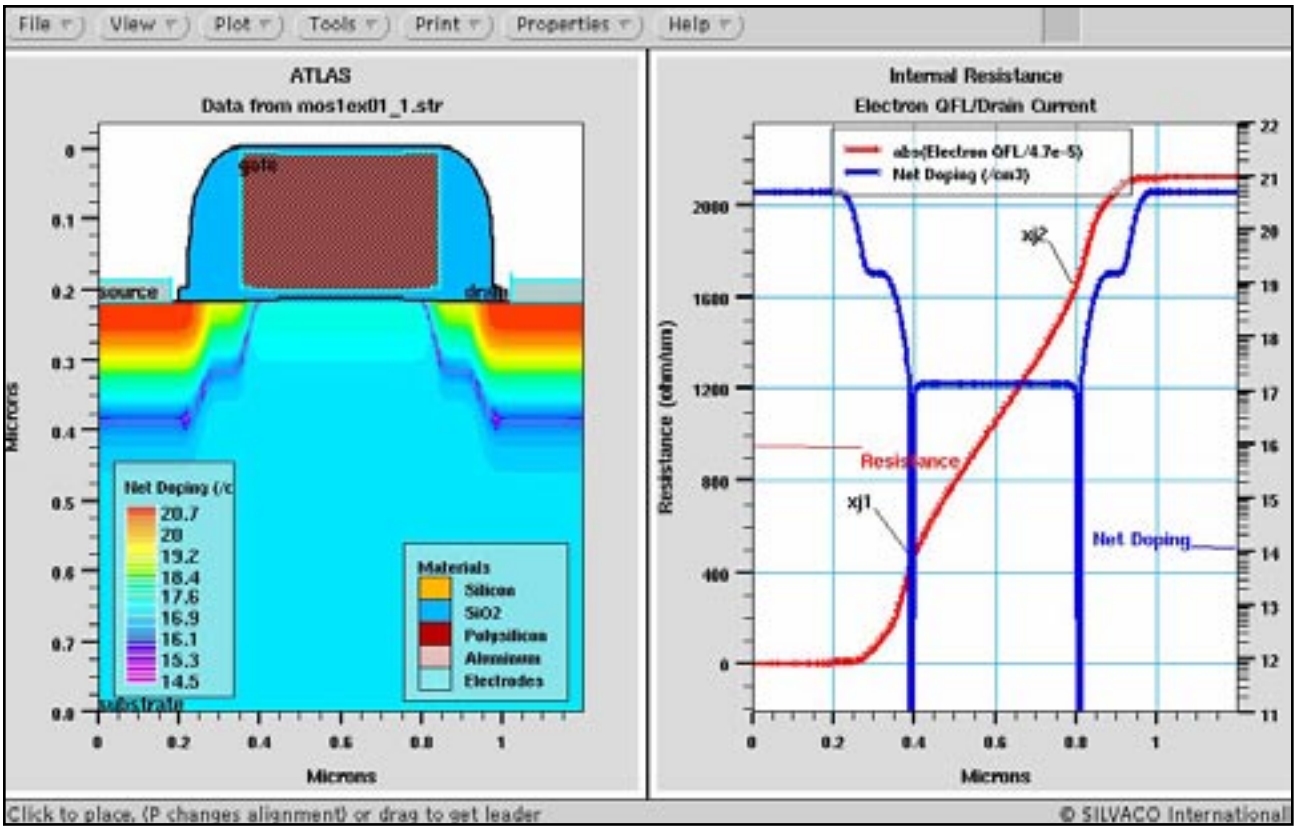


Figure 1. Target MOSFET device structure and resistance distribution along the gate channel cutline(0,0.22)-(1.2, 0.22)

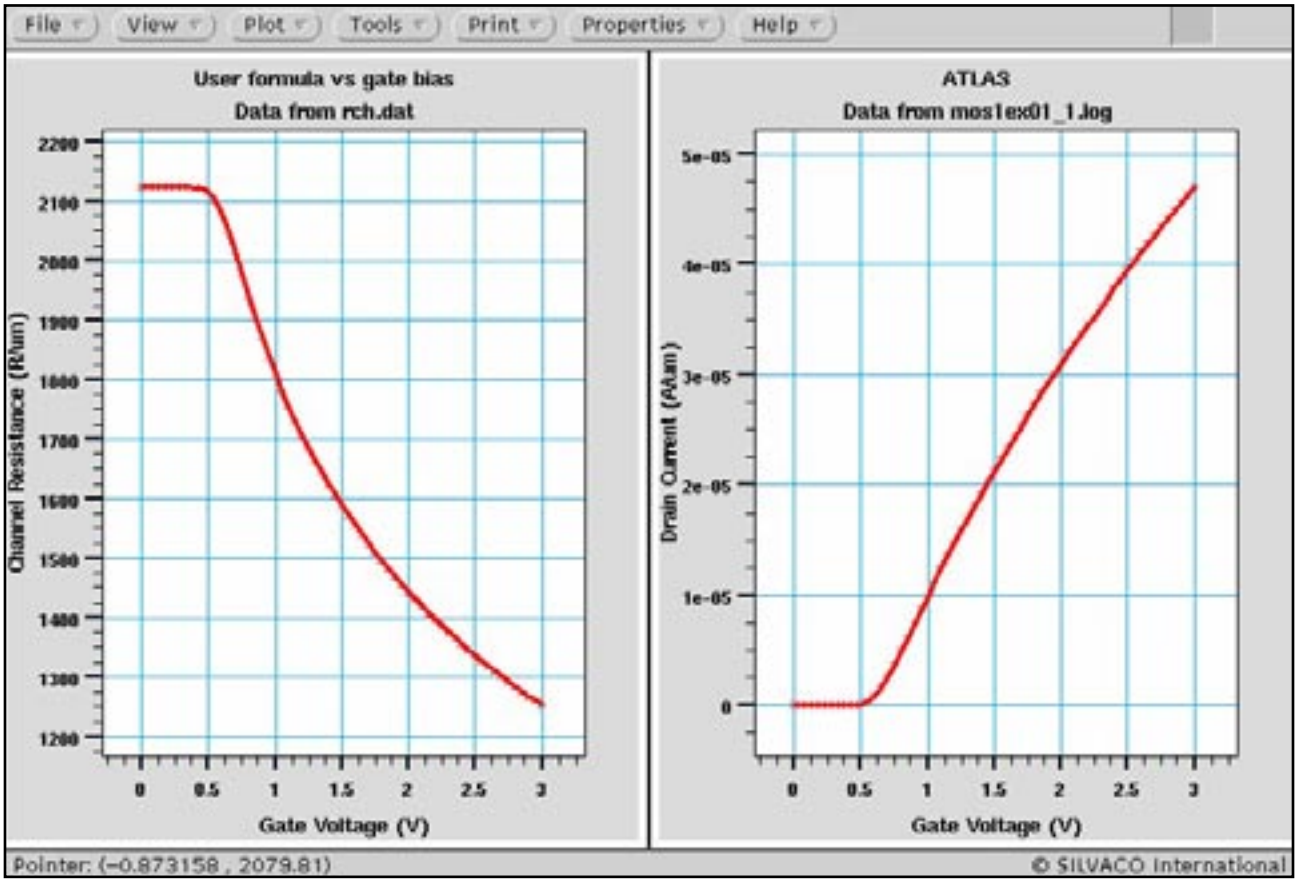


Figure 2. Channel Resistance and IdVg curve.

```
#
# set the location to 0.01 microns below
  the interface
set xj_y=$xj_y+0.01
# find the locations of the junction edges
extract init infile=mos1ex010.str"
extrace name="xj1" xj material="Silicon"
  mat.occno=1 y.val=$sj_j junc.occno=1
extrace name="xj2" xj material="Silicon"
  mat.occno=1 y.val=$sj_j junc.occno=2
```

Now the PROBE statement can be used to determine the values of the electron QFL at the two junctions. The following lines show how to extract the electron QFL values as a function of gate bias.

```
probe name="ch1" x=$xj1 y=$xj_y qfn
probe name="ch2" x=$xj2 y=$xj_y qfn

# ramp gate
log outf=mos1ex011.log master
solve vgate=0 vstep=0.05 vfinal=3.0
  name=gate
```

Finally, you can extract the channel resistance as a function of gate bias.

```
extract infile="mos1ex011.log"
extract name="id" max(curve(v."gate",i,"dra
  in"))
extract name="Rch" curve(v."gate",abs(probe
  ."ch1"-probe."ch2")/$id)
  outf="rch.dat"
```

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