Enhanced Silicon Light Emission Intensity with Multiple SiGe Quantum Well Structure

Abstract
The measured I-V curve from a ten period Si/SiGe MQW pin LED fabricated using a UHVCVD system[1] is compared with ATLAS simulation results. A sizable silicon emission peak is observed at high current injection mode at room temperature. This phenomena can be explained as follows: because of the hetero-junction between the top silicon buffer layer and MQW, when bias increases there is a potential barrier formed due to band bending. Thus there will be a large accumulation of holes in the buffer layer. The recombination rate in this layer increases which results in increased silicon light intensity.

Introduction
The use of silicon germanium (SiGe) for optoelectronic components is highly advantageous since SiGe is compatible with Si based technologies. Improved growing techniques for heterostructures have also made the manufacturing of SiGe based devices much easier. Advantages of using SiGe for optoelectronic structures include the low defect density of the material, which enhances operation at room temperatures. Also a SiGe based device's operating wavelength can be tuned over the range of 1.3um to 1.55um making them ideal choices for optical fiber communications. Therefore there is wide spread interest in SiGe and SiGe based devices. The device studied in this article is a ten period Si/SiGe multi quantum well (MQW) structure. ATLAS is then used to simulate the device and the simulated data is compared to the measured I-V data. In this way a more physical insight into the device operation can be obtained.

Preparation
The device studied in the article utilizes a p-i-n structure with a silicon buffer layer. The sample was grown on n-Si(001) substrates by a UHV chemical vapor deposition (UHV-CVD) system at a pressure of 5×10⁻⁹Torr at 600°C for all of the epitaxial layers. After depositing a 25 nm undoped Si layer on the n+ substrate, the 10 periods consisting of Si/Si₀.₅Ge₀.₅ making up the MQW structure were grown. Each period of the MQW consists of a 3.9 nm Si₀.₅Ge₀.₅ well and a 3nm Si barrier. However, because of the background doping of the UHV-CVD, this region was actually lightly p-type doped (N_A~10¹⁶cm⁻³) and denoted as P- region. After the growth of the MQW, a 24nm undoped Si layer was deposited. Finally, a silicon layer was deposited on top acting as the buffer layer. The top layer is heavily doped p-type (N_A=10¹⁹cm⁻³) in order to form an ohmic contact.

Continued on page 2...
The material parameters and the MQW module parameters used in ATLAS are as following:

\[
\text{mqw } \text{ww}=0.0039 \quad \text{wb}=0.003 \quad \text{mwell}=10 \quad \text{nx}=5 \quad \text{ny}=240 \quad \text{acceptors}=1\text{e}16 \\
\text{xmin}=0 \quad \text{xmax}=0.05 \quad \text{ymin}=-0.094 \quad \text{ymax}=-0.022 \quad \text{material}=	ext{SiGe} \quad \text{xcomp}=0.5 \\
\text{material}=	ext{silicon} \quad \text{EG300}=1.12 \quad \text{affinity}=4.05 \quad \text{taun0}=1\text{e}-7 \quad \text{taup0}=1\text{e}-7 \quad \text{ni}=1\text{e}10 \\
\text{nc300}=2.8\text{e}19 \quad \text{nv300}=1.8\text{e}19 \quad \text{mun}=1450 \quad \text{mup}=450 \quad \text{vsatn}=2.4\text{e}7 \quad \text{vsatp}=1.65\text{e}7 \quad \text{bn}=1 \quad \text{bp}=0 \\
\text{material}=	ext{siGe} \quad \text{EG300}=0.917 \quad \text{affinity}=4.033 \quad \text{taun0}=4\text{e}-11 \quad \text{taup0}=4\text{e}-11 \quad \text{mso}=0.1625 \quad \text{ni}=1\text{e}12 \\
\]

**Discussion**

Figure 1 shows a cross section of the device. Figure 2 shows the measured and simulated IV curves. Figure 3 shows the simulated device band diagram at zero bias. The band diagram and corresponding hole distribution for three different injection currents are shown in Figure 4. Figure 5 shows the intensity versus energy for two different injection currents. From Figure 5 we see that for low injection levels the light intensity has two peaks, one for Si and one for SiGe. Both the peaks are somewhat comparable. As the injection level is increased the peak corresponding to SiGe is considerably reduced whilst the peak...
corresponding to the Si material is increased. Even though excellent confinement is achieved by the quantum wells, the main component in the optical spectrum at high injection levels is not from SiGe, as expected, but from Si.

To try to understand the phenomena simulations were performed to analyse the electron and hole distributions in the structure (shown in Figure 6). For initial injection currents, holes flow into the quantum wells and are stored in them. This in turn promotes a build up of the internal electric field at the interface of the QW/Si buffer regions. This electric field - band bending forms a barrier to hole flow. Figure 6 shows that the hole distribution in the quantum well for injection currents of 50mA and 250mA is almost the same, however in the Si buffer region the hole distribution is increased by a factor of almost five for the two injection currents. As the light emission is dependent on the radiative recombination and the radiative recombination in turn is proportional to the electron-hole product, the Si light emission increases considerably with higher injection currents whilst the SiGe light emission receives little increase.

Conclusion

We successfully simulated a MQW SiGe LED which can enhance Si light emission using ATLAS. This has enabled the underlying physical behaviour of the device to be more thoroughly understood.

Reference

Comparison of 3-Dimensional Quantum Effects in Nano Devices
Using the ATLAS3D BQP Model

Introduction

With the MOSFET gate lengths scaling down to sub-20nms many kinds of devices have been proposed and researched such as double-gate, tri-gate, four-gate and gate-all-around (wire) MOSFETs.

In this work, the carrier distribution and capacitance of these 4-types of nano MOSFET were compared using the Bohm Quantum Potential Model [1] in ATLAS3D.

Nanodevice : Geometry and Structure

Figure 1, shows the nanodevice structures. (a) is a double-gate MOSFET, (b) is a tri-gate FET, (c) is a four-gate FET, and (d) is a Wire FET. All these structures have a common gate oxide thickness of Tox=1nm, silicon thickness of Tsi=5.6nm (on nanowire the diameter is 5.6nm), gate length of W=5.6nm, and total device length of L=8nm. Also, the doping level used is \( N_A = 1 \times 10^{16} \) cm\(^{-3}\) and \( N_D = 1 \times 10^{20} \) cm\(^{-3}\).

![Materials: Conductor, Silicon, SiO2](image1)

(a) Double-Gate FET(2)

![Materials: Conductor, Silicon, SiO2](image2)

(b) Tri-Gate FET(3)

![Materials: Conductor, Silicon, SiO2](image3)

(c) Four-Gate FET(4)

![Materials: Silicon, SiO2, Aluminum](image4)

(d) All-around(Wire)-FET(all)

Figure 1 : Scheme of the Nano-Devices. Tox=1nm Tsi=5.6nm, L=5.6nm W=8nm
(a) DG-FET, (b) Tri-Gate FET, (c) Four-Gate FET, (d) Wire FET.
Simulation

The Bohm Quantum Potential (BQP) model is an expansion of the Wigner equation and calculates the effects of quantum confinement on the electron and hole concentration and C-V curves [1].

As we have 4 different structures, we compared carrier concentration on the center cutplane of the gate as shown in Figure 2.

Figures 3 and 4 show the effects of carrier confinement on the center of the gate channel. The tri-gate FET with no gate electrode on bottom shows asymmetrical confinement.

Figure 5 shows that the electron concentration distribution at a gate voltage of 1.0V. From this concentration distribution it can be seen that the wire FET has an isotropic electron carrier concentration.

Figure 2. Cutplane Position Carrier Distribution Comparison.

Figure 3. Electron Concentration with BQP Solution at Vgate=0.0V.
The peak electron and hole concentrations of the 4 MOSFET types are shown in Table 1.

Figure 6 shows how the threshold voltage depends on the structure of the 4 devices. The dual gate FET has the lowest threshold voltage but the lowest above threshold conductance. But the four gate and wire FET show higher threshold voltages than the dual gate FET. The four FET has higher drain current than the wire FET because of the area and confinement effect of the FETs.

**Conclusion**

This article presents the basic characteristics of 4 types of nano devices using the BQP model in 3-Dimensional structures. The characteristics are very dependent on the device geometry so the carrier confinement distribution and C-V curves are consequently different. The BQP model is very effective and flexible at simulating quantum confinement effects for 3-Dimensional geometries.

**Reference**


<table>
<thead>
<tr>
<th></th>
<th>Electron Concentration</th>
<th>Hole Concentration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual-GateFET</td>
<td>1.6e14</td>
<td>8.9e7</td>
</tr>
<tr>
<td>Tri-Gate FET</td>
<td>1.99e13</td>
<td>6.03e7</td>
</tr>
<tr>
<td>Four-Gate FET</td>
<td>1.0e12</td>
<td>1.07e9</td>
</tr>
<tr>
<td>Wire-Gate FET</td>
<td>2.51e11</td>
<td>7.9e9</td>
</tr>
</tbody>
</table>

Table 1. Peak carrier concentrations.
Figure 5. Electron Concentration with BQP Solution at $V_{g}=1.0\text{V}$ and $V_{d}=0.4\text{V}$.

Figure 6. Comparison of $I_dV_g$ and C-V Curves.
Evaluating of the Avalanche Failure of Power MOSFETs using ATLAS

Introduction

Power MOSFETs are widely used with an inductive load for S/W power supplies, DC-DC converters, and so on. But due to high frequency operation, the surge voltage applied to the MOSFETs at turn-off depends on the inductance and parasitic inductance in the circuit. For some operation modes, the pulse width for the turn-on or off will be very short, and the device fails due to the short surge period.

In this article, the device simulator ATLAS was used to predict the maximum inductive loads and find out the failure current due to the device intrinsic temperature.

Single Pulse Unclamped Inductive Switching

Figure 1 shows that the single pulse unclamped inductive switching (UIS) test circuit for avalanche testing. Figure 2 shows the traditional operation waveform (avalanche operation waveform)[1].

The avalanche current ($I_{AV}$) depends on both the inductance value and the direction of the on time (PW). Therefore, to get a high $I_{AV}$, a small inductance or a long on time should be chosen.

From the circuit shown in Figure 1, the single pulse avalanche energy ($E_{AV}$) can be calculated:

$$E_{AV} = \frac{L}{2} \cdot I_{AV}^2 \cdot \frac{V_{DSS}}{V_{net} - V_{nn}} \tag{1}$$

The measured energy value depends on the avalanche breakdown voltage, $V_{DSS}$, which tends to vary during the discharge period due to the device temperature increase. Also for low $V_{DSS} - V_{DD}$, there is limited use of this circuit because it introduces a high-test error. Here the most important value is $BVDSS$, which depends on the device temperature. So the effects of self-heating should be also considered to predict the device operation and avalanche failure.

Avalanche Failure Mode Analysis

I. Active Mode (Parasitic Bipolar Effect)

Most semiconductor devices contain parasitic components intrinsic to the physical design of the device. In power MOSFETs, these components include capacitors due to displaced charge in the junction between p and n regions, resistors associated with material resistivity, a body diode formed where the p+ body diffusion is made onto the n- epilayer, and an NPN sequence (BJT) formed where the n+ source contact is diffused[2].

Figure 3a shows a U-Groove gate region design, and Figure 3b shows the complete circuit component model. This structure has already been considered for gate charging characteristics.[3]

In avalanche, the p-n junction acting as a diode no longer blocks voltage. With higher applied voltage a critical field is reached where impact ionization tends to infinity and carrier concentration increases due to avalanche multiplication.

The electric field inside of the device is most intense at the point where the junction bends. This strong electric field causes maximum current flow in close proximity to the parasitic BJT. The power dissipation increases
temperature, thus increasing $R_b$, since silicon resistivity increases with temperature. When the voltage drop is sufficient to forward bias the parasitic BJT, it will turn on with potentially catastrophic results, as control of the switch is lost. But in practice the failure is passive mode due to the thermal effect under UIS conditions (Figure 1 and Figure 2).

II. Passive Mode (Thermal Effect)
During unclamped inductive switching as the MOSFET is subjected to increasing energy, the internal chip temperature rises dramatically as in Equations 2 and 3.

$$\Delta T_M \propto I_{AV}^3$$  \hspace{1cm} (2)

$$\Delta T_M \propto E_{AV}^3$$  \hspace{1cm} (3)

where $I_{AV}$ and $E_{AV}$ are the avalanche current and single pulse avalanche energy respectively. But this approximate calculation has a large error when predicting the internal device temperature.

ATLAS with self-heating and MixedMode can simulate the exact device temperature dependence on the channel doping profile and parasitic BJT as well as the avalanche breakdown voltage due to the device temperature.

Simulation Results and Discussion
Figure 4 shows the traditional single pulse UIS waveform. This UIS condition does not consider the effects of self-heating and the device temperature is constant at the room temperature.

The avalanche operation time can be obtained but it is not possible to tell if this circuit is under safe operation conditions or not. So if the self-heating effects are considered with thermal resistance, then the effects of that device capability on the UIS condition can be found. Figure 5 shows that the test power device has a breakdown voltage of 58V at room temperature[4].

Under UIS circuit conditions, $\frac{V_{BS}}{3} \approx 20$ V was chosen. To predict the safe operation range, the inductive load ($L$) and the avalanche ($I_{AV}$) current was varied. The inductive load was chosen as 0.1mH, 1mH, 10mH. For 0.1mH and 1mH the avalanche current was simulated from 10A to 50A with a 10A step. For 10mH, the avalanche current was simulated from 5A to 10A with a 1A step.

For safe device operation under UIS, the maximum device temperature must be under 608K(335°C). For power MOSFETs, at this temperature, current increased rapidly, forming a localized hot spot that quickly becomes a destructive mesoplasma.
Figure 5. Power MOSFET breakdown voltage is (58V).

Figure 6 and Figure 7 show the switching avalanche waveform. Figure 6 shows that the maximum device temperature is lower than the device intrinsic temperature, (335°C) while Figure 7 shows that the maximum device temperature is higher than 335°C.

Figure 8, can be used to find the device safe operation range under UIS conditions. In this plot, the blue line is from the simulated data, X is avalanche failure condition, O is avalanche safe condition. Depending on the inductive load and avalanche current the predicted safe operation range is close to the measured data(red line).

**Conclusion**

This article shows the capability of ATLAS to predict the avalanche failure of the power devices under the Unclamped Inductive Switching (UIS) conditions. During single pulse UIS, the device temperature is higher, and under some conditions, the device temperature is can exceed the intrinsic temperature (335°C). ATLAS can be used to predict the safe operation range.

**Reference**


[2] A.Narazaki, K.Takano, K.Oku, H.Hamachi and T.Minato, “A Marvelous Low on-resistance 20V rated Self Alignment Trench MOSFET(SAT-MOS) in a 0.35um LSI design rule with both high forward blocking voltage yield and large current capability”, *ISPSD’04*. 7-1, p.393-396


Interconnect Parasitic Extraction of BiCMOS Cell Using Simucad CLEVER

1. Introduction
Interconnect parasitic effects play a very important role in modern integrated circuit design, especially for digital circuit. This article presents how a cell level BiCMOS nand gate is extracted with R (resistances) and C (capacitances). The extracted RC result is then back-annotated into SPICE netlist for POST verification purpose. We used the Simucad product, CLEVER which is a highly accurate 3D process interconnect RC extractor.

2. Description of BiCMOS Cell Extractor and Simulation Results
2.1 Overview
In order to perform parasitic extraction, we need a layout file and a command file. Command file defines the physical processes and starts the interconnect simulation. It also generate the 3D structure files and SPICE netlist. The layout file can be in the form of a GDS format. Besides, we may also need a layer mapping file which provides a name for each layer and a rule file which is similar to the technology file to define active device and connectivity. Figure 1 shows the data flow inside CLEVER. Figure 3 is the saved layout after loading the layer mapping file. The new layer names are showed in this layout.

2.2 Layer mapping file and rule file (tech file)
To start, CLEVER loads the GDS format layout. We renamed its corresponding layer number by some meaningful names (Figure 2) for convenience. These layer names are used in defining the rule file. The rule file defines the connectivity between layers. It also defines both the active devices (we only used MOS and BJT in this article) and the passive devices (resistor diode and capacitor). Defining the rule file is the key to accurately extract the device geometry from a layout file. Here we will demonstrate a simple BiCMOS nand gate rule file which contains five NMOS transistors, two PMOS transistors and two BJTs.

And !nwell active NACTIVE
And nwell active PACTIVE
And NACTIVE poly NGATE
And PACTIVE poly PGATE
And NACTIVE !poly NSD
And PACTIVE !poly PSD
Not nwell PSD PSUB
Not !nwell NSD NSUB

The Boolean operations above define NMOS and PMOS transistors with substrate region(four terminal device). As for BJT, there are three types of BJT format in CLEVER.

1. **Collector type**: Collector contains base, base contains emitter.
2. **Emitter type**: Emitter contains base, base contains collector.
3. **Base type**: Base contains collector and emitter.

<table>
<thead>
<tr>
<th>nwell</th>
<th>active</th>
<th>poly</th>
<th>pbase</th>
<th>nselect</th>
<th>pselect</th>
<th>cont</th>
<th>metal1</th>
<th>buried</th>
</tr>
</thead>
<tbody>
<tr>
<td>drawing 42 0</td>
<td>#NWELL</td>
<td>drawing 43 0</td>
<td>#Active area</td>
<td>drawing 46 0</td>
<td>#Poly gate</td>
<td>drawing 58 0</td>
<td>#Pbase</td>
<td>drawing 45 0</td>
</tr>
<tr>
<td>drawing 44 0</td>
<td>#pselect</td>
<td>drawing 25 0</td>
<td>#Contact</td>
<td>drawing 49 0</td>
<td>#Metal1</td>
<td>drawing 38 0</td>
<td>#buried_n+</td>
<td></td>
</tr>
</tbody>
</table>

Figure 2. Renaming GDS number.
We used the first type of BJT definition (collector contains base and base contains emitter).

And pselect pbase base1
And base1 active BASE
And nselect pbase emitter1
And emitter1 active EMITTOR
And nselect buried COLLECTOR1
And COLLECTOR1 active COLLECTOR
2.3 Simulation Results

Once the layout file and rule file (technology file) are loaded, CLEVER will start the process simulation such as deposition, etching and lithography. There are two types of etching/deposition modes in CLEVER. Geometric mode allows the user to quickly build up the so-called “Manhattan” structures in which all regions have either vertical or horizontal faces. The physical mode is more accurate and is based on parameters such as etch/deposit rate, time, and others. It provides a generic way of simulating the physics behind process steps such as chemical vapor deposition (VCD), chemical mechanical polishing (CMP), or reactive ion etching (RIE). A 3D structure is created from the process simulation. The physical mode will take more time and memory while creating a more realistic structure. There is a trade-off between accuracy and simulation time. In our example, we use the more realistic physical mode.

Figure 6. 3D structure after final process.

Figure 7. Top view with gate oxide layer.
The commands in Figure 4 demonstrate CLEVER loading a layout file which is the cell “nand_gate_new_exploded” in the GDS file “bicmos.gds”. It also loads a layer mapping file “gds_map.map” and a technology file “nand_gate.lmp”. The `save` command saves the renamed layout file and the initial netlist extracted from CLEVER by using the rule file. A more realistic lithography and deposition process is used for the active layer. Then the commands in Figure 5 save the 3D structure and performs interconnect analysis on the 3D structure. Figures 6, 7, 8 are the saved 3D structures. Finally, a RC netlist (Figure 9) is saved and will be included in a SPICE simulator such as SmartSpice (Simucad Spice simulator).

The parasitic effects are clearly seen from Figures 11 and 12. This waveform shows that functionality (Figure 10) is correct for a BiCMOS nand gate and time delays. This RC delay is critical for digital applications.

**Conclusions**

We have performed RC extraction based on a cell level BiCMOS nand gate using the Simucad tool, CLEVER. CLEVER helps IC designers extract accurate RC parasitics for both active and passive devices on the layout level. With physical processes integrated with layout, users can use CLEVER to investigate and improve the cell layout design and minimize parasitic effects. The 3D structure extraction ability can also help the designers to visually modify their structures after verification.
Figure 10. Waveform of initial netlist without RC extraction

Figure 11. Comparison simulations between netlist with RC and netlist without RC

Figure 12. Zoomed in waveform comparisons
JOIN THE WINNING TCAD TEAM

USA Headquarters:

Silvaco International
4701 Patrick Henry Drive, Bldg. 6
Santa Clara, CA 95054 USA

Phone: 408-567-1000
Fax: 408-496-6080
sales@silvaco.com

www.silvaco.com

Contacts:

Silvaco Japan
jpsales@silvaco.com

Silvaco Korea
krsales@silvaco.com

Silvaco Taiwan
twsales@silvaco.com

Silvaco Singapore
sgsales@silvaco.com

Silvaco UK
uksales@silvaco.com

Silvaco France
frsales@silvaco.com

Silvaco Germany
desales@silvaco.com