Inductance Optimization using 3D Field Solver based on Design Of Experiment Approach

Abstract
A new 3D electromagnetic simulator coupled with a statistical analysis, for inductance loop optimization is presented. It allows RF designers to easily create inductor design by only specifying as inputs the desired inductance and Q factor for example and get as outputs layout parameters like radius, wire width, space between wires and numbers of coils. To do so, inductance simulations using Design of Experiments (DoE) approach are done and subsequent Response Surface Model (RSM) are generated. Performing an optimization on the RSM model a gds2 inductance loop layout is generated according to the user specified initial constraints and will be ready to use in a design of RF-circuits. Inherent to this new methodology the designers can now take into account process variations which is mandatory for current technology node.

1. Introduction
Up to a few GHz, on-chip inductors are among the most critical components to design radio-frequency integrated circuits (RFIC). The main parameters that characterize an inductor are its self-inductance value L, its cut-off frequency and its quality factor Q (a good inductor has a high Q). For on-chip inductors, Q is limited for example by the inductor’s series resistance, the resistive loss (skin effect and proximity effect) and the current induced by the capacitive coupling to the ground plane and the substrate. In this context it is imperative to allow engineers to easily and accurately create any RF structure and give designers the flexibility to innovate new geometries simply by editing parameters such as radius, number of turns, width and spacing of coils. The aim of this paper is indeed to explain how this can be possible using a specific methodology based on Design Of Experiments approach in combination with a new field solver simulator.

2. 3D Electromagnetic Simulation
In this paper, we use the 3D electromagnetic field solver QUEST. QUEST is very accurate to design and characterize arbitrary 3D passive structures (inductance loop for example) as a function of process and layout parameters. QUEST is mainly dedicated to simulate multi-level interconnections according to the current technology (typically up to 8 metal levels). Some conductors may be grounded (connected to a reference potential) or floating (not connected to any potential).
QUEST computes firstly the 3D structure resulting of the layout information, process and techno file inputs, then, after simulation, QUEST can give RLGC parameters, S-Y-Z-parameters, Q factor and spice model for inductance loop simulation and standard Spice W-element format for transmission line simulation (Figure 1). All these output parameters are function of the frequency. These results are stored in a database and can be used in post-treatment for statistical analysis for example.

3. Field Solver

QUEST is based on a 3D field solver elaborated in collaboration with CEA-LETI[1][2]. We use an original formulation of the Quasi-Static Maxwell equations where the problem is separated in two parts, an impedance and a capacitance part.

The impedance problem is written using a (A, T) formulation [3], where A is the magnetic vector and is an equivalent electric potential vector defined on the conductors surface, µ the mobility, ω the frequency and _ the conductivity.

\[
\nabla \times \mu^{-1} \nabla \times A - \nabla \times I = 0 \\
\n\nabla^2 \times (\sigma \nabla \times T) - j\omega \nabla \times A = 0
\]

The magnetic potential vector A is calculated using edge finite elements [4] on a 3D regular grid (Figure 2a). The electric potential vector is calculated using scalar P1 elements on a triangle meshing of the conductors surfaces (Figure 2b).

The capacitance problem comes from the equation

\[
\nabla^2 \times (z^2)^{-1} \nabla^2 \phi = j\omega p^2
\]

where are the surface potential and the surface electric charge respectively. z^2 is a local impedance given by the impedance problem. It is solved using a fast and accurate computation method so called « fictitious domain method » [1].

4. Inductance Loop Validation

QUEST results have been validated in collaboration with ST Crolles on realistic inductors using advanced CMOS processes (0,12um technology, 6 metal levels). QUEST directly uses real gds2 files and can compute any type of geometries (square, spiral, octagonal inductors). Figure 3 presents a 4-turns inductor structure computed by QUEST. The real process with a quasi unlimited numbers of dielectric layers can be directly taken into account without any simplification.
We made comparison between measurements and simulations on a 2-turns, 4-turns and 5 turns inductors. As can be seen in Figure 4 and 5, simulations and experimental data match very well. The Q-factor was given by $Q = \frac{-\text{Im}(Y_{11})}{\text{Re}(Y_{11})}$ and $L$ extracted from the imaginary part of $\frac{1}{Y_{21}} = -(R + jwL)$. Different types of inductors have also been validated but not shown here. The simulations of the inductance loops were performed on a Linux PC AMD 2800 64 bits. The simulation time for the 2 turns inductance shown in Figure 5 was 10min with 21 frequency points.

5. Inductance Synthesis and Optimization

After having validated the field solver, we will use and show an original methodology to design inductance loop based on simulation results instead of experimental data from real wafers (which is long to have and very expensive). As an example, we want to design a gds2 inductance loop layout, based on a 0.12um technology from ST, having as constraint a minimum area and a specific value of inductance $L$. For that purpose, Design of Experiment (DoE) approach and parameterized gds2 layout have been used. Indeed the idea is to make a variation of layout parameters such as radius, number of coils, width and spacing and run the simulations using a DoE for subsequent modeling using Response Surface Model (RSM)\cite{5}. Performing an optimization on the RSM model gds2 inductance loop layout can be generated according to the user specified initial constraints and will be ready to use in a design of RF-circuits. To achieve this goal, the first step is to create a parameterized gds2 layout. For that purpose, the script language of a layout editor (Expert from Silvaco) was used to create a generic parameterized inductance gds2 layout as a function of layout parameters (Radius, Wire Space and Width, Number of coils) as shown in Figure 4. Now we want to vary layout parameters of the inductance previously defined. The frequency range for the simulation was set between 100Mhz to 9Ghz. The wire width was varied from 4um to 12 um, the space between wires from 4um to 10um, the number of coils from 2 to 4 and the radius between 50um to 150um. A third order full factorial DoE has been used for the layouts parameters. 27 different layouts were created. Different RSM models were generated ($L$, $C$, $Q$, S-Parameters ...) as a function of layout parameters (space, width, number of coils, radius). By using the RSM model for the inductance, very interesting information for the designer can be found. For example isosurface values (Figure 6) of inductance as a function of radius, number of coils and wire width, allow to have a first idea of the area needed to design the inductance layout. Another interesting information for the designer is the correlation between parameters. Indeed the inductance value is highly correlated to the radius and number of coils and less to the wire width and wire space as shown in Figure 7.
This is a good indication for the designer in order to focus his effort in optimizing the preponderant parameters. The ultimate goal is to perform automatic synthesis of the “ideal” gds2 inductance layout that the user has to design for a specific circuit. The aim is to find, for example, the set of layout parameters to obtain an inductance value of 2nH using a minimum surface of silicon for a circuit working at 2Ghz. For that an optimization is performed based on the inductance RSM model and the following results are obtained: NBcoils=3, Width=4.8um, Space=5.2um and Radius=60um. The designer now has at his disposal a complete inductance layout corresponding to his need. He can easily perform a second optimization without running any additional simulations in specifying for example a specific value for L and Q factor or even use a desirability function like the maximum of L with a fixed value for the Q factor.

He will then obtain in a few seconds a new gds2 inductance layout corresponding to what he wants.

After having defined his nominal layout parameters the designer may want to study the impact of the frequency and the variation of process parameters. For example the Q-Factor is shown, in Figure 8, as a function of the frequency for the layout with its nominal values previously obtained (NBcoils=3, Width=4.8um, Space=5.2um and Radius=60um) The designer can easily see the variation of the characteristics of the inductance anticipating the needs of his circuit to work at a different frequency.

Using the same concept as previously defined we can also make variation of process parameters (Thicknesses of dielectrics or metals, permittivity ..) in order to predict the output parameters of the inductance (L, Q, S-Parameters ..) as a function of process variation. This is very interesting for designers in order to integrate the fab process variation in the design. After having modeled the desired outputs (Q-factor for example) as a function of process parameters we can use Gaussian distribution given by the foundry for each process parameters. This distribution correspond to the deviation of each process parameters as compared to their nominal value due to the variation of process condition in the fab (calibration of machines, temperature variation ..) Then, we include for each process parameters the corresponding distribution in the RSM model. As a result we are able to determine what is the deviation of the output parameters (Q-factor for ex) including the process variation from the foundry. 4 process variables have been used in this example : Metal5 and Metal6 thicknesses and inter metal dielectric IMD4 and IMD5 thicknesses as illustrated in Figure 9. The domain of variation of these process parameters are shown in Table 1. A third order full factorial DoE has been used leading to 81 simulations.

Sensitivity analysis shown that the Q-factor is highly dependent on Metal5 and Metal6 thicknesses (Figure 10d). A Gaussian distribution for each process parameters have been set as input in the RSM model for Q-factor, R and L, with a standard deviation of +/- 10% as compared to their nominal value.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nominal</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>M5 Thickness (um)</td>
<td>0.25</td>
<td>0.35</td>
<td>0.45</td>
</tr>
<tr>
<td>M6 Thickness (um)</td>
<td>0.86</td>
<td>0.96</td>
<td>1.06</td>
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<td>IMD4 Thickness (um)</td>
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<tr>
<td>IMD5 Thickness (um)</td>
<td>0.26</td>
<td>0.36</td>
<td>0.46</td>
</tr>
</tbody>
</table>

Table 1: Domain of variation of process parameters.

Figure 7. Pareto graph showing the correlation between the inductance value and the layout variables.

Figure 8: Q factor as a function of the frequency.
One can observe in Figure 10a a Gaussian distribution of the Q-factor with a mean value of 6.86 and a standard deviation of 0.225. This variation is mainly due to a change of the resistance as a function of process parameters (Figure 10b) whereas the inductance does not vary (Figure 10c). Based on these results, the designer has a better understanding of the behavior of his inductance versus the process variation and thus can take them into account during the design. In this example, a +/- 10% of Metal5 and Metal6 thickness variation will result in +/- 3.2% on the Q-factor as shown in Figure 10a.

**Conclusion**

This article presented a new field solver simulator based on a original numerical method. Complex and complete inductance layout can be simulated very accurately. Thanks to the speed of this new simulator and integrated DoE feature, statistical analysis (meaning 10 to 100 simulations) is now possible in a only few hours. We have established a completely new approach to design inductors. Designers can now perform inductance synthesis and also include process variation in their design for the first time in realistic simulation time.

**Acknowledgments**

We acknowledge STM Crolles to have provided measurements and support to accomplish this work.

**References:**


