Simulation Standard

Connecting TCAD To Tapeout

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Simulating the Source of Polarization Charge in AlGaN/GaN HFETs

Polarization-induced charges at the AlGaN/GaN interface of heterojunction field-effect transistors (HFETs) create a high density, two-dimensional electron gas (2DEG) in the channel. One approach to simulating the 2DEG is to place a fixed positive charge at the AlGaN/GaN interface, thus attracting a fixed quantity of electrons to the channel. Silvaco's ***ATLAS*** software can do this with either an INTERFACE statement or automatically with the use of the POLARIZATION parameter on the REGION statement. This is fine, as far as it goes, but this simple approach glosses over some nuances having to do with the source of carriers in the channel. A paper by Ibbetson, *et al.*,[1] explored this question theoretically and experimentally. Based on an analysis of the electrostatics of the structure, they determined that surface states at the top of the AlGaN barrier are the most likely source of the electrons attracted to the channel. This article demonstrates the simulation of this effect.

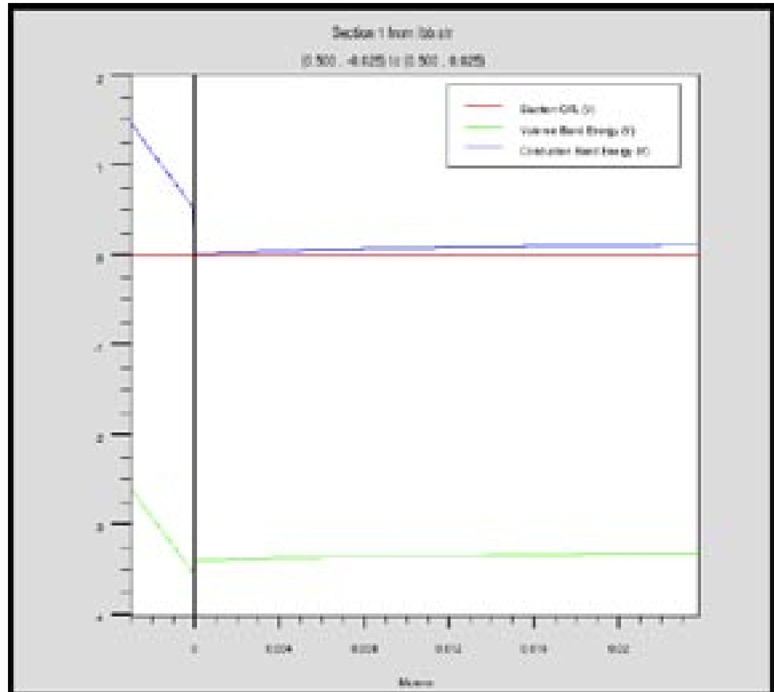

Figure 1. Band diagram of 30 A of AlGaN on GaN.

Ibbetson gave two possible explanations of the mechanism by which charge is transferred from the surface donor states to the 2DEG. Our simulations support his second explanation, that of surface pinning of the Fermi level. In wurtzite materials, the polarization has a spontaneous and a piezoelectric component. It is assumed that the relatively thick GaN buffer layer is unstrained, so it has only the spontaneous component. So fixed charges for GaN, 2.122e13 cm^{-2}, are placed at the top (-2.122e13 cm^{-2}) and bottom (+2.122e13 cm^{-2}) of the buffer layer. The thin AlGaN layer is assumed to experience a uniform strain from its composition-dependent lattice mismatch with the GaN substrate. For the 34% AlN composition of AlGaN used in Ibbetson's experiments, the nominal value of the total polarization charge is 4.005e13 cm^{-2}, so -4.005e13 cm^{-2} is placed at the top surface of the AlGaN and +4.005e13 cm^{-2} is placed at the bottom, at the interface with GaN. Therefore, the total polarization charge placed at the interface is +1.883e13 cm^{-2}, which would attract that density of electrons to the 2DEG in the channel. That is not

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SILVACO INTERNATIONAL

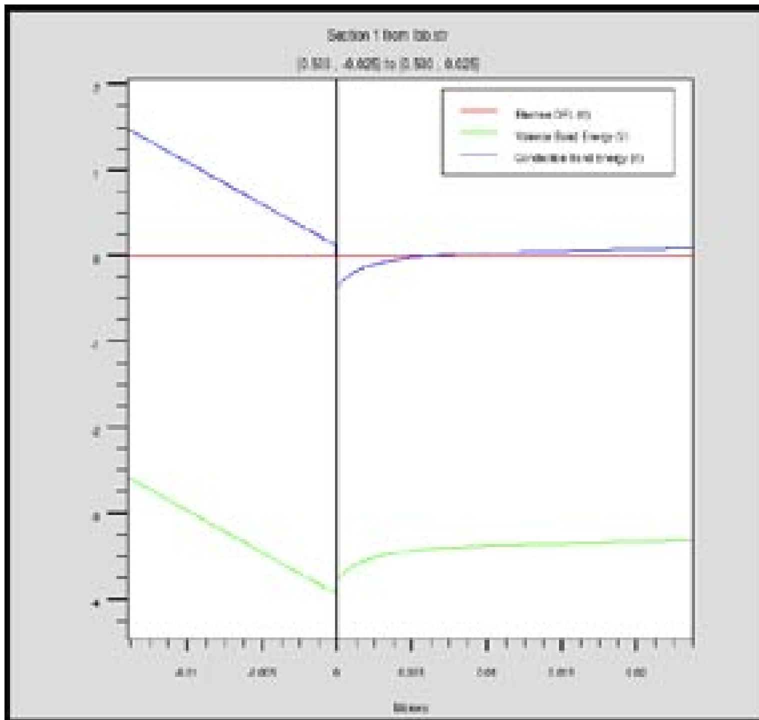


Figure 2. Band diagram of 140 A of AlGaN on GaN.

Conclusion

In conclusion, understanding and controlling the source of the electrons in the 2DEG in AlGaN/GaN HFETs is important for the optimization of their performance. The Silvaco toolset has shown itself to be useful in this regard.

exactly the density value actually found for the 2DEG. The density of the 2DEG varies with the thickness of the AlGaN layer.

Figures 1 and 2 show that the Fermi level at the AlGaN surface is pinned at 2.6 volts above the valence band by the presence of the donor traps and the polarization charge. In Figure 1, the thickness of the AlGaN is 30 A. In this case, the Fermi level is below the GaN conduction band, so no accumulation of charges occurs in the channel.

In Figure 2, the thickness of the AlGaN layer is 140 A, and the Fermi level is above the GaN conduction band at the interface, creating a depletion region in which electrons may accumulate to form the 2DEG.

In order to match Ibbetson's measured results, we adjusted three variables: the ionization energy of the donor surface traps, the magnitude of the AlGaN polarization charge, and the density of the surface traps. The surface trap density had to exceed that of the surface polarization charge. This was done in ***ATLAS*** with the help of the ***DeckBuild*** design of experiments tool, Batch DOE. Figure 3 overlays our simulated (red) and the measured (green) results.

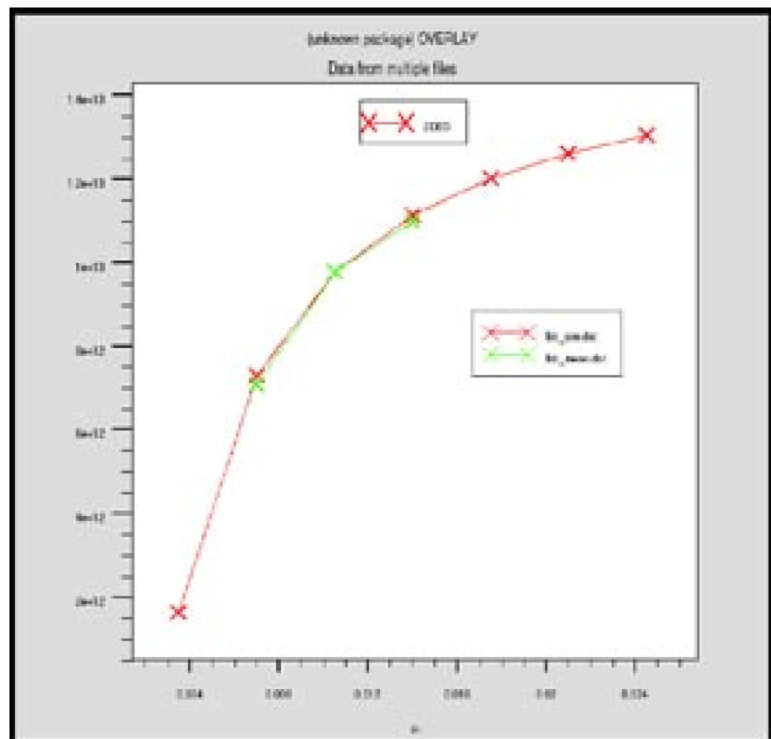


Figure 3. 2DEG density versus AlGaN barrier thickness.

References:

[1] Ibbetson, J.P., ***et al***, "Polarization Effects Surface States, and the Source of Electrons in AlGaN/GaN Hetrostructure Field Effect Transistors", Appl. Phys. Lett., V.77, N.2, 10 July 2000, pp. 250-252.

ATLAS Device Simulation of Amorphous Oxide Semiconductor Thin-Film Transistors

1. Introduction

Amorphous oxide semiconductor materials have attracted much attention as key components of TFTs for flexible electronics [1]. The advantages of such materials include flexibility and transparency which are compatible with plastic substrates, and higher mobilities than those of amorphous-Si and organic semiconductor TFT materials.

In this paper, the operation of an amorphous oxide semiconductor TFT was analyzed by the two-dimensional numerical simulator ***ATLAS*** to verify the applicability of standard drift-diffusion models to an amorphous oxide semiconductor material.

2. The Device Structure and Models

An amorphous oxide semiconductor TFT fabricated and reported by Nomura et al. [2] was simulated and resultant ID-VD and ID-VG curves were compared with measured data.

The device structure reported is shown in Figure 1. Top gate structure was adopted. Amorphous In-Ga-ZnO (a-IGZO) channel layer was fabricated on a polyethylene terephthalate (PET) sheet. A high-k dielectric Y_2O_3 material for gate insulator and transparent indium-tin oxide (ITO) material for the source, drain and gate electrodes were deposited. The channel length and width are 50 μm and 200 μm respectively.

In order to grasp the fundamentals needed to describe a-IGZO TFT electrical behavior, models which are as simple as possible were selected and their parameters were calibrated as follows:

For all the ITO electrodes, Schottky contact model with work function of 4.6 eV were chosen. For the a-IGZO material, an acceptor type density of states model with no doping, constant electron mobility model of 8.0 $cm^2/(Vsec)$, and band-to-band tunneling model were assumed.

Figure 2 shows the energy distribution of acceptor type density of states used. Unlike amorphous-Si or many organic materials, slope of tail state is quite gentle and peak density of states is located not at band edges but around mid-gap.

3. Results and Discussion

The output characteristics are shown in Figure 3. The simulation results (blue lines) are in fairly good agreement with the measured data (red lines). Since the mobility dependencies of a-IGZO material have not been fully investigated yet and remains mostly unknown, constant mobility model is used. The mobility modeling for a-IGZO material may improve simulation accuracy much further.

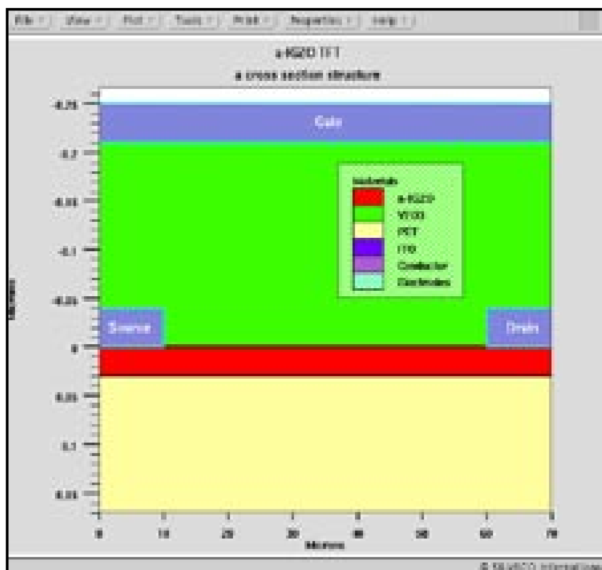


Figure 1. Cross section of the a-IGZO TFT.

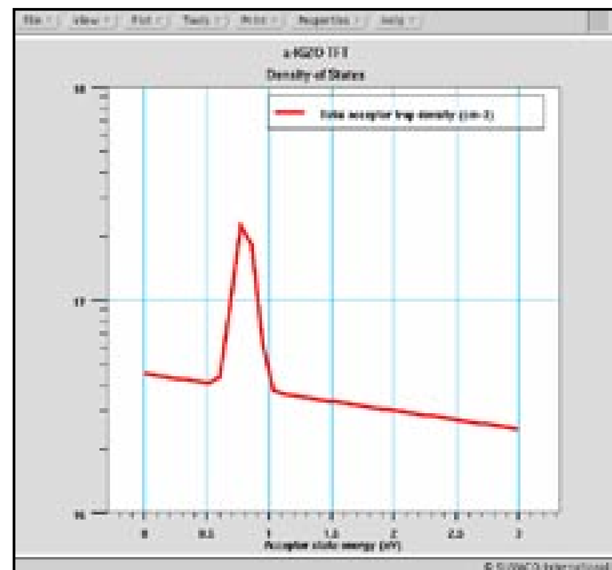


Figure 2. Energy distribution of acceptor type density of states assumed.

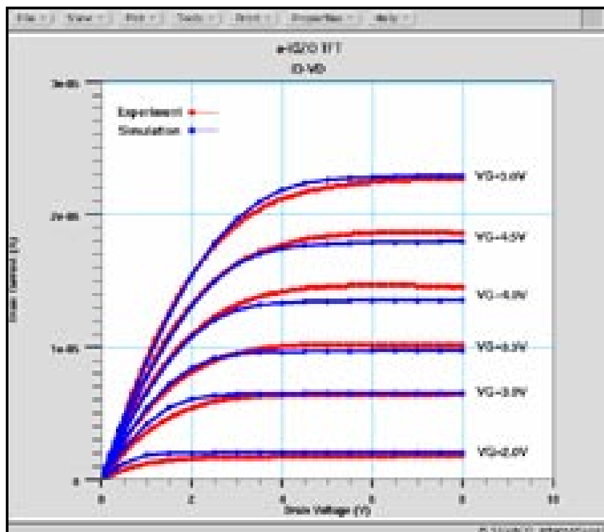


Figure 3. Simulated ID-VD curves with the experimental data.

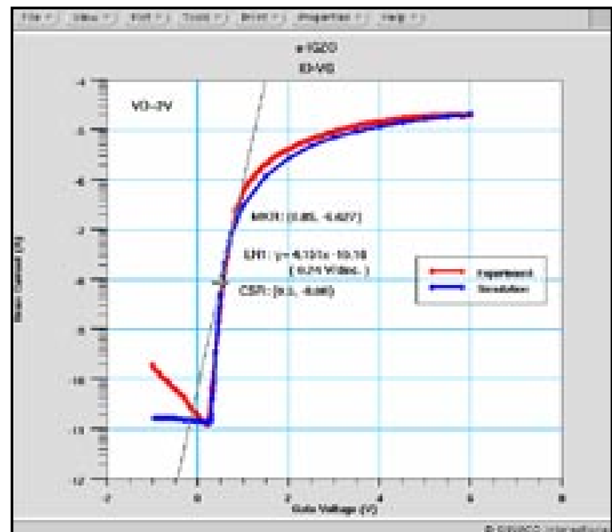


Figure 4. Simulated ID-VG curve with the experimental data.

The simulated transfer characteristic (blue line) for a drain-source voltage of 2V is shown in Figure 4 with measured curves (red line). The simulated on/off current ratio of about 1.0e6 and the subthreshold slope about 240 [mV/decade] are well agreed with measured data. For the gate reverse biased region, though it is stated in ref.[2] that drain current corresponded with gate current in measurements, gate current model is omitted as a matter of minor importance. That is thought to be the cause of the difference in drain off currents. But as such gate leakage current may cause the interface charge between a-IGZO and Y_2O_3, in this particular case, a sheet charge of 1e11 [1/cm^2] is assumed to simulate the ID-VG measurement curve.

Figure 5 shows electron concentration distribution in the channel layer with potential contour lines superimposed both in on state (upper picture) and off state (lower one). Channel pinch-off is clearly shown near the drain in on state, and channel electron is well depleted in off state and hole inversion layer about 1.0e17 [1/cm^3] which is also superimposed as contour lines comes out under gate. Depending on the donor type density of states which are not needed to be considered this time, there may be a possibility for complementary operation.

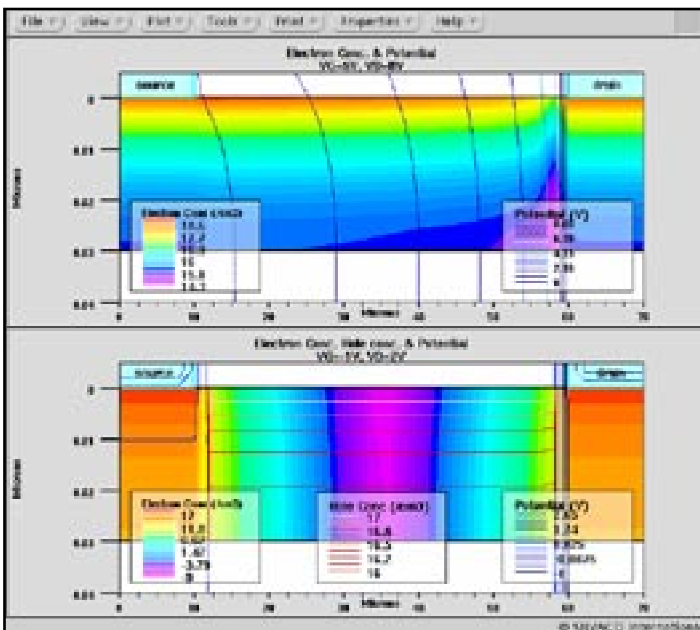


Figure 5. Electron concentration in the channel layer and superimposed potential contour lines in ON and OFF state respectively.

4. Conclusion

In this paper, it was shown that the electrical characteristics of an amorphous oxide semiconductor TFT can be simulated numerically by standard drift-diffusion models in ***ATLAS***. A density of states model was used to characterize the a-IGZO material for trapped charges and generation/recombination in it.

The models of standard drift-diffusion with density of states have wide applicability not only for organic materials [3] but also for amorphous oxide semiconductors.

References

[1] K.Nomura, H.Ohta, A.Takagi, T.Kamiya, M.Hirano, and H.Hosono, Nature, vol.488, 432(2004).

[2] K.Nomura, A.Takagi, T.Kamiya, H.Ohta, M.Hirano, and H.Hosono, Jpn.J.Appl.Phys., Vol.45, No. 5B, 4303(2006).

[3] *Simulation Standard*, Vol.12, No.2, 1(2003).

Accurate Spice Netlist Extraction in *STELLAR* Using New Substrate Partition Feature

I Introduction

By default ***STELLAR*** calculates the capacitances between interconnect lines and the whole substrate. In certain conditions it may lead to some inaccuracies. For example ***STELLAR*** may calculate the capacitance of a poly line over an active area but this capacitance is already present in the spice compact model (Cox). Another example is that the substrate of a MOSFET transistor is usually connected to Vdd or Gnd depending on its polarity. So we may need to separate the Vdd areas from the grounded substrate. The aim of the substrate partition feature is to divide the substrate in different regions to calculate or not capacitances between interconnect lines and these different substrate regions. For example, we do not want to calculate the capacitance between a line over the substrate region shown in Figure 1.

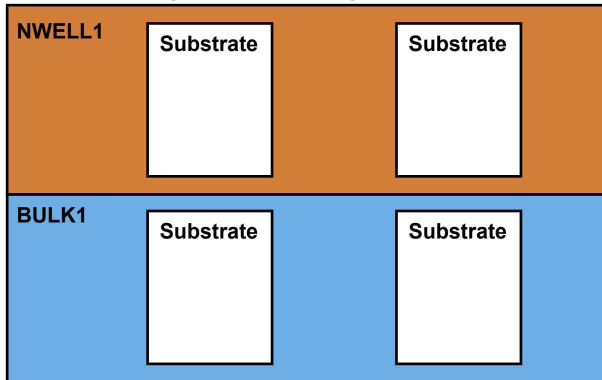


Figure 1. Final mask layers defined in ***STELLAR***.

II *STELLAR* GUI

Techno file: layer setup

We will explain here how to define the mask layers shown in Figure 1. The NWELL, PACT, NACT regions are defined in the original gds file (Figure 2).

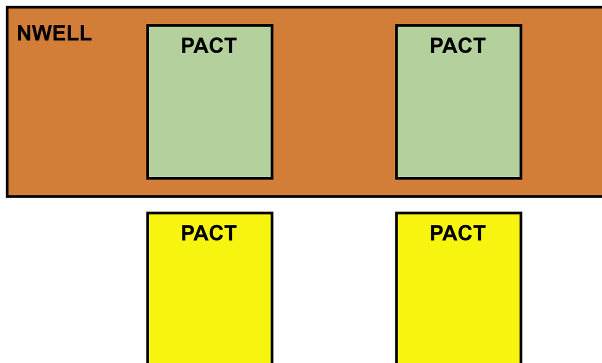


Figure 2. Original mask layers in the gds file.

The other layers are defined in the technology panel of ***STELLAR***

BULK is defined as a « Derived Layer » (Figure 3).

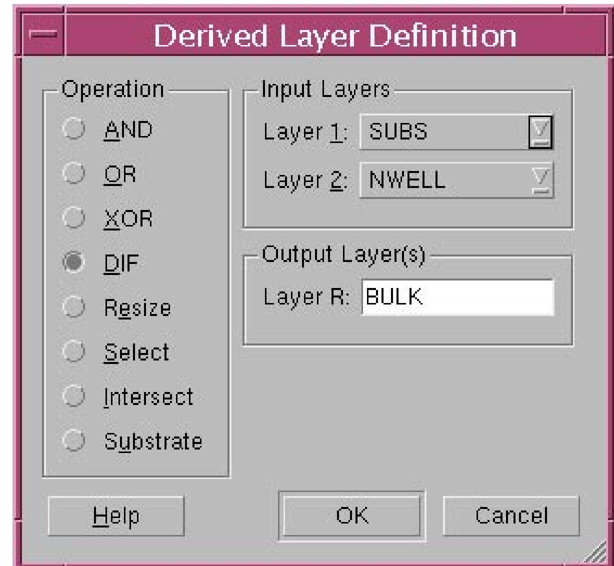


Figure 3. BULK derived layer definition.

SUBS is a key word in ***STELLAR*** which defined the total surface of the substrate (actually the smallest area including all the layout). The NWELL1, BULK1 are defined in the ***STELLAR*** GUI also as « Derived Layer » (Figure 4 and 5).

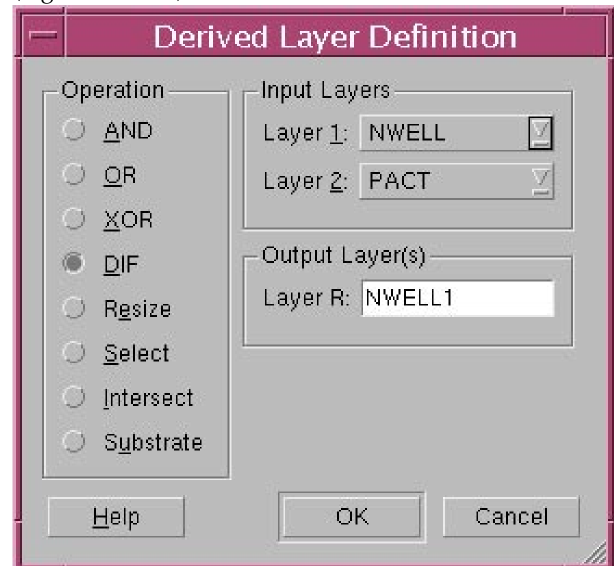


Figure 4. NWELL1 derived layer definition.

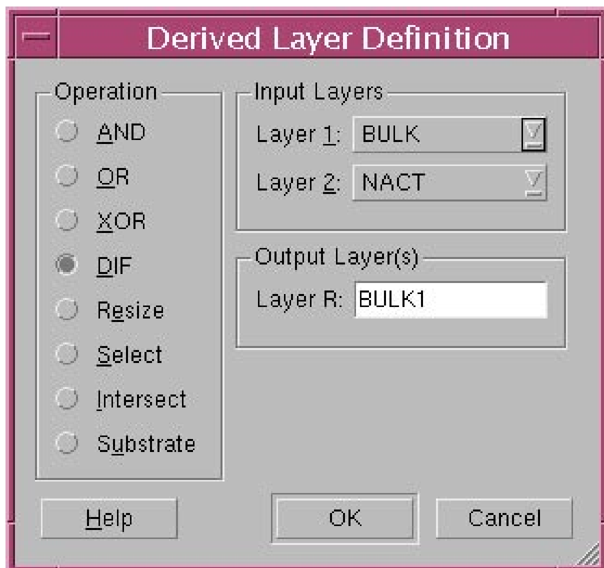


Figure 5. BULK1 derived layer definition.

By default ***STELLAR*** will name « Substrate » all the substrate region which does not belong to a defined region (Figure 1).

Techno file: connection setup

The connection is defined in the ***STELLAR*** techno panel. If there are layers that have to be connected to the substrate (CONT_BULK, CONT_WELL) then we have to use the connectivity panel as indicated in Figure 6.

Process Definition

The layers NWELL1, NBULK1 have to be defined in the Process panel of ***STELLAR*** using a specific key word: « Substrate_Partition » (Figure 7).

From the « Substrate_Partition », STELLAR builder will generate a plane surface with a thickness=0.

Note that labels attach to the substrate_Partition is the name of that layer used in the process panel. For example in Figure 7 we use BULK1 as a substrate layer and ***STELLAR*** will output in the spice netlist the capacitance between BULK1 and poly.

Name	Type	Material	Thickness
NWEL1	Substrate_Partition		
BULK1	Substrate_Partition		
oxyde02	Dielectric	oxide	0.5
POLY	Conductor	polysilicon	0.7
oxyde2	Dielectric	oxide	1
oxyde3	Dielectric	oxide	1
AIR	Dielectric	Air	4

Figure 7. substrate partition definition.

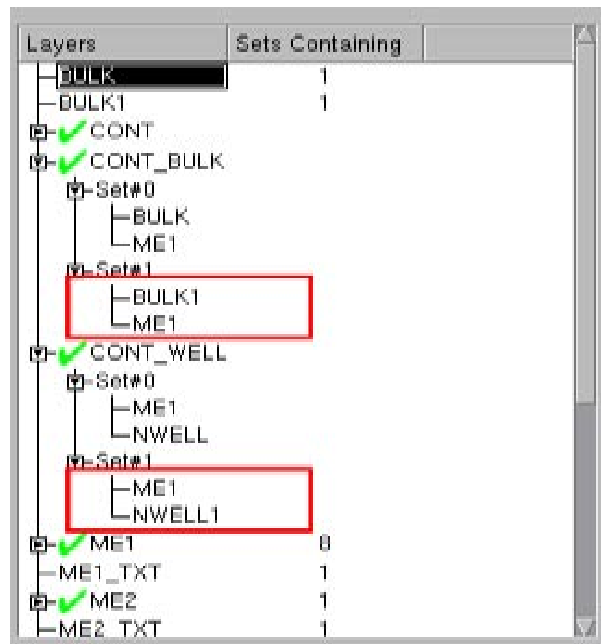
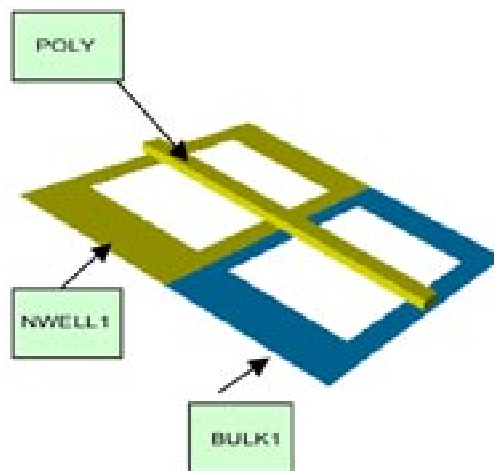


Figure 6. Substrate connectivity.

Example

We take an example as shown below :



The capacitance calculation without the substrate partition gives:

Final capacitance report (in F)- sorted

poly	substrate	1.471416e-14

The capacitance calculation with the substrate partition gives:

Final capacitance report (in F)- sorted

poly	substrate	1.093147e-14
BULK1	poly	1.901284e-15
NWELL1	poly	1.881415e-15

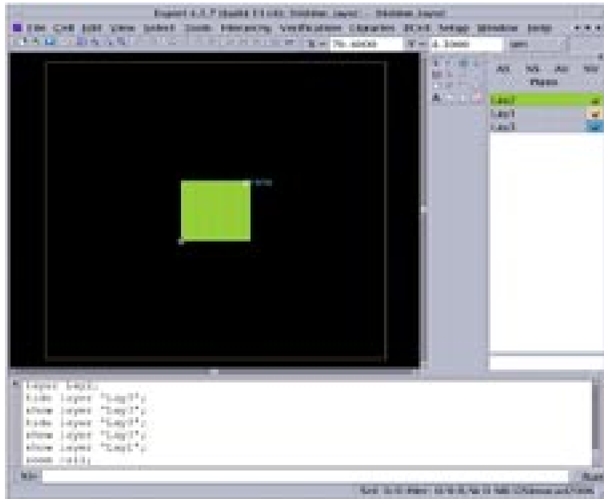


Figure 8. Layout under study.

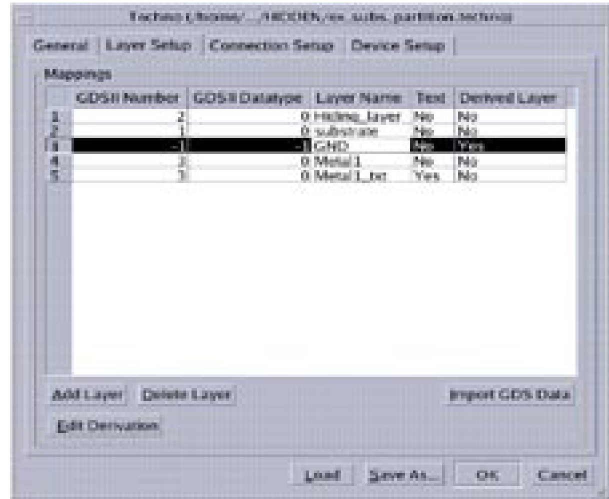


Figure 9. Layer setup definition

III Application: Hiding layer

We want to calculate capacitances using the substrate partition feature of ***STELLAR*** and compare to ***CLEVER*** for validation purpose. The layout used for this study is shown in Figure 8.

There are 3 mask layers identified in the ***STELLAR*** techno panel (Figure 9). We want to calculate the capacitance between the Metal1 plate and the substrate without taking into account the overlap capacitance between the Metal1 plate and substrate. Note that layer 2, named hiding_layer, was specifically design in order to define the substrate partition. Indeed GND layer is defined in the techno panel (Figure 9) as a derived layer: GND=substrate - hiding_layer and will be used in the process panel as a substrate_Partition (Figure 10).

Note that from the « Substrate_Layer », (GND) ***STELLAR*** builder will generate a plane surface with a thickness=0 as shown in Figure 11.

The capacitance calculation with the substrate partition gives:

Final capacitance report (in F)- sorted

plate GND 4.81e-15

The capacitance calculation without the substrate partition gives:

Final capacitance report (in F)- sorted

plate substrate 3e-14

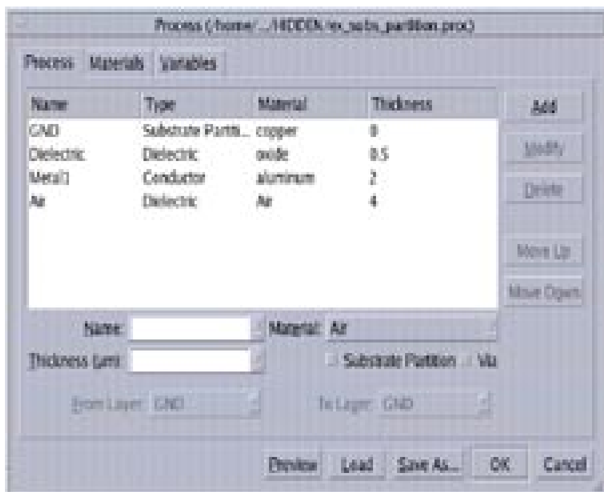


Figure 10. Process panel showing the use of GND layer as a substrate partition layer type.

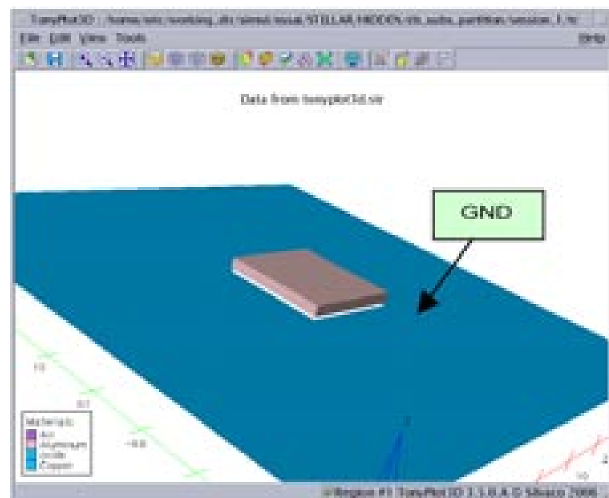


Figure 11. 3D structure without oxide.

Figure 12. ***CLEVER*** input deck.

Figure 13. Substrate simulated in ***CLEVER*** . Note the presence of dielectric with a very low permittivity.

In this last case the overlap capacitance between the plate and the substrate was calculated increasing significantly the overall capacitance.

Comparison with *CLEVER*

We wanted to compare ***STELLAR*** results with ***CLEVER*** for validation purpose. For that we obviously used the same layout (Figure 8) and the same process. What we did in ***CLEVER*** to mimic the substrate partition feature used in ***STELLAR*** is shown in Figure 12. We use the metal1 mask to define a region in the substrate that we fill with a dielectric and on top of that we set a very low permittivity for this dielectric. The resulting 3D structure is shown in Figure 13.

The capacitance calculation for the standard structure gives:

Final capacitance report (in F)- sorted

plate	**substrate**	**3.08e-14**

The capacitance calculation in ***CLEVER*** which mimic the ***STELLAR*** substrate partition:

Final capacitance report (in F)- sorted

plate	**GND**	**4.59e-15**

The difference between ***CLEVER*** and ***STELLAR*** results are less than 5%.

Conclusion

We have shown that ***STELLAR*** is able to define different substrate regions. This feature is useful to avoid the calculation of some capacitances like Cox already present in the spice compact model or to separate the Vdd areas from the grounded substrate.

Three Dimensional Electro-Thermodynamic Analysis for GaN Light Emitting Diodes

Abstract

Improvement in temperature characteristics of GaN LEDs is important for realizing reliable devices operating at high temperatures. In this article, the thermal characteristics of GaN LEDs have been analyzed by using the ***ATLAS*** three dimensional thermal conduction model and thermal heat model. Maximum operation temperature has also been calculated. It was shown that the distribution of lattice temperature using the conventional structure.

1. Introduction

Nitride-based compound wide bandgap semiconductor materials such as GaN, InGaN and AlGaN or AlInGaN have been attract the greatest interest as materials for high performance light emitting devices in the blue to ultraviolet wavelength region light emitting diodes(LEDs), and laser diodes. These LEDs are used extensively as back lighting in liquid-crystal displays, traffic light lamps, and indoor or outdoor displays.

Analysis of thermal characteristics for GaN LEDs have been carried out by using the three-dimensional thermal conduction model. In this article, three-dimensional analysis introduced the thermal conduction model and the self-heating effect as well.

2. Simulation Model

The polarization of the wurtzite materials with built-in electrical fields in semiconductors is characterized with two components, spontaneous polarization, Psp, and piezoelectric polarization, Ppi.

Polarization in Wurtzite Materials

$$P_t = P_{SP} + P_{pi} \qquad \text{eq. 1}$$

$$P_{pi} = 2\frac{a_s - a_0}{a_0}\left(E_{31} - \frac{C_{13}}{C_{33}}E_{33}\right) \qquad \text{eq. 2}$$

where E31 and E33 are piezoelectric constants, and the a0 parameter is the lattice constant of the material layer in question (as is the substrate value).

Self Heating Effect

The heat flow equation added to the primary equation such as poisson and carrier continuous equation for the device characteristics.

$$C\frac{\partial T_L}{\partial t} = \nabla(\kappa \nabla T_L) + H \qquad \text{eq. 3}$$

$$C = \rho C_P \qquad \text{eq. 4}$$

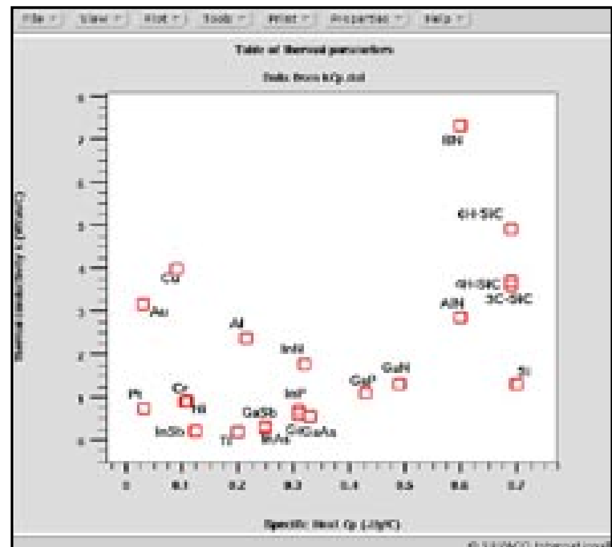


Figure 1. Thermal conductivity and specific heat for metal and semiconductor materials

where C is the heat capacitance per unit volume, and k is the thermal conductivity, and H is the heat generation, Tl is the local lattice temperature and Cp is the specific heat and ρ is the density of the material.

Heat Generation

When carrier transport is handled in the drift-diffusion the heat generation term, H, used in equation 3 has

$$H = \left[q\frac{|\vec{J}_n|^2}{\mu_n n} + q\frac{|\vec{J}_p|^2}{\mu_p p}\right] + q(R-G)\left[\phi_p - \phi_n + T_L(P_p - P_n)\right] - qT_L\left(\vec{J}_n \nabla P_n + \vec{J}_p \nabla P_p\right) \qquad \text{eq. 5}$$

$$\left[q\frac{|\vec{J}_n|^2}{\mu_n n} + q\frac{|\vec{J}_p|^2}{\mu_p p}\right]$$ is the Joule heating term

$$q(R-G)\left[\phi_p - \phi_n + T_L(P_p - P_n)\right]$$

is the Recombination and Generation Heating and Cooling term

$$-qT_L\left(\vec{J}_n \nabla P_n + \vec{J}_p \nabla P_p\right)$$ accounts for the Peltier and Thomson Effects.

3. Simulation Results for Thermal Resistance

A schematic three dimensional structure shows in Figure 2. This structure is the conventional LED structure GaN-sapphire. The structure combinated with GaN/AlGaN/InGaN/GaN on sapphire.

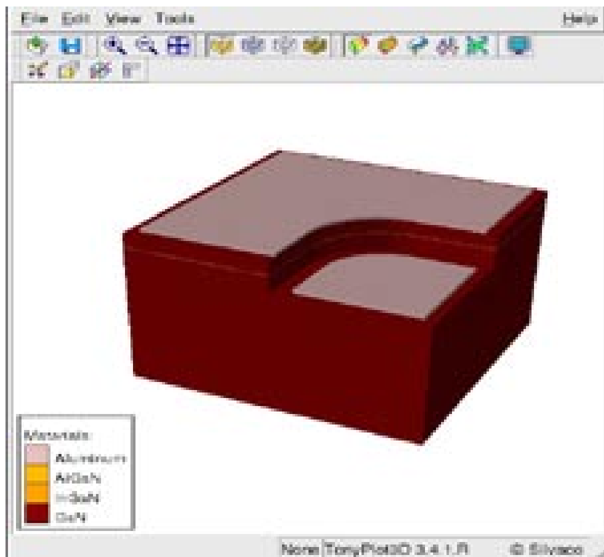


Figure 2. Simulated GaN LED structure.

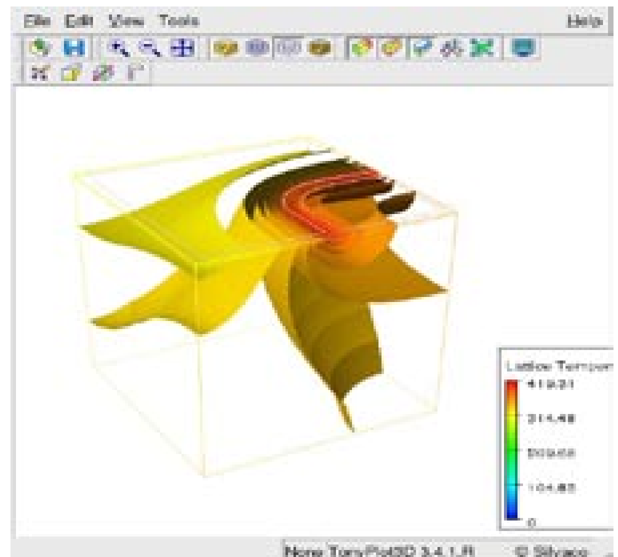


Figure 3. Lattice Temperature Distribution on the LED at Anode Current 600mA.

Based on the calculation results, the thermal resistance Rth of the device was derived using the following equation,

$$\left(\vec{J}^{U}_{tot} \cdot \vec{s}\right) = \frac{1}{R_{th}}\left(T_L - T_{ext}\right) \qquad \text{eq. 6}$$

$$R_{th} = \Delta T_{act} / Q_{total} \qquad \text{eq. 7}$$

where the ΔTact is temperature rise in the active layer and Qtotal is the total heat generation. The definition is practical because the entire input power is included in Qtotal. However, it should be noted that the thermal resistance calculated by Eq.6 is a lumped value and differ depending on the spacial distribution of the heat source.

In Figure 3, the maximum temperature 419 K distributed around the active layer and the edge of the mesa. On two dimensionally, the lattice temperature shows along the active layer vertically.

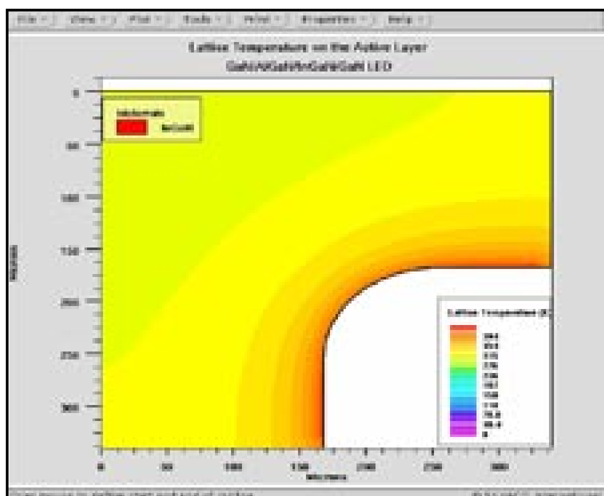
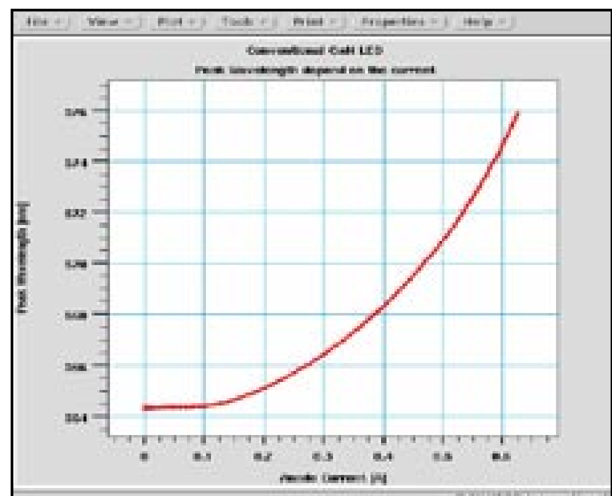


Figure4. Lattice Temperature on the center of the InGaN active layer on 2 dimension at Anode Current is 600mA.

In Figure 5, the junction heating effect on LEDs can be further interpreted using the variation injection currents. When the driving current increased from 0.2 to 0.6A, the peak wavelength of LEDs showed a drastic red shift from 565nm to 576nm.

4. Conclusions

Thermal characteristics of GaN LEDs have been analyzed by using the ***ATLAS***, three-dimensional thermal heat flow and heating model. The dependence of the thermal resistance and the current flow effect is more effective the maximum operation temperature Tmax. This depend on the conductivity of material and device structure. This operation temperature depend on the injection current makes the peak wavelength red shift.



.Figure 5. Peak Wavelength as a function of injection current.

Hints, Tips and Solutions

Sung Wong, Senior Applications and Support Engineer

Q. How to obtain a stable grid and smooth doping profile in non-planar a-Si TFT using *ATHENA/Elite*?

A. Silvaco process and device simulation tools have been successfully used for many TFT applications. It has been shown that if accurate density of state distributions are specified the transfer characteristics of TFT devices show good agreement with experiments. The typical configuration of TFT includes a non-planar n+ doping source/drain region around the metal gate. Such a non-planar structure could be simulated only by the process simulator ***ATHENA*** because ***ATLAS*** cannot generate the regions with rounded shapes.

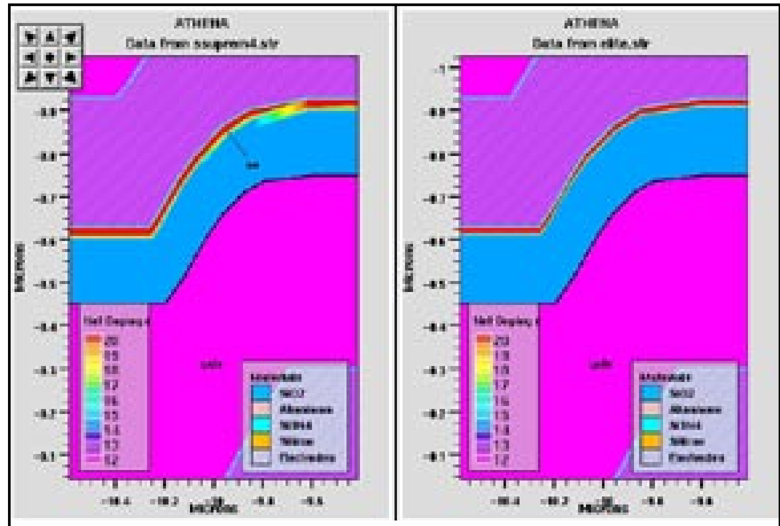


Figure 1. Ssuprem4 n+ doping v.s Elite doping profile

The accuracy of ***ATLAS*** device simulation strongly depends on grid quality and uniformity of doping along the surface of a-Si region. The internal ***SSuprem4*** deposition algorithm does not produce a smooth grid and consequently uniform doping. To overcome this difficulty the advanced topography simulation module of ***ATHENA*** must be used for a-Si deposition step. ***Elite*** produces much better grid and avoids non-uniform doping as seen in the left plot of Figure 1.

Figure 2 shows that experimentally proved IV-curves can only be obtained when ***Elite*** module is used for simulation of the critical a-Si deposition step. If ***Elite*** is not used the reverse biased trend of the IV-curve disappears which means that these characteristics are very sensitive to the grid and doping quality. Therefore, we strongly recommend to use ***Elite*** deposition for simulation of non-planar TFT devices.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department
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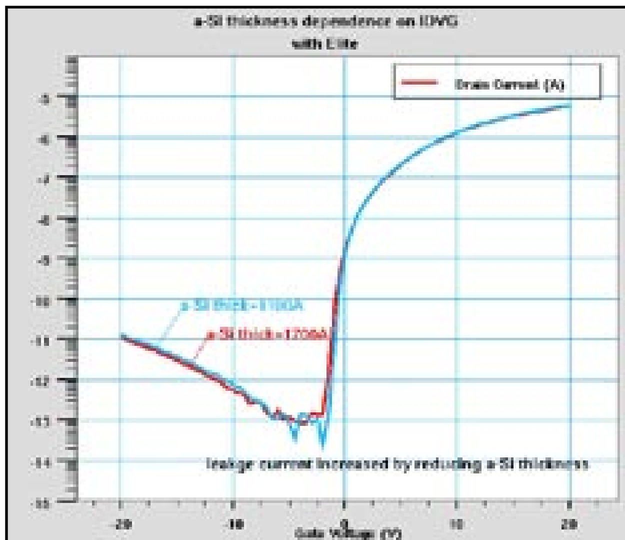

Figure 2.(experimental data is omitted) The left plot shows leakage current increase with a-Si thickness when simulating with ELITE. The right plot does not show such a behavior if ELITE is not used.

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