# Simulation Standard

Connecting TCAD To Tapeout

A Journal for CAD/CAE Engineers


## Capacitance Coupling Calculation of IPS mode TFT-LCD Using *CLEVER*

### Introduction

The increasing demand of the TFT-LCD industry has lead to a rapid growth in display size and resolution. The higher cell packing density results in a narrowing viewing angle and image degradation due to electrical coupling between the data bus lines and display electrodes. This "crosstalk" therefore becomes a serious limitation. The in-plane switching(IPS) mode has been used as an excellent technology solution for realizing extremely wide viewing angles. The IPS-mode TFT-LCD has however a drawback of lower aperture ratio than the twist nematic(TN)-mode TFT-LCD when the pixel size is larger than about 140 dots per inch[1].

If the electrode structure of the IPS implementation is not properly designed, it will result in a small aperture ratio and a visible crosstalk distribution.

It is well known that the crosstalk caused by parasitic capacitive coupling between driving electrodes and data-bus lines could result in image degradation

The crosstalk can be reduced by a thick dielectric film such as SiNx between the data-bus line and the common electode of the IPS structure.

It is reported that a low dielectric constant organic passivation film is a good candidate to reduce crosstalk rather than the same thickness of an inorganic layer considering manufacturing cost. A major effort to reduce the crosstalk of the IPS mode TFT-LCD is to optimize the electrode configuration to shield the pixel electrodes and the display area from the varying data-line voltages

As a result, the IPS mode is more sensitive to process variations not just the LC itself. So variation in array process, electrode width, height and surface topology must be accurately token into account.

Consequently, the optimum thickness of the organic layer or inorganic insulator layer is very important for both the cost and performance of the LCD-TFT display.

In this article we will show that ***CLEVER*** gives a good agreement with measuremt for TFT-LCD pixel structure and have the capability to study crosstalk effects of IPS-mode TFT-LCD.

### *CLEVER* for Flat-Pannel Display

***CLEVER*** has been successfully demonstrated very accrurately to extract parasitics even at very deep-submicron era. ***CLEVER*** vconsider aspect ratio which is the mesh quality of active rand pixel region. Also gate metal pattern with angle and undercut can be simulated. So accurate shape of metal and film topology using advanced ***CLEVER3D*** process simulation is indispensable to predict accurate IPS TF-LCD parasitic capacitance and so crosstalk. Table 1 show good agreement with measurement of different common-pixel electrode structures.

| | meas(total)(fF) | CLEVER(Clc/Cdc/Clc+Cdc) | | |
|---|---|---|---|---|
| Ref | 99.6 | 51.0 | 53.4 | 104.4 |
| 1 | 93.46 | 41.2 | 52.6 | 93.8 |
| 2 | 91.25 | 36.5 | 54.3 | 90.8 |

Table 1. Common-Pixel & Common-Data Capacitance with different Common-Pixel Electrode Spacing(accuracy=5%)

*liquid crystal permittivity = 12.1

Ref/1/2: Pixel-Common space is increasing order.

*Continued on page 2 ...*

*INSIDE*





SILVACO INTERNATIONAL

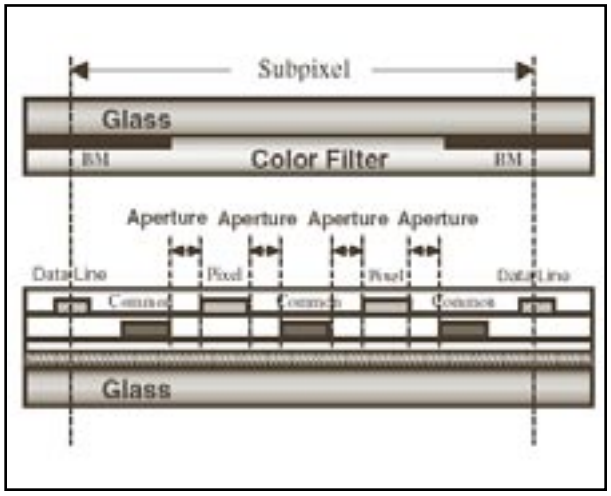


Figure 1. Conventional IPS mode TFT-LCD vertical structure.

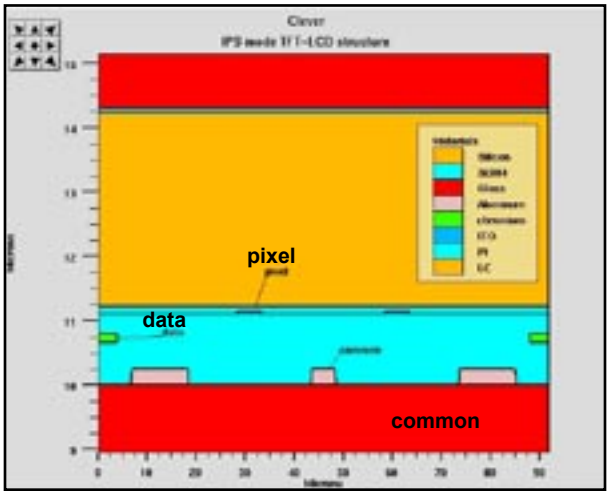


Figure 2. ***CLEVER*** structure – see the taperd shape of common electrode.

## Couping Capacitance Calculation of IPS Mode TFT-LCD Using *CLEVER*

Coupling voltage of the pixel electrode dVp is defined as,

$$\Delta V_p = \frac{C_{pd1}\Delta V_{d1} + C_{pd2}\Delta V_{d2}}{C_{LC} + C_{pd1} + C_{pd2} + C_{pg1} + C_{pg2} + C_{po} + C_{GS} + C_{st}} \quad (1)$$

Compared to TFT-TNs, the denominator of eq.(1) is small because all the electrodes are arranged on the same side of the substrate. Therefore in order to suppress ΔVp in the IPS mode TFT-LCD, $C_{pd1}$ and $C_{pd2}$ been to be smaller than those of the TN mode TFT-LCD.

Capatitive coupling ratio, CCR is a good approximation representing the degree of crosstalk.

$$CCR = \frac{C_{pd1} + C_{pd2}}{C_{LC}(V) + C_{pd1} + C_{pd2} + C_{pg1} + C_{pg2} + C_{po} + C_{GS} + C_{st}} \quad (2)$$

$C_{lc}$: liquid crystal capacitance

$C_{pd1}/C_{pd2}$: coupling capacitance from the adjacent data line and the data-line to the pixel electrode

$C_{pg1}/C_{pg2}$: coupling capacitance from the adjacent gate line and gate line to pixel electrode

$C_{po}$: coupling capacitance from the pixel to common electrode in the array substrate

$C_{gs}$: TFT gat-to-source parasitic overlap capacitance

$C_{st}$: storage capacitance

With respect to the voltage dependent Clc, we can consider the permittivity of LC material, contact when constant field is applied.

The data-pixel capacitance and data-common capacitance of various IPS structrure was simulated using ***CLEVER***[4].

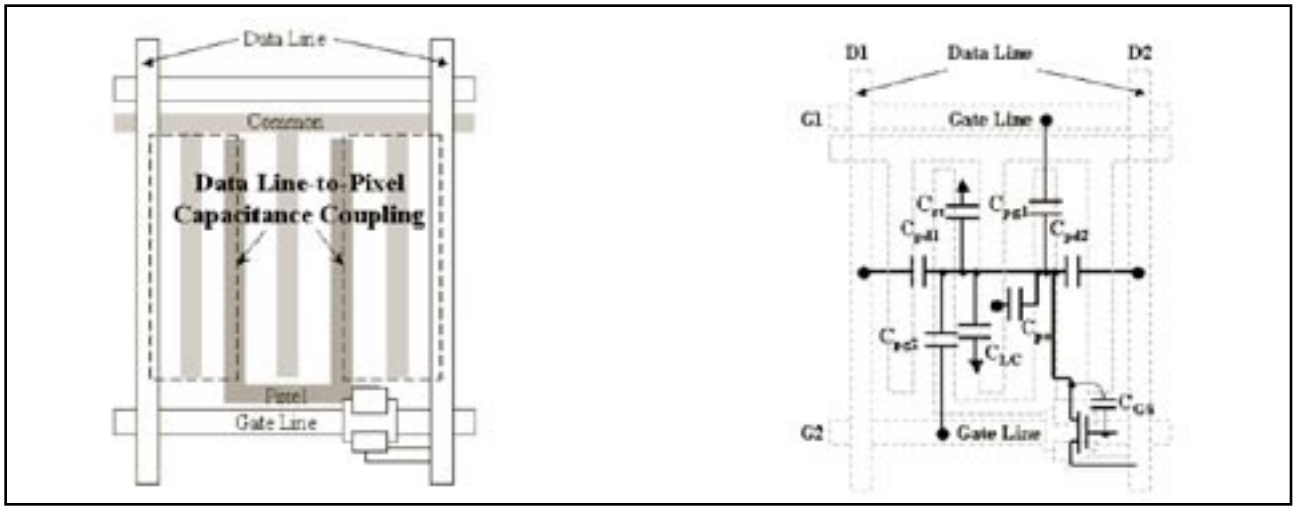


Figure 3. Equivalent circuit of pixel.

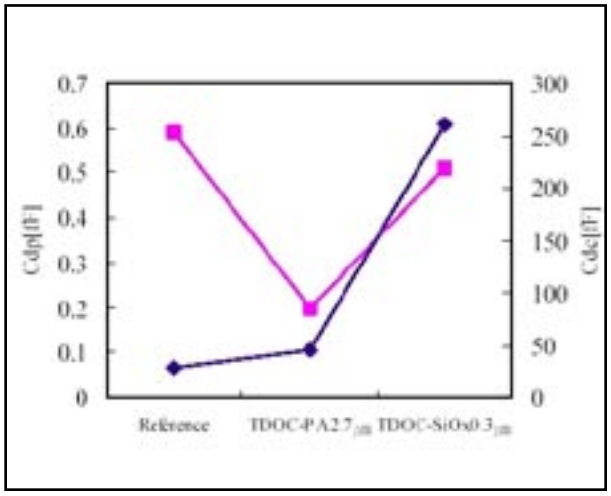


Figure 4. Coupling cap. of IPS structure.

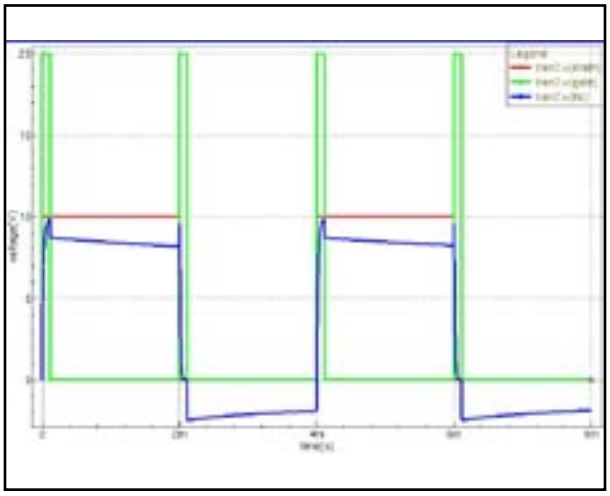

Figure 5. Example spice input file to pixel simulation.

## RC Delay

From extracted parasitics netlist, we can simulate the RC delay effect across data line directly using ***SmartSpice*** simulation. In this simulation, only one pixel was simulated.

```
M1  drain  gate  ito    nTFT  w=49u  l=38.5714u
As=1274p Ad=2439p Ps=150u Pd=610u Nrs=0.142857
Nrd=0 geo=0
C1   substrate gate   7.0162449e-14
C2   substrate drain  1.815544e-14
C3   substrate data   2.0479665e-14
C4   substrate ito    1.4275399e-13
C5   gate   drain  1.169502e-13
C6   gate   data   4.7088442e-14
C7   gate   ito    4.6344247e-13
C8   drain  ito    4.1971866e-15
C9   data   ito    7.8982418e-15

lib "tft.lib" ntft
vg gate 0 dc 20 pulse 0 20 0 1u 1u 108u 2m
vd drain 0 dc 10 pulse 0 10 0 1u 1u 2m 4m
vcom com 0 dc 5

mntft drain gate ito ntft w=20u l=5u
cst ito com 1.06p
re ito co 1.28k
c0 co lc 317f
rlc lc com 10g
clc lc com 125f

cgs gate ito 20f
cgd gate drain 20f

.tran 0.1u 8m
.save v(drain) v(gate) v(ito)
.end
```

Figure 6. SmartSpice simulation of pixel.

## Conclusion

The ***CLEVER's*** accurate 3D field solver can be applied to TFT-LCD design to predict origin of various coupling capacitance and so crosstalk.

The process variation such as passivation layer and the configuration of electrodes is easily simulated by ***CLEVER***. From the integrated prospect point of view, Silvaco's ***CLEVER-SmartSpice*** supply good framework for future full-panel design.

## Appendix

(1) J.S. Lin , Jpn J.App. Phys. Vol43, No.4A, 2004, p1476-1480

(2) Y. Z. Muju Li, IEEE Trans. ED vol.48, No.2, Feb. 2001,p218

(3) Webster E. Howard, IEEE Trans. ED, vol.36,No.9, Sept. 1989, p1938

(4) H.S. Chang, LCD R&D Center, LG-Philips LCD, Korea IDW' 2005

# New Parasitic Capacitance Modeling in *Hipex-C*

## Introduction

In deep submicron technology, conduction layers have widths much smaller than their thicknesses (see Figure 1). This makes edge parasitic capacitance effects more dominant than plate capacitance.

In a multi-body system, neighboring conductors may capture some or all of the electrical fields lines emanating from a particular conductor. These field lines would otherwise terminate else where. This phenomenon is called charge sharing, which plays an important role in modeling parasitic capacitances.

This article presents new approaches to dealing with charge sharing and vertical shielding in Silvaco's parasitic capacitance extraction tool, ***Hipex-C***. The three main commands in ***Hipex-C***, `FRINGE`, `LATERAL` and `AREA`, cover all of the capacitance calculation requirements that one would expect from a industry leading capacitance extraction tool. `FRINGE` enables edge-to-body, `LATERAL` enables edge-to-edge and `AREA` enables plate capacitance modeling.

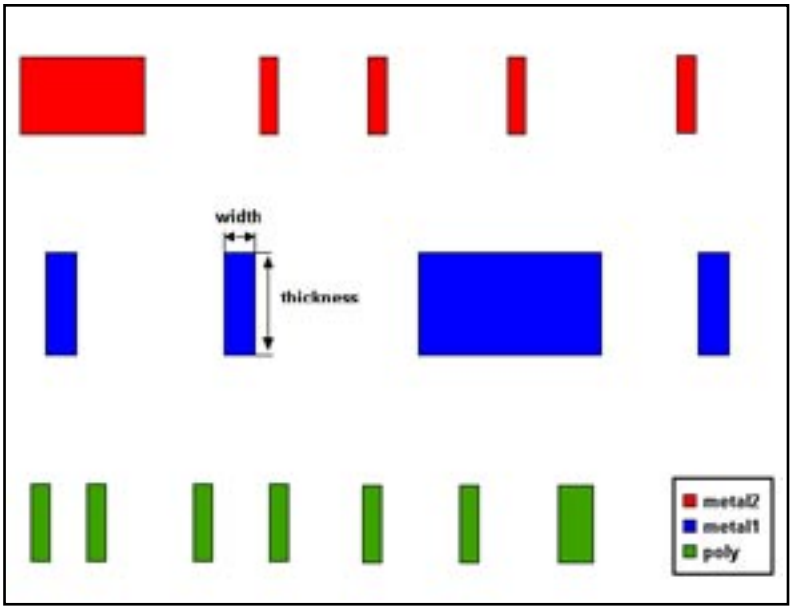


Figure 1. Cross-sectional view of a chip.

All the commands allow one to specify different capacitance coefficients for different vertical configurations of the primary layers to account for charge sharing effects. The layers above or below or both the primary conductor(s) define the vertical configuration.

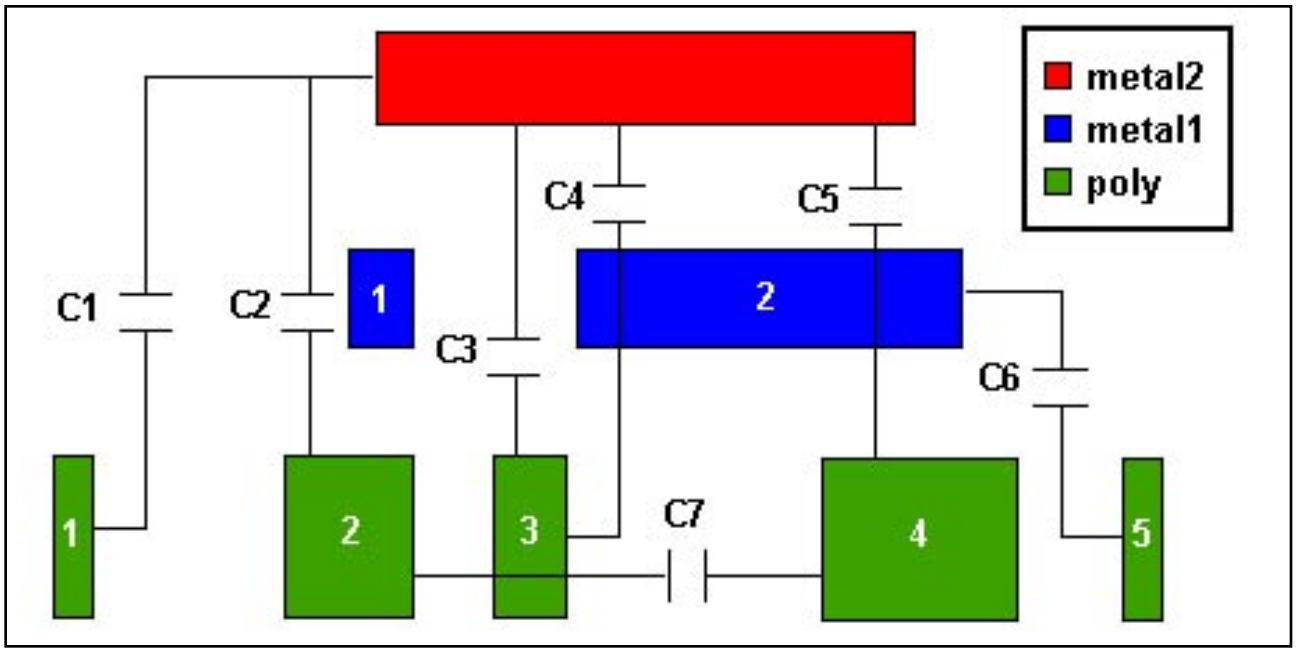


Figure 2. Vertical shielding example (cross-sectional view)

## Vertical Shielding

Vertical shielding is caused by the vertical order of layers. When more than two conduction layers overlap, the inside layers shield the capacitance effects between the outer layers, Figure 2. demonstrates the effects of vertical shielding.

Note the following vertical shielding effects for primary layers `metal2` and `poly`:

- The first `metal1` shape is shielding the `metal2` edge from the edge of the first `poly` shape (lateral C1) and the body of the second `poly` shape (fringe C2)
- The second `metal1` shape is shielding the edge of the third poly shape from the `metal2` body (fringe C4) and the bodies of the `metal2` shape and the fourth `poly` shape from each other (area C5)

For lateral capacitance, a primary layer shape can shield another primary layer shape:

- The third `poly` shape is shielding the edges of the second and fourth `poly` shapes from each other (lateral C7)
- The fourth `poly` shape is shielding the `metal1` edge from the edge of the fifth `poly` shape (lateral C6)

The only capacitor, which is not shielded, is area C3.

In older versions of ***Hipex-C***, the user has had to specify correct shielding layers in the `/INSIDE_LAYERS` option for each capacitance statement. For example,

```
CUP AREA met2 poly 1.08e-5 /INSIDE_LAYERS=
met1;
CUP FRINGE met2 poly 1.2e-4 /INSIDE_LAYERS=
met1;
CUP FRINGE poly met2 8.7e-5 /INSIDE_LAYERS=
met1;
CUP LATERAL met2 poly /K=9.01e-6 /MAX_DISTANCE=3
/INSIDE_LAYERS=met1;
```

In the latest version of ***Hipex-C***, we have introduced the new statement for specifying vertical order of conduction layers, `CUP ORDER`. It lists the layers from bottom to top.

For example,

```
CUP ORDER bulk, diff, poly, met1, met2, met3,
met4, met5, met6;
```

This statement determines shielding layers for a given pair of primary layers. In the example above, layers `met2` and `met3` are shielding layers for any type of capacitance associated with `met1` and `met4` layers. This kind of vertical shielding occurs automatically.

The `/INSIDE_LAYERS` option is also available for specifying extra shielding layers. This option is especially useful for lateral capacitance statements, in which a layer can be both primary and shielding layer at the same time (see capacitors C6 and C7 in Figure 2).

For example:

```
CUP LATERAL met1 /INSIDE_LAYERS=met1 /
K=7.0526e-5 /MAX_DISTANCE=1.245 /SHIELD_FAC-
TOR=0.1;
CUP LATERAL met2 met1 /INSIDE_LAYERS=met2,
met1 /K=4.58e-6 /MAX_DISTANCE=0.6 /SHIELD_
FACTOR=0.14;
```

The `/SHIELD_FACTOR` parameter controls the effect of shielding on lateral capacitances. The default value is zero, which avoids lateral capacitance when there is shielding. ***Hipex-C*** always avoids the shielded area and fringe capacitances.

## Charge Sharing

In a multi-body system, any neighboring conductors can influence the capacitance associated with the two primary conductors. Older versions of ***Hipex-C*** as well as the latest version can model the charge sharing from a layer edge between another layer body and the same layer lateral edge. Figure 3. illustrates these charge sharing effects. As the distance D to lateral edge decreases, the lateral capacitance `C1` and `C4` increases, while the fringe capacitance `C2` and `C3` decreases.

The built-in lateral and fringe capacitance equations show these qualitative dependencies in the quantitative manner:

```
C_lateral = n1 * L / (D + n2)^n3
C_fringe  = n1 * L * (1 - exp(-n2 * (D + n3)))
```

Here, `L` is the length of an edge; `D` is the lateral distance; `n1`, `n2`, and `n3` are the specified non-negative constants.

The latest version of ***Hipex-C*** can effectively model the charge sharing effects caused by the presence of layers geometry above and below the primary layer(s). Using the `/OUTSIDE_LAYERS` option with the capacitance statements, you can specify different capacitance coefficients for each vertical configuration of the primary conductors. The layers above and below, if applicable, the primary conductors define the vertical configuration.

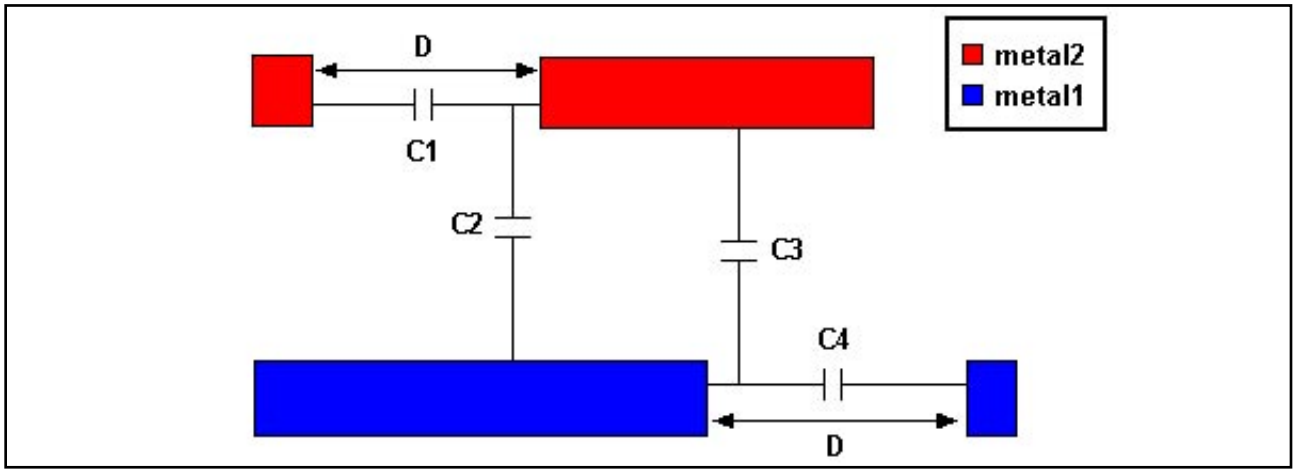


Figure 3. Charge sharing with lateral edge (cross-sectional view).

When ***Hipex-C*** encounters a capacitance for the primary layers, it first looks for a statement with the `/OUTSIDE_LAYERS` option that matches the surrounding layers. If the tool finds an exact match, then it uses the coefficients for the statement to compute the capacitance. If ***Hipex-C*** does not find a match, it uses the capacitance coefficients for a statement without an `/OUTSIDE_LAYERS` option. Therefore, statements without `/OUTSIDE_LAYERS` options provide the default coefficients for any vertical configuration of the primary layers.

For primary layers `layer1` and `layer2`, you can specify one or two outside layers:

```
\OUTSIDE _ LAYERS = layer3

\OUTSIDE _ LAYERS = layer4

\OUTSIDE _ LAYERS = layer3, layer4
```

Here, `layer3` is below `layer1` and `layer4` is above `layer1`. For a `LATERAL` statement, there might be only one primary layer, `layer1`.

Figure 4. demonstrates different vertical configurations of the two primary layers. Capacitance effects for the primary layers, `layer1` and `layer2`, are shown in red. Charge sharing effects with the outside layers, `layer3` and `layer4`, which lessen the capacitance effect, are shown in black.

The statements corresponding to the vertical configurations shown in Figure 4 are listed as follows:

```
a) CUP FRINGE layer1 layer2 /
   OUTSIDE _ LAYERS= layer3

b) CUP FRINGE layer1 layer2 /OUTSIDE _ LAYERS=
   layer4

c) CUP FRINGE layer1 layer2 /OUTSIDE _ LAYERS=
   layer3, layer4

d) CUP LATERAL layer1 layer2 /OUTSIDE _ LAYERS=
   layer3, layer4

e) CUP LATERAL layer1 /OUTSIDE _ LAYERS=layer3,
   layer4
```

## Conclusion

New version of Silvaco's ***Hipex-C*** tool provides effective means for modeling vertical shielding and charge sharing effects. The user can account for different patterns of primary layers by specifying capacitance coefficients for each pattern.

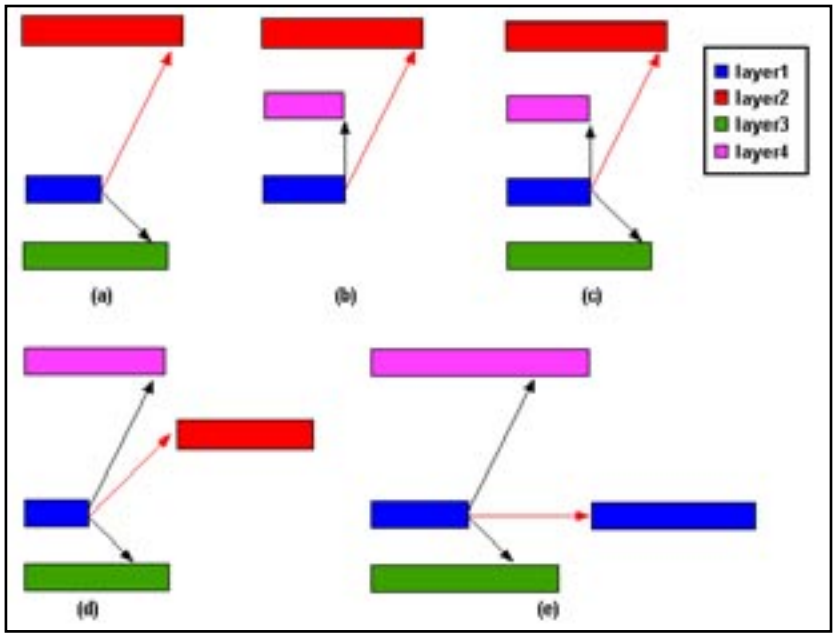


Figure 4. Charge sharing with outside layers geometry (cross-sectional view).

# *Expert*: Layout Versus Layout (LVL) Comparison

## Introduction

The functionality Silvaco's Layou Editor, ***Expert,*** has recently been expanded with the new feature called Layout Versus Layout comparison (LVL) .

LVL is available as a separate window called by menu commands:

- Verification/"Layout vs. Layout (LVL)"

- View/"Dock Windows"/ "Layout vs. Layout (LVL)"

It is also possible to open an LVL window from the cell context menu in "Project Tree" window by clicking the right mouse button on any two selected cells.

LVL functionality is also used in the "Cell Name Collision" window which is opened if there are cell name collisions during cell import/copy operations.

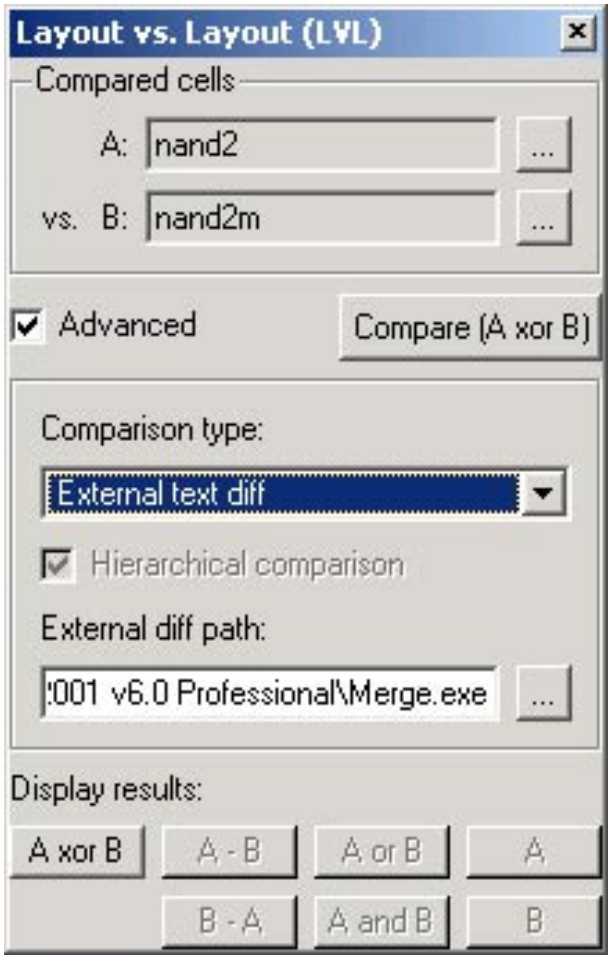


Figure 1. LVL Window.

## LVL Window

After an LVL window is opened and two cells are selected for comparison, user can use seven different buttons to display the differences between these cells.

"A xor B" – works like the symmetric difference (logical XOR)

"A - B" – works like the set difference (logical DIFF)

"B - A" – works like the set difference (logical DIFF)

"A or B" – works like the union (logical OR)

"A and B" – works like the intersection (logical AND)

"A" – displays cell A

"B" – displays cell B

"Compare (A xor B)" button works the same way as "A xor B" but it always clears all cache information calculated in the previous comparisons.

There are three available types of comparison:

- **Object-by-Object** (default), compares geometrical objects, specified in the layout editor. Two intersecting objects in the same layer are considered separately.
- **Geometry**, compares merged geometry. Two intersecting objects in the same layer are merged before comparison.
- **External text diff**, converts both cells to ***LISA*** script text and then starts specified external tool to compare these two flat text files. In many cases text comparison is much more easy to use. It allows to see clearly the small differences in the cells just by one or two mouse clicks. The lines of the generated ***LISA*** script are sorted by object type, coordinates, and other parameters, therefore you will always get the same text for cells with identical geometry.

  **NOTE**: Users can choose any external tool like "Araxis Merge" or WinDiff. See http://en.wikipedia.org/wiki/Diff for more information on freeware and commercial text diff tools.

  Figure 2 shows the results of such text comparison performed with "Araxis Merge" tool.

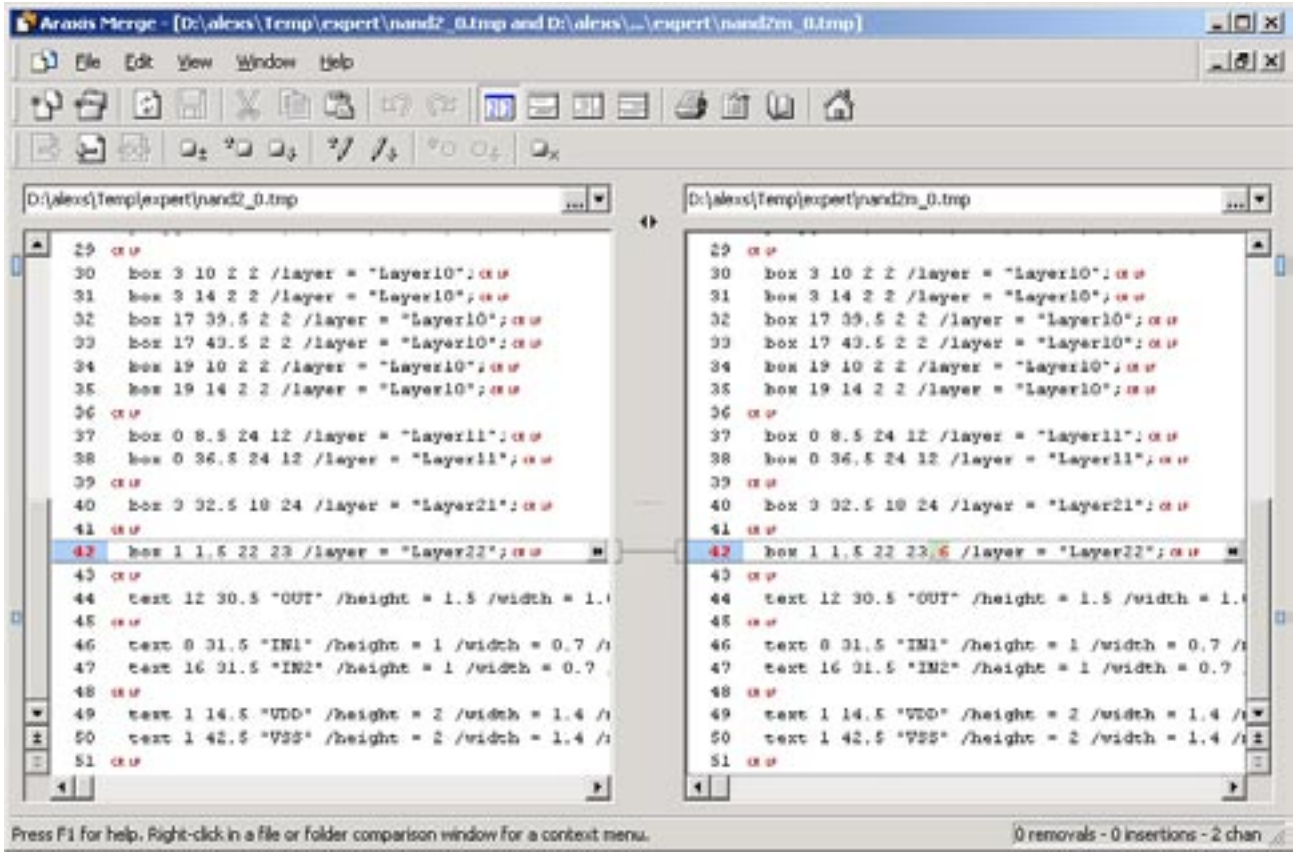


Figure 2. Text comparison results.

## Using LVL from Collisions Window

"**Skip All Similar Cells**" button performs quick object-by-object comparison and marks all similar cells as resolved (green checkboxes).

"**Compare (LVL)**" button displays the LVL tool window with two selected cells. After that the user can perform any necessary comparisons using this tool.

"**Automatically skip similar cells**" checkbox indicates that the quick cell comparison must be performed automatically on every opening of the collision dialog.

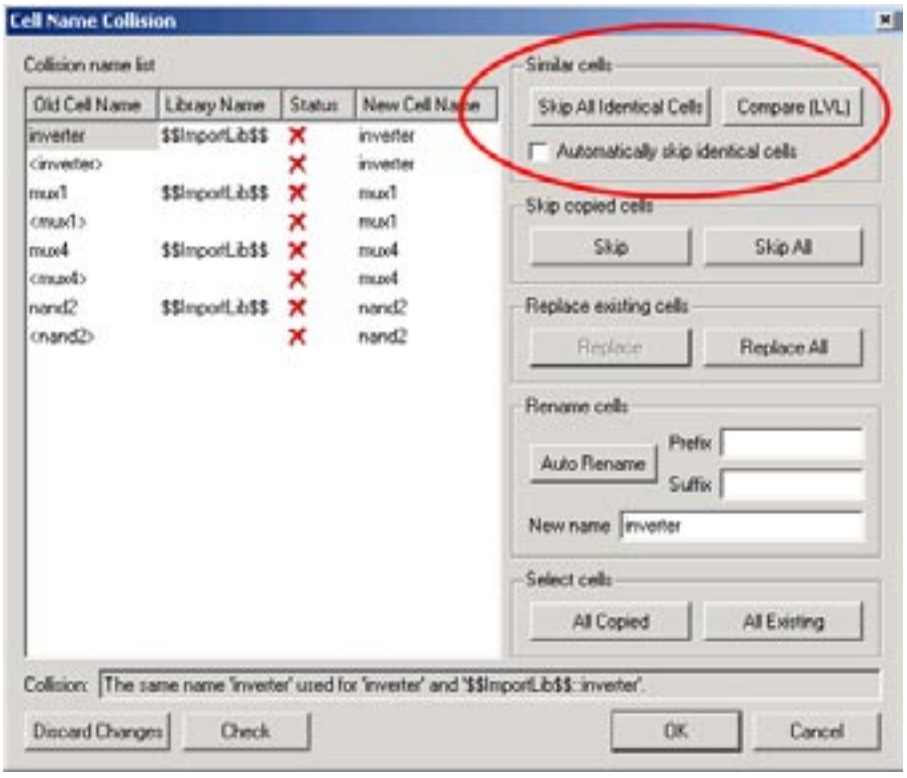


Figure 3. LVL functionality in "Cell Name Collision" window.

# *Expert*: Wiring

## Introduction

The wiring tool in ***Expert*** automatically creates the shortest wire connecting two points specified by the user. The created wire goes around any existing layout objects. It may lie in multiple layers (multi-wire) if the source and target points are on different layers or if the wire is shorter than the alternative single-layer wire case.

## Point to Point Routing

The simplest scenario of using the wiring tool is when the user just defines the source and destination points in some particular layer. The tool uses the Lee algorithm to find the shortest path around all obstacles. Width and styles for the new wire are initially taken from the layout technology but can easily be redefined.

Users may wish the resulting wire to come through some particular areas. In this case ***Expert*** allows defining additional intermediate points. In this case the resulting path will include these points. Users can also bound routing by some particular area. In this case the tool will not consider possible routes outside of this area.

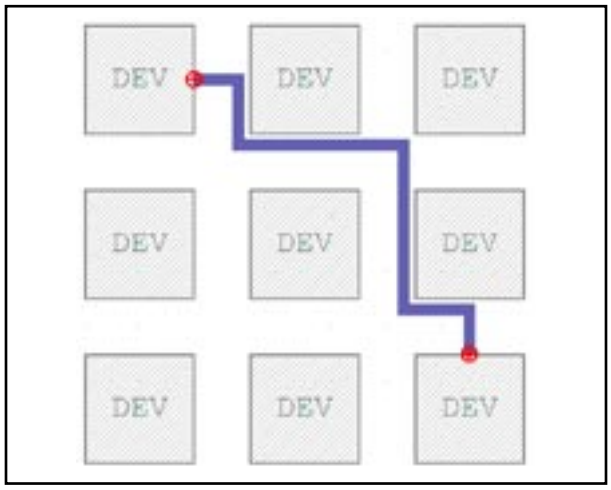

Figure 1.

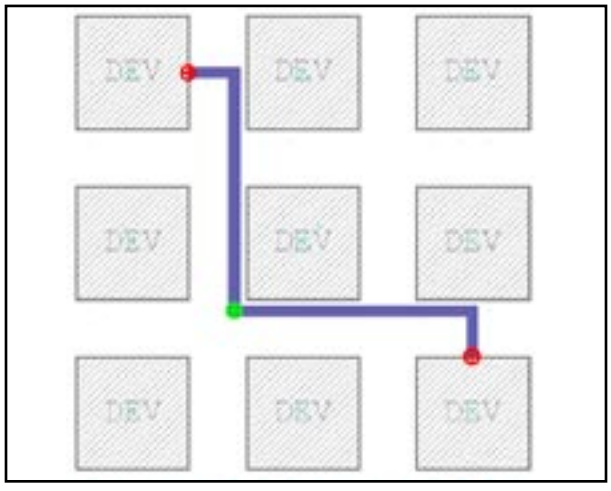

Figure 2.

If the technology file has contact definitions then ***Expert*** may perform wiring on multiple layers. The resulting path may be much shorter than the path on single layer because it can lie not only around obstacles but also above or below them.

In the case of multi-layer routing users have additional options to affect the resulting path: one might define source, destination and intermediate points on different layers, might define different width and styles for wires in different layers, or might fine-tune all options to get just the path the user needs.

## Routing Area

The tool finds a route in some particular routing area. This area can be calculated automatically or can be user defined. In either case it is better for the tool performance if the routing area is small. In automatic mode the tool first tries to find the route in the minimal possible area. If such attempts fail it expands the area as necessary and tries again. If the user wants to expand the area in any particular direction or restrict it to some rectangle, it is possible to define custom routing area and the tool will not consider possible routes outside of this area.

## Contacts

In order to be able to perform wiring in multiple layers the tool needs contacts to be defined in the technology file. ***Expert*** allows regular or parametric cells as contacts. Such cells could be in the current project or in external library.

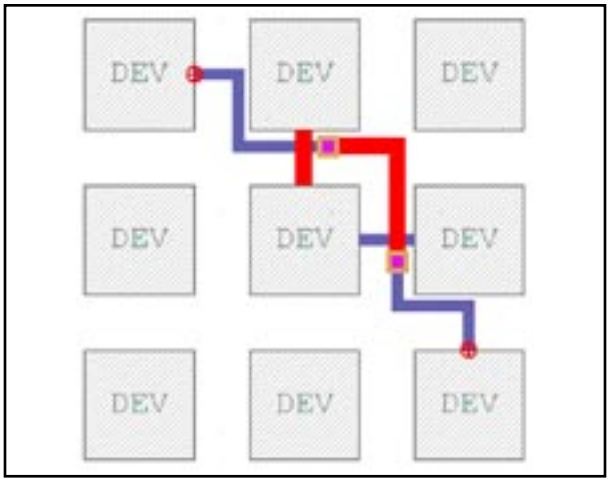

Figure 3.

# Calendar of Events

## March

| | |
|---|---|
| 1 | |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | DATE – Munich Germany |
| 8 | DATE – Munich Germany |
| 9 | DATE – Munich Germany |
| 10 | DATE – Munich Germany |
| 11 | |
| 12 | |
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| 15 | |
| 16 | |
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| 18 | |
| 19 | |
| 20 | |
| 21 | ISQED – San Jose |
| 22 | ISQED – San Jose<br>HEART – Tampa FL |
| 23 | ISQED – San Jose<br>HEART – Tampa FL |
| 24 | |
| 25 | |
| 26 | |
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| 31 | |

## April

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| 1 | |
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| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | GOMAC – Las Vegas, NV |
| 8 | GOMAC – Las Vegas, NV |
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## Bulletin Board

### *ISQED - International Symposium on Quality Electronic Design*

Ken Brock, Silvaco's VP of marketing participated in the evening panel titled "IP Creation and Use--What roadblocks are ahead or it is just clear and bumpy road?"

This panel debated the key technology and business issues that could disrupt the basic premises of cell-based design using IP blocks. The panel includes representatives of semiconductor manufacturers, EDA vendors, design managers, and IP providers.

Tets Maniwa, president of TM Associates, observed that if migration to new process nodes was slowing down, as he believed it was that might help stabilize the targets for which IP developers had to design. A similar stability, he noted, was coming from the increasing use of IP in FPGAs, which were themselves a relatively stable design target.

Ken Brock, vice president of marketing at Silvaco, added to Maniwa's thoughts about the pressures on IP developers. "The IP business has changed dramatically in the last couple of years," he said. "It is no longer possible to design a piece of hard IP that is foundry-independent.

### *DATE – Design, Automation, and Test in Europe*

Come and see Silvaco applications engineers demonstrate complete analog, mixed-signal, and RF IC design solutions. Silvaco supports this integrated design flow with process design kits (PDK) targeted to specific foundry processes.

*If you would like more information or to register for one of our our workshops, please check our web site at* ***http://www.silvaco.com***

# Hints, Tips and Solutions

Michel Blanchette, Applications Engineer

**Q. I have to send copies of my project layout to different members of my group, but they need to see only specific layers of the layout. How can I provide them only the required layers without having to alter my project?**

A. You can use a stream out mapping file, which simply specifies the layers that are going to be output in the gds file. This procedure does not alter your design nor require you to create different copies of your design.

Here are the steps to export the GDS using a mapping file.

Open the ELD project and choose the cell from which you want to stream out.

Go to the Layer Bar and press on "NV" for non-visible, then make visible only the layers you want to be part of the streamed out file.

Go to the menu View>>Layer View>>Layer lists>> and choose "Save visible layer list". This will open a window, which will allow you to save this visibility list in a mapping file (*.ell)

In order to use this mapping file in your stream out process, go to the menu Setup>>GDSII input/output>> and go to the tab GDS Output. At the top of the output tab, check the box "Use output layer remapping table" and specify the path to the (*.ell) file you previously saved.

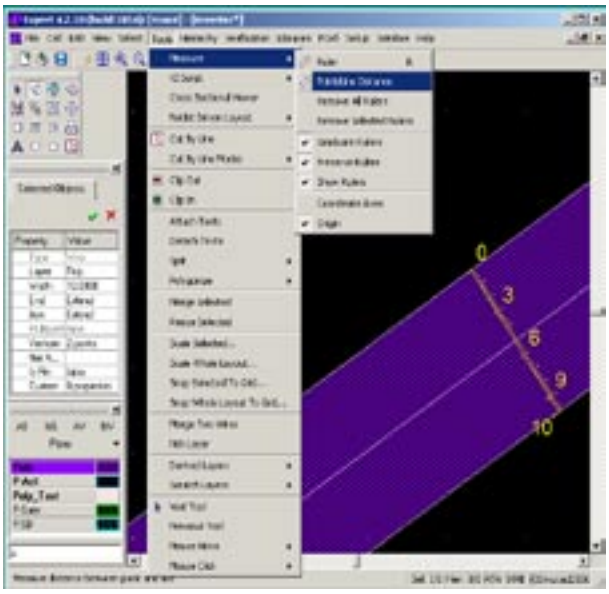

Figure 2. Measurement with Point/Line Distance Option.

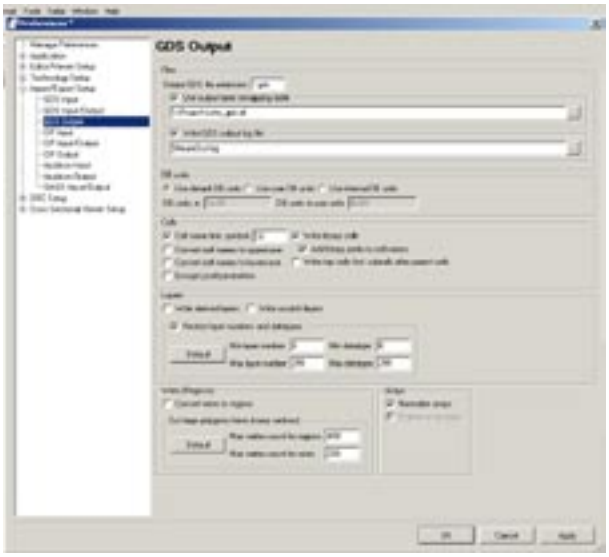


Figure 1. Specifying path for use of GDS remapping table.

Press OK to accept this modification to the GDSII output setup.

You are now ready to stream out your cell.

**Note**: When you have completed the stream out process, you will need to go back and uncheck the box "Use output layer remapping table" otherwise you are going to use this remapping table on every stream out.

**Q. How can I measure the width of a geometry placed at an angle not multiple of 45 degree, for example a line placed at 35 degree.**

A. There is a measurement option called "Point/Line Distance". If you set the gravity to snap to the edge of geometry and use the Point/Line Distance option, it will measure from edge to edge or line to line at a 90-degree angle of the line. This gives you the exact width of the geometry regardless of its angle of positioning.

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