Gate Charging Simulation Using *ATLAS/MixedMode*

Introduction

In modern power devices, the total power loss comprises both a conductive power loss component and a capacitive loss component. As the cell pitch decreases, the conductive loss will decrease while the capacitive loss will increase. Therefore, for small cell pitch the capacitive power loss may be the dominant component of the total power loss in the device.

There is clearly a need for a method that will allow analysis of the capacitive component of the power loss. One technique to do this in a power UMOSFET device is to analyze the gate charging time using ***ATLAS/MixedMode.***

ATLAS/MixedMode is a circuit simulator that can include elements simulated using device simulation, as well as compact circuit models.

Device Structure and Circuit

As shown in Figure 1, this design has a U-Groove in the gate region, and has a higher channel density which reduces the on-resistance as compared to VMOSFETs or DMOSFETs.

Effects of device size and transconductance makes power loss component analysis more difficult. A more useful parameter from the circuit design point of view is the gate charge rather than capacitance. Figure 2 shows the gate charge simulation test circuit.

Simulation Results and Discussion

The advantage of using gate charge is that the designer can easily calculate the amount of current required from the drive circuit to switch the device on in a desired length of time because Q=CV and I=C dv/dt, the gate charge is the product of time and current.

For example, a device with a gate charge of 20nC can be turned on in 20μs if 1mA is supplied to the gate or it can turn on in 20ns if the gate current is increased to 1A. These simple calculations would not have been possible with input capacitance values.

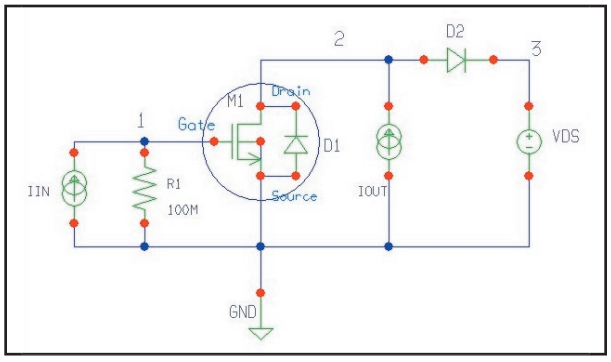

Figure 2. Test Circuit for Gate Charging

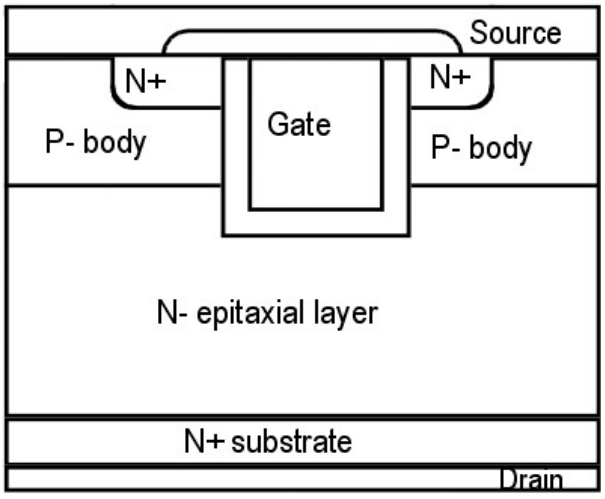

Figure 1. Typical UMOSFET Structure

Figure 3 shows gate voltage versus drain bias. From 4μs, drain voltage becomes Vds(on)=Ion*Rds(on), and the transient is completed. The MOSFET is biased to the edge of the ohmic region from the active region. From this waveform, the total gate charge, gate-source charge and gate-drain(Miller) charge can be obtained from the product of time and gate current.

Conclusion

This article presented a review of the capacitive loss of a power MOSFET using the ***ATLAS/MixedMode*** simulator. This gate charging analysis makes it easy to calculate the amount of current to switch the device in a desired length of time.

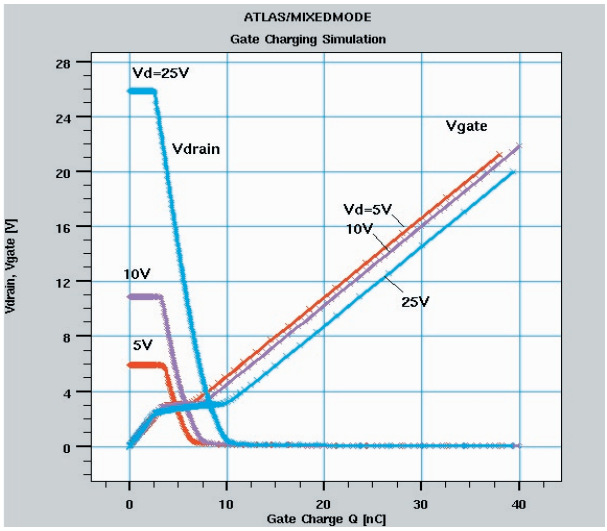

Figure 3. The waveform of the gate charging at gate current is 2mA