Simulation Standard

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Transient Simulations of Edge Emitting Fabry-Perot InP/InGaAsP Laser Diode Using Silvaco TCAD Tools

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In this communication we present a brief description of our initial results of transient simulation of InP/InGaAsP Fabry-Perot edge emitting laser diode structure Using Silvaco *ATLAS/Blaze* and *Laser* modules. The data presented here have not been optimized and it represents work in progress. This initial simulation presented here represents a heterostructure of bulk materials without any quantum confinement calculations or strain effects. This naturally will impact on the calculated lasing frequency.

The simulated device is an n-i-p InP diode with InP active region containing a 200nm thick InGaAsP layer. Semi-insulating current blocking regions were also used in the simulated structure. Due to the presence of Fe in these regions, traps were introduced

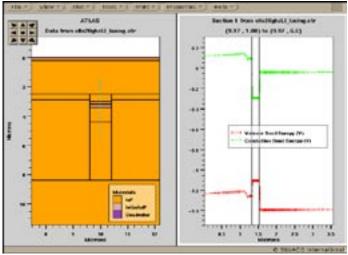


Figure 1. InP/InGaAsP edge emitting laser diode structure. A cut line is used to illustrate the band gap diagram across the active region.

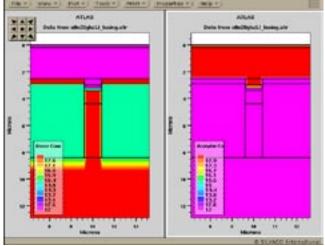


Figure 2. The doping profiles are shown here. Generic donors and acceptors were used alongwith deep level traps to simulate the effect of Fe in the current blocking regions.

at 0.62eV in the band gap for these layers. Figure 1 shows the general structure of the diode together with the band gap diagram at a bias point of 1.2 volt at the anode.

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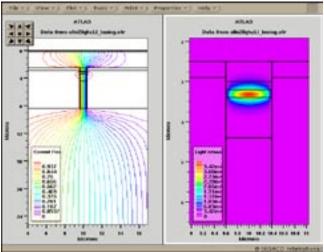


Figure 3. The current flow contours through the device are shown at a bias of 1.2V on the anode. The transverse optical mode is also shown

Simple doping profiles were used as shown in Figure 2 to achieve the current blocking effect. This can be seen clearly in Figure 3 where the total current contours can be seen. Each of the colored contours represents an equal portion of the total current running through the device at the chosen bias of 1.2 volts. Also shown at this bias is the light intensity from the active region of the laser diode. Figure 5 shows the energy spectrum of the emitted photons at the same bias of 1.2V.

The transient simulation experiment was done by first biasing the diode in dc mode up to 1.9V and then, introducing a voltage pulse of 0.0225V over a ramp time of 1E-10 seconds then simulating the transient over a time period of 1E-8 seconds. The photon density ringing effect can be seen with an oscillation frequency (fc) of

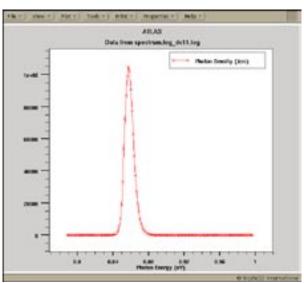


Figure 5. The transient solution was obtained by using a small voltage pulse over a 1E-10 seconds.

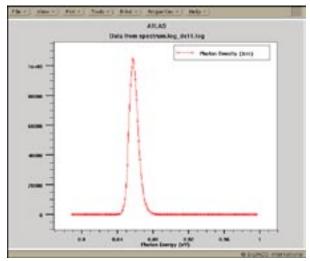


Figure 4. The photon energy spectrum at a bias of 1.2V on the anode.

5.9GHz. This frequency is dependent on the time dependent interaction between the carrier density within the laser cavity and the optical field therein.

Conclusion

In conclusion we demonstrate the scope of laser simulation within the Silvaco TCAD tools using the *ATLAS/Laser* modules and in particular the coupling of photonic and electrical equations for time domain simulations of experimentally observed dynamic damped ringing effects of the photon density after application of a short rise time input voltage pulse to the laser.

Reference

 NUSOD-2002, Held at The Swiss Federal Institute of Technology (ETH), Zurich, Switzerland. Sep 25-27 2002.

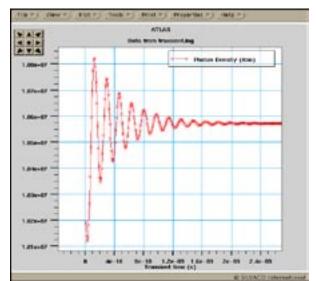


Figure 6. The damped oscillations of the photon density with time following a voltage step with a risetime of 1E-10 seconds.

Practice of LPE Rule File Generation by EXACT

EXACT automatically generates technology file for parasitic R and C extraction with *HIPEX-RC* or other rule-base LPE tools. Here I describe how to write a *LISA* script to generate those LPE rule files.

The Structure of *LISA* Script to Generate LPE Rule Files

EXACT generates an LPE rule file for parasitic C extraction which contains a couple of parts: one is for overlapping capacitances between a couple of layers, and another one is for lateral capacitances for a single layer. You can write LISA script for each of those parts separately for easier maintenance.

EXACT allows you to use LOAD command to execute multiple *LISA* script to generate LPE rule files separately. You can merge those generated rule files using some shell commands such as "cat". You can use those shell commands with a function 'sh("<filename>");' in *LISA* script.

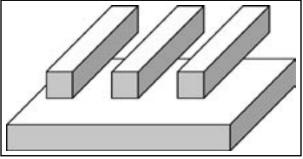


Figure 1.

And also, you can write some description independent from *EXACT's* simulation, such as comments or layer derivation commands, using WRITE command in *LISA* directly. You can merge those description prepared as another separated text file.

You can calculate lateral capacitances using a built-in test pattern "OneArray" (Figure 1).

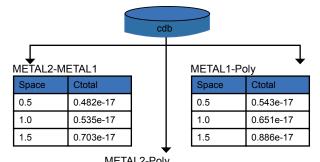
```
`sh("rm tut4 total*.txt");'
fp1=open("tut4_total1.txt", "write");
write(fp1, "!=========\n");
write(fp1, "! HIPEX-C command file created by EXACT2\n'');
write(fp1, "!----\n");
write(fp1, "! Generated by " & get time());
write(fp1, "!======\n\n");
close(fp1);
fp1=open("tut4_total2.txt", "write");
write(fp1, "!===========n");
write(fp1, "! End of Script\n");
write(fp1, "!========\n\n");
close(fp1);
load ("tut4_OV_1.lisa");
load ("tut4 OV 2.lisa");
load ("tut4 LL.lisa");
'sh("cat tut4 total1.txt tut4 OV 1.txt tut4 OV 2.txt tut4 LL.txt tut4 total2.txt >> tut4 total.txt");'
load ("tut4 OV 1.lisa");
load ("tut4_OV_2.lisa");
load ("tut4_LL.lisa");
'sh("cat tut4 total1.txt tut4 OV 1.txt tut4 OV 2.txt tut4 LL.txt tut4 total2.txt >> tut4 total.txt");'
```

Example of LISA script for LPE rule generation (1): Lateral capacitance.

First you specify the C database created by EXACT using a *LISA* function DATABASELOAD(). Next, you use EXTRACT_NAME() to add a name to a specified part of extracted capacitance. You can specify the part by a couple of node names that becomes the terminals of extracted capacitances.

And then, you use SELECT() command to generate a table that contains extracted capacitance and other related parameters, such as width or separation of wires.

```
db = DatabaseLoad('.");
extract_name("total","B_gnd", "Llp');
tableOA = select(db, "OneArray", {1...3},
{Width", "Space"}, {"Ctotal"});
```



IVIE TALZ-POLY		
Space	Ctotal	
0.5	0.185e-17	
1.0	0.22e-17	
1.5	0.253e-17	

You use COLUMN_VECTOR_OP() and COLUMN_SCALAR_OP() to calculate extracted capacitance values in the generated table. These commands calculate all elements in specified columns. For example, the following description calculates a mean value of capacitances between the center wire and right or left one.

Column_scaler_op(table_OA, "Ctotal", table_OA, CtotalB, "*", 10e15);

Space	Ctotal	_	Space	Ctotal	CtotalB
0.5	0.482e-17		0.5	0.482e-17	0.0482
1.0	0.535e-17		1.0	0.535e-17	0.0535
1.5	0.703e-17		1.5	0.703e-17	0.0703

And finally, you can use WRITE_PARAMETERS(_)_to output those coefficients to a text file in a rule format. If you specify "OneArrayLayer1Space" or "OA_LL", it generates multiple lines for each row in the table.

- per area (area_coef)
- per perimeter length (coind_coef)
- for between side edge and surface (side_up_coef, side_down_coef)

Described here is how to calculate area_coef and side_up_coef / side_down_coef.

You can use a built-in test pattern "ParallelPlate" to calculate capacitance per area.

You can get a value for side_down_coeff by deducting this capacitance value per are from a total value in OneArray.

```
'sh("rm tut4_LL.txt");'
   db = DatabaseLoad("./tutorial_db");
   extract_name("OA_LL1", "L1p", "L1l");
   extract_name("OA_LL2", "L1p", "L1r");
   i=0:
   loop begin
     if (i GTR 3) then (leave loop);
     OA combinations = {i};
     1-----
        Create table for Lateral Capacitance
     table_LL1 = select(db, "OneArray", OA_combinations,
          "OneArrayLayer1Space", "OneArrayLayer1Width"},
         {"OA_LL1", "OA_LL2"});
     save_table(table_LL1, CSV, "table_LL1.csv");
     ! Calculate Fringe Capacitance
     column_vector_op(table_LL1, "OA_LL1", table_LL1, "OA_LL2", table_LL1,
            "OA LL sum", "+");
     column_scalar_op(table_LL1, "OA_LL_sum", table_LL1, "OA_LL_tmp", "/", 2);
     column_vector_op(table_LL1, "OA_LL_tmp", table_LL1, "OneArrayLayer1Space",
             table_LL1, "OA_LL_tmp2", "*");
     column_scalar_op(table_LL1, "OA_LL_tmp2", table_LL1, "OA_LL", "*", 1e15);
Example 2.
```

```
layername1 = get element(table LL1, "LAYER0", 1);
layername2 = get_element(table_LL1, "LAYER1", 1);
!-----
! Write script for Overlap Capacitance
write_parameters("tut4_LL.txt", table_LL1,
     {" !----\n"});
write parameters ("tut4 LL.txt", table LL1,
    {" ! Lateral capacitance of " & layername2 & "\n"});
write_parameters("tut4_LL.txt", table_LL1,
    {" !----\n\n"});
write_parameters("tut4_LL.txt", table_LL1, {"
                                      /layer1=" & layername2 & "\n"});
write_parameters("tut4_LL.txt", table_LL1, {"
                                      /vicinity=2.0\n"});
write_parameters("tut4_LL.txt", table_LL1, {"
                                      /k1\_coef=(\{\n''\});
write_parameters("tut4_LL.txt", table_LL1,
         {", "OneArrayLayer1Space", ", ", "OA LL", "}\n"});
write_parameters("tut4_LL.txt", table_LL1, {" })\n"});
write_parameters("tut4_LL.txt", table_LL1, {"
write_parameters("tut4_LL.txt", table_LL1, {"
                                      /k2 coeff=0\n''});
                                      /k3 coeff=1;\n\n''});
```

Example 3.

In the actual *LISA* script, it uses SELECT(_) function to create tables for OA_CTotal extracted between interconnect and substrate in OneArray, and also for PP_Ctotal, extracted in ParallelPlate.

Cside down

Cside_down

CArea

And then, it uses COLUMN_VECTOR_OP() to deduct the above two capacitance, and uses the result as OA_CFringe, corresponding to Cside_down.

Column_scaler_op(table_OA, "Ctotal", table_OA, CtotalB, "*", 10e15);

Space	Ctotal	+	Space	Ctotal	CtotalB
0.5	0.482e-17		0.5	0.482e-17	0.0482
1.0	0.535e-17		1.0	0.535e-17	0.0535
1.5	0.703e-17		1.5	0.703e-17	0.0703

If you want to replace result extracted by *EXACT* to rule script for LPE tools such as *HIPEX*, you need to combine more than one test pattern, and then deduct between them. Especially, if you want to higher the extraction accuracy of LPE_tool, this combination can affect the result.

Others

You can use LISA basic functions freely in the *LISA* script for LPE rule generation. In the above examples, *LISA's* OPEN() and WRITE() functions are used to create arbitrary text files. And also, you can use LOOP BEGIN - END construction, so that you can access each element in a created sequence freely. With those functions, you can write *LISA* script for LPE rule generation without restriction. It is important to use those functions freely for writing *LISA* script for various LPE tools.

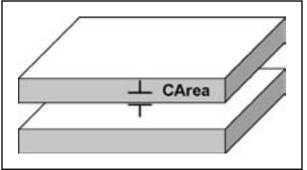


Figure 2a.

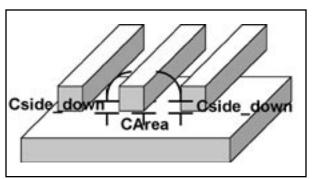


Figure 2b.

```
1-----
   Create table for Fringe Capacitance
 1-----
 table_OA = select(db, "OneArray", OA_combinations,
    { "OneArrayLayer1Space", "OneArrayLayer1Width" },
    { "OA Ctotal" });
 1-----
 ! Create table for Overlap Capacitance
 1-----
 table PP = select(db, "ParallelPlate", OA combinations,
    {"ParallelPlatePlateWidth"},
   {"PP Ctotal"});
 1-----
 ! Calculate Fringe Capacitance
 !-----
 merge(table PP, "PP Ctotal", table OA);
 column vector op(table OA, "PP Ctotal", table OA, "OneArrayLayer1Width",
      table OA, "OA CAreaB", "*");
 column vector op(table OA, "OA Ctotal", table OA, "OA CAreaB",
      table_OA, "OA_CtotalB", "-");
 column scalar op(table OA, "OA CtotalB", table OA, "OA CFringe", "*", 1e15);
 column_scalar_op(table_OA, "OA_CAreaB", table_OA, "OA_CArea", "*", 1e15);
 !-----
 layername1 = get_element(table_OA, "LAYERO", 1);
 layername2 = get element(table OA, "LAYER1", 1);
 Carea_coef = get_element(table_OA, "OA_CArea", 1);
 1-----
 ! Write script for Overlap Capacitance
 1-----
 write parameters("tut4 OV 2.txt", table OA,
     {"!----\n"});
 write parameters("tut4 OV 2.txt", table OA,
     {" ! Overlap capacitance between " & layername1 & " and " & layername2 & "\n"});
 write_parameters("tut4_OV_2.txt", table_OA,
      {"!----\n\n"});
 write parameters("tut4 OV 2.txt", table OA, {" CUP OVERLAP\n"});
 write parameters("tut4 OV 2.txt", table OA, {"     /lpe mode=(medium)\n"});
 write_parameters("tut4_OV_2.txt", table_OA, {" /layer2=" & layername2 & "\n"});
 write parameters("tut4 OV 2.txt", table OA, {"
                                 /vicinity=2.0n''});
 write_parameters("tut4_OV_2.txt", table_OA, {"
                                  /area coef=" & Carea coef & "\n"});
  write\_parameters("tut4\_0V\_2.txt", table\_OA, \{ " \ /c\_side\_down\_coef=(\{ \n'' \} ); \} 
 write parameters ("tut4 OV 2.txt", table OA,
        {", "OneArrayLayer1Space", ", ", "OA CFringe", "}\n"});
 write parameters("tut4 OV 2.txt", table OA, {"
                                 });\n\n"});
end;
```

Example 3.

Two-Dimensional Device Simulation of the InGaAs/InP Avalanche Photodiodes

1. Introduction

The high gain, and high gain-bandwidth product of the avalanche photodiodes is one of the key device for the long distance optical communication systems. For the 0.92-1.65um wavelength range, the narrow bandgap materials, like InGaAs(0.77eV), are used as the absorption medium. And the breakdown location is a major issue to design of the APD's. In order for the device to operate with high gain and low noise[1], the design of the guard ring to suppress edge breakdown is important.

The object of this article is to get the multiplication[2], the leakage current under the dark and the illuminated current[3] was simulated. And the other important factor of the cut-off frequency calculated by the numerical device simulator *ATLAS*.

2. Device Structure and Models

In order to simulate of the APD's, the thickness and doping level used conventional APD device. The dark current and illuminated current is very depend on the absorbed layer and the doping profile. And the multiplication layer thickness is the very key parameter of the breakdown voltage and position of the avalanche. Here the simple APD's structure showed with guard ring as Figure 1.

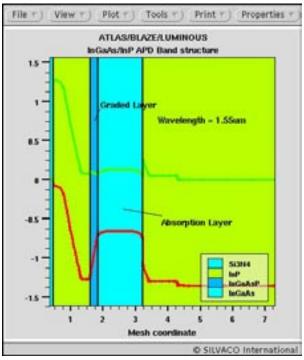


Figure 2. The Band structure of the APD.

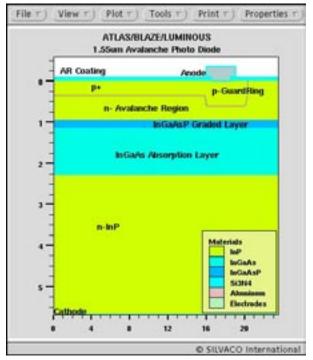


Figure 1. Cross-sectional view of the simulated APD.

A thick InGaAs absorption layer with very low donor type is on the InP substrate with the InP buffered layer. The speed of the APD is very depend on the thickness of the absorption layer. This is due to the reduction in transit time when this absorption layer is reduced. And in order to reduce the charge build-up at the heterojunction interface a graded layer is introduced between the InP and InGaAs absorption layer.

To simulate the avalanche photodiodes, the generation rate due to impact ionization must be calculated.

The general impact ionization process is described by

$$G = \alpha_n |\overrightarrow{J}|_n + \alpha_p |\overrightarrow{J}|_p$$

here, G is the local generation rate of electron-hole pairs, $\alpha_n \alpha_p$ are the ionization coefficient for the electron and hole, $J_n J_n$ are their current density.

In *Blaze/ATLAS*, the impact ionization rate included with the self-consistantly in basic equation and material parameters[4]. For the purpose of numerical simulation, the parameters for the InP and InGaAs was given in Table I. And the other basical material parameters are integrated in *Blaze/ATLAS* depend on the mole fraction. Figure 2 shows the Band structure of this APD.

Parameter	Units	InGaAs	InP
Electron Auger Coeff	cm6/s	7.0e-29	9.0e-31
Hole Auger Coeff	cm6/s	7.0e-29	9.0e-31
Electron SRH lifetime	sec	8.0e-8	6.0e-12
Hole SRH lifetime	sec	8.0e-8	6.0e-12
Radiative Recombination Rate Coeff	cm3/s	9.6e-11	1.2e-10
Electron Impact Ionization	1/cm	5.15e7	1.0e7
Electron Critical Field V/cm		1.95e6	3.45e6
Hole Impact Ionization	1/cm	9.69e7	9.36e6
Hole Critical Field	V/cm	2.27e6	2.78e6
Light absorption Coeff	1/cm	8000	0

Table I. List of the Material Parameters used for the simulation

And the influence of the applied bias with illuminated condition, the opto-generation rate must be calculated. The *Luminous* is a general purpose of ray tracing and light absorption program integrated into the *ATLAS*.

$$G = \alpha_n |\overrightarrow{J}|_n + \alpha_p |\overrightarrow{J}|_p$$

here, the η_0 is the internal quantum efficiency, P^* contains the cumulative effects of reflection, transmission, and loss due to absorption, λ is the wavelength of the illuminated light, h is Planck's constant, c is the speed of light, α is the absorption coefficient.

The light into the APD can set the gaussian form as like the beam from the optical fiber. And the C-Interpreter could make sure the user's unique absorption model depend on the illuminated wavelength. In Figure 3 under the metal has high absorption coeff, so the photogeneration rate close to be zero.

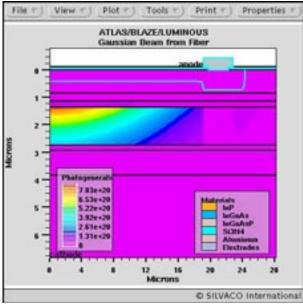


Figure 3. The gaussian beam form like outcoupling from optical fiber.

3. Simulation Results and Discussion

The dark current and illuminated current versus bias voltage is shown in Figure 4. As the Figure 4, there are 3 phase of operation.

In phase I, the current is due to thermally excited carriers in the InP, and for the illuminated case, the collection of generated is zero.

In Phase II, the charge sheet has been fully depleted and the device operates like to p-i-n photodetector. Under this condition, the carriers are not transported to multiplication layers in the high field. And for the illuminated case, the depletion layer still under the Graded layers, so the absorption effect is very low.

In phase III, the device operates as an APD. The carriers generated within the InGaAs absorption layer with photogeneration can drift into the high field multiplication region, so an internal gain mechanism was provided

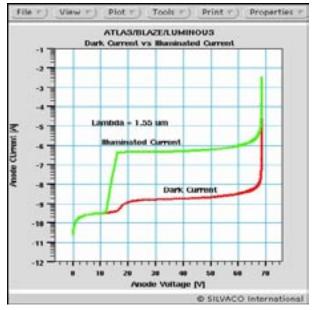


Figure 4. Typical I-V plot of the dark and illuminated current.

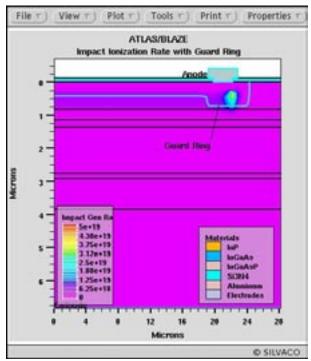


Figure 5. Impact Ionization rate distribution due to the Electric field.

with the impact ionization. In Figure 5, the distribution of the impact ionization rate shows where the maximum electric field is high on the multiplication layer.

Finally, the AC response of the APD was calculated with small signal analysis of the illuminated light. The Figure 6 shows the 3 GHz cut-off frequency by the *Luminous/ATLAS*. The plot of the 3dB bandwidth could make the collect the cut-off frequency each Anode bias point.

4. Conclusion

The InGaAs Avalanche Photodiodes has been successfully simulated within the *Luminous/ATLAS* for the DC analysis and AC analysis in this article. And the dark current and illuminated current was shown under the reverse voltage. The ATLAS is linked seamless the drift diffusion to impact ionization and photogeneration.

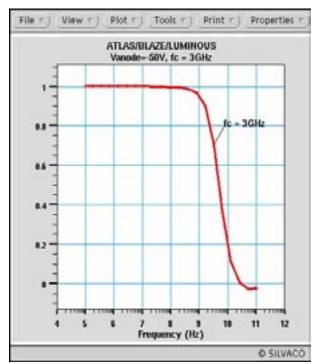


Figure 6. Frequency vs Normalized modulated output.

Reference

- [1] Mohammad A. Saleh et al, "Impact-Ionization and Noise Characteristics of Thin III-V Avalanche Photodiodes", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 48, NO. 12, DECEMBER 2001, pp.2722-2731
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- [3] C.L.F.Ma, M.J.Deen , L.E.Tarof, "Multiplication in Separate Absorption, Grading, Charge, and Multiplication InP-InGaAs Avalanche Photodiodes", IEEE Journal of Quantum Electronics, Vol.31, No.11 November 1995, pp.2078-2088
- [4] Joseph W. Parks, et al, "Theoritical Study of Device Sensitivity and Gain Saturation of Separate Absorption, Grading Charge, and Multiplication InP/InGaAs Avalanche Photodiodes", IEEE Transactions on Electron Devices, Vol.43, No.12, December 1996, pp.2113-2121

Calendar of Events

November December 3 4 5 6 ICCAD - San Jose, CA ICCAD - San Jose, CA ICCAD - San Jose, CA 10 ICCAD - San Jose, CA 10 11 ICCAD - San Jose, CA 11 13 IEDM - San Francisco, CA 13 14 14 IEDM - San Francisco, CA 15 IEDM - San Francisco, CA 16 16 17 17 18 18 19 19 20 21 21 22 22 23 24 25 25 26 27 28 29 29 30

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Bulletin Board



Silvaco at IEDM

See Silvaco TCAD and modeling tools at IEDM simulate CMOS, bipolar, SOI, strained silicon and SiGe devices, noise behavior of MOS structures and device measurement and characterization. Silvaco leadership in CMOS imagers, CCD's, TFT's, MEMS, organic, amorphous, and polycrystalline devices, vacuum microelectronics, emissive displays and sensors for chemical, molecular and biological applications. Silvaco tools solve these problems using analytical, numerical, and statistical approaches to modeling electronic and optical devices. their isolation and interconnection. Process and device engineers simulate front-end and back-end process modules for fabrication of CMOS, memory, BIC-MOS, and compound semiconductors (GaAs, InP, GaN, SiC, and their related alloys) devices. Front-end processing includes substrate technologies, lithography, etching, isolation technologies, thin dielectrics, high dielectric constant materials and metal electrodes for transistors and MIM capacitors, shallow junctions, RTP, silicides, and new materials. Back-end processing include conductor systems, low dielectric constant materials, contact and via processes, planarization, and design considerations for multilevel interconnects.

 $If you would \ like \ more \ information \ or \ to \ register \ for \ one \ of \ our \ workshops, \ please \ check \ our \ web \ site \ at \ \ http://www.silvaco.com$

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Hints, Tips and Solutions

Robin Jones Ph.D., Senior Applications and Support Engineer

Q. How do you perform a lift off procedure in ATHENA?

A. A common technique for creating metal contacts is one known as a lift off. When performing a lift off process step, in order to create metal contacts, for example, it is imperative that the part of the metal to be lifted off is disjoint from the deposited metal layer. A good way of performing a lift off process procedure in *ATHENA* is to make use of a deposit machine created in *ATHENA*.

The ATHENA syntax for such a procedure is as follows:

rate.depo machine=audepo material=gold a.m \
sigma.dep=0.0 unidirec dep.rate=500 \
angle1=0.00

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deposit machine=au_depo time=1.0 minutes \
divisions=6

Here we have first created a machine called au_depo, the material we are depositing is gold, a.m specifies that the rate is in Angstroms per minute, dep.rate is the deposit rate i.e. in this case it is 500 Angstroms, unidirec specifies it is unidirection, angle1 is the angle used by unidirec. Sigma.dep specifies the surface diffusion parameter used by unidirect.

After the machine has been created use is then made of the deposit command which in turn makes use of the machine just created. Figure 1(a) shows such a deposit.

Beneath the gold is the photoresist barrier. Note how the gold on top of the barrier is disjoint from the the gold surrounding the barrier. This therefore makes it possible for a strip resist command to remove the resist and thus lift off the gold, Figure 1(b).

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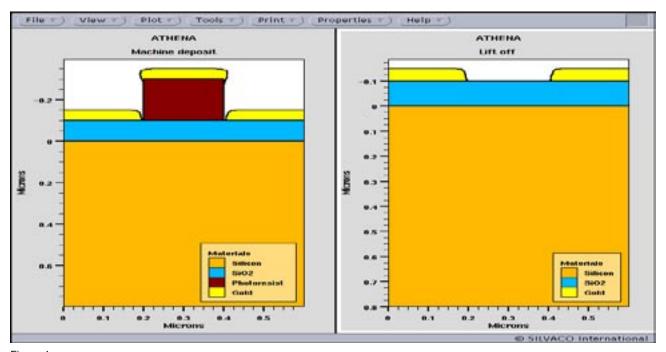


Figure 1.



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