Simulation Standard

Connecting TCAD To Tapeout

A Journal for Process and Device Engineers

STELLAR – Process Based Parasitics Capacitance Extraction on Large Custom Cells : Overview and Features

I Introduction

SILVACO has recently released a new suite of interconnect analysis tools to meet the demands of state of the art cell, circuit and chip design. Indeed based on the success of ***CLEVER*** and ***EXACT,*** SILVACO wants to provide to customers tools with the same accuracy as the previous ones but dedicated to bigger layouts. It is becoming increasingly clear that with current designs around 0.1um parasitics are more and more important to take into account. Designers have to make an important decision whether to have verification either very precise using tools like ***CLEVER*** on relatively small layouts [1] or using classical LPE tool like ***HIPEX*** [2] which are known to be sometimes not accurate enough. Between them a wide gap lies and the aim of SILVACO new products is to fill it. These new tools keep the same famous in-house trends so-called TCAD driven CAD which means that as a fundamental core a 3D process simulator and a 3D field solver are the basis for an accurate parasitics extraction today.

This article will illustrate the architecture and the applications of ***STELLAR*** our new Fast Capacitance Parasitics Extractor Software and we will compare results to the field solver reference on the market ***CLEVER***.

II STELLAR Architecture

Parasitic extraction accuracy is crucial for deep submicron designs. The targeted accuracy has been considered to be 3D Field Solver based. ***STELLAR*** reaches this goal by using a combination of 3D process and 3D field solver capabilities. The 3D process simulation allows the geometry of the final structure to be very accurately generated. Once the geometry is generated, a 3D topology of the layout is obtained. This is essential for accurate parasitic extraction for deep and ultra deep submicron technology.

This combination also allows ***STELLAR*** to be a powerful and flexible solution for extracting highly accurate parasitic capacitances in deep submicron designs summarized in the following chart. Note the architecture of ***STELLAR*** (Figure 1) is identical to that of ***CLEVER*** and ***QUEST***. However the process simulator and the field solver are different.

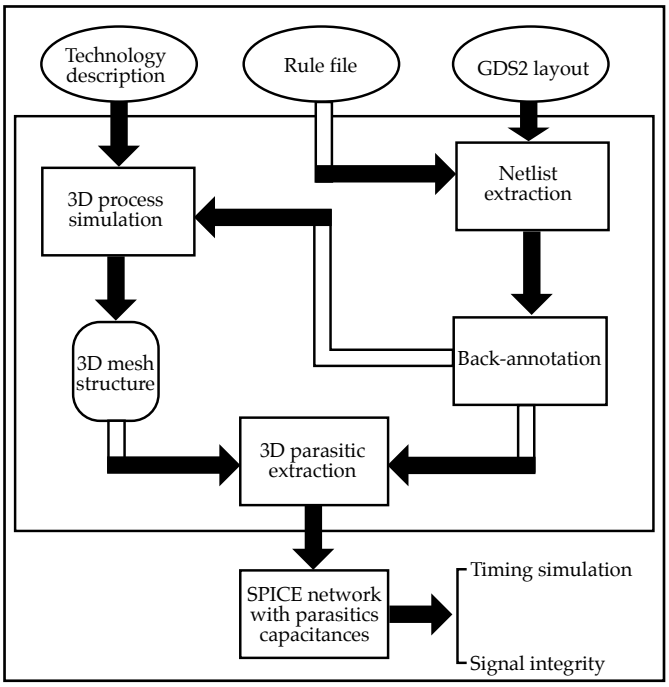

Figure 1. The Parasitic Extraction Overview in CLEVER.

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INSIDE

Figure 2. Main STELLAR window.

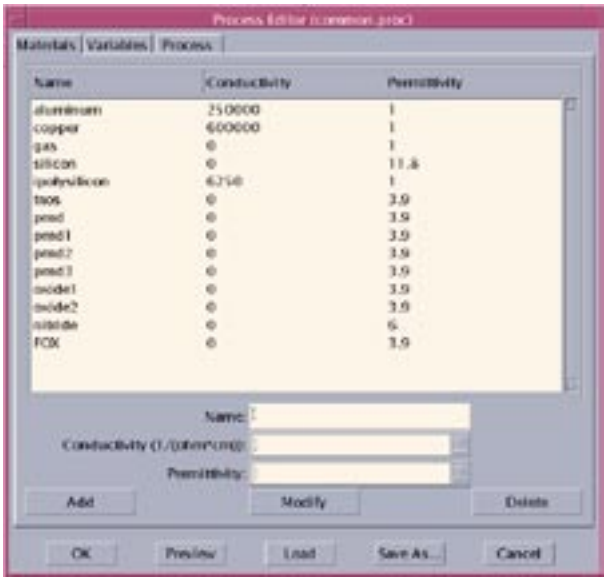

Figure 3. STELLAR process window

Capacitances are calculated from the distribution of charge density on the surfaces of conductors. Classically one can solve partial differential equations on the potential which can be done using finite difference or finite element methods. The normal derivative of the potential on the surfaces gives the charges acquired for capacitance calculation. The resultant matrix is sparse but large because the whole dielectrics volume is discretized. A very good 3D tetrahedral mesh is thus needed to solve this problem. Arbitrary conductor shapes and non-homogeneous structures can be handled. This is typically ***CLEVER***.

A new method [3] is used in ***STELLAR***. The meshing of a complex 3D domain is avoided by the use of two different meshes: a regular 3D grid on the whole domain and a surface mesh on the conductors. Due to this specific grid algorithm (volume + surface) the resultant matrix is sparse and a fast solver can be used to solve this system at low memory cost. The typical type of structure able to be simulated is planar and Manhattan. However, dummy metal simulations are also available [4].

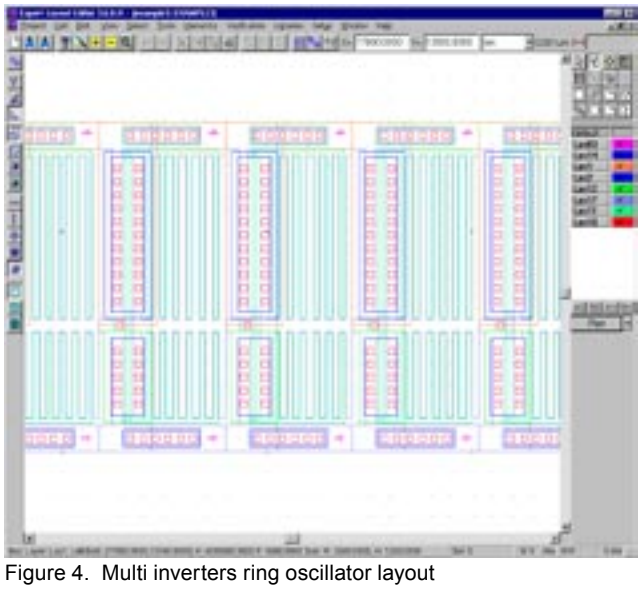

Figure 4. Multi inverters ring oscillator layout

III Product Overview

STELLAR exhibits the standard graphical user's interface used in our ***DISCOVERY*** range of products (from ***QUEST***, ***EXACT*** to ***QUEST3D***), which eases its handling like all SILVACO software, which have been known to be intuitive and very easy to start with. The main steps to follow to define a complete parasitics capacitance extraction, from layout input, to final parasitics netlist extraction (note that all the pictures are from the GUI, but one can be done by more advanced users through batch mode) are now discussed.

When invoking ***STELLAR***, the main ***STELLAR*** window shows up (Figure 2) and exhibits all the sequential steps that must be completed in order to extract the parasitic capacitances netlist.

The first step consists in describing the backend process flow, by indicating the material properties (conductivity for conductors and permittivity for insulators) and thicknesses. All of these parameters can be defined as variables allowing process variation experiments to be performed (Figure 3).

The second step is the layout input to ***STELLAR***, which can handle GDSII standard.

Eventually, the technological files required for netlist extraction need to be inputted. These may consist of derived layer generation, layer connectivity and device recognition. The actual device extraction performed on the layout is actually achieved using ***HIPEX-NET*** [2].

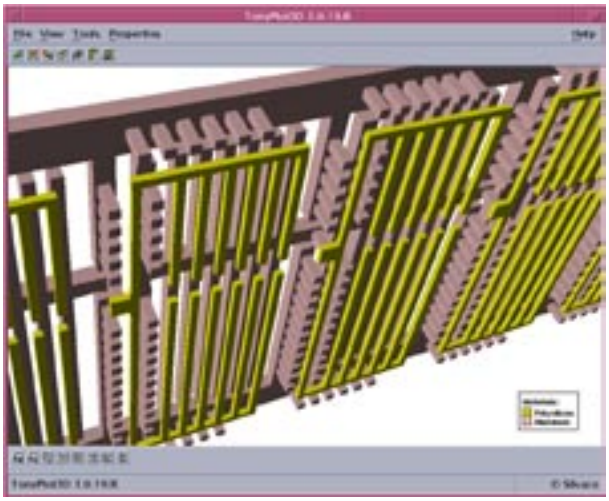

Figure 5. Backend 3D structure used by STELLAR

The next stage is the definition of the required accuracy for computation. After this has been completed ***STELLAR*** has all the relevant data to generate the 3D structure that will be meshed to extract parasitic capacitances.

Two types of data can be outputted according to the user's wish: the 3D backend structure for topology checking purpose, and/or the parasitics netlist.

STELLAR also exhibits a very powerful feature, consisting of a built-in design of experiment (DOE) library. The available ones are: stepped, full or half factorial, box Behnken, circumscribed or faced central composite, linear and Gaussian random and Latin hypercube. This allows a large choice in the variation method, accordingly to the required range.

After having selected the type of DOE variation the simulation can be carried out automatically accordingly to the selected DOE, and the results (both 3D structure and parasitics netlist) stored in separated directories for subsequent use.

IV Simulation Results and Validation

STELLAR is targeted to simulate larger structures than the ones simulated by ***CLEVER*** [4]. An example of this is a multi stage inverter ring oscillator that has been simulated with ***STELLAR*** (Figure 4).

Once the process and technological files are parsed, the 3D interconnect structure that is to be meshed is generated and then subsequently used by the solver (Figure 5).

The parasitic capacitance netlist is then computed, and merged to the netlist extracted by ***HIPEX***-NET thus having the devices extracted from the input layout. The final netlist is then ready to be used by ***SmartSpice*** or any compatible SPICE simulator, for signal integrity analysis or delay analysis, as shown in Figure 6.

In order to validate ***STELLAR***, its output and simulation time are compared to a simulation using ***CLEVER***. ***CLEVER*** is a widely well accepted tool for field solver applications and is considered to be our reference for parasitics extraction [5].

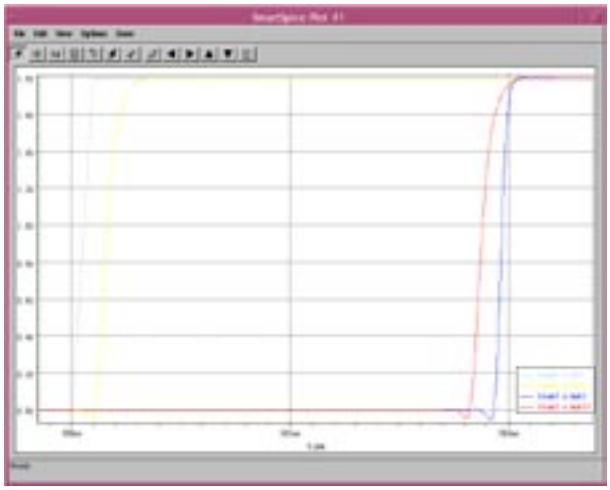

Figure 6. SmartSpice transient analysis of the 34 stages inverters ring oscillator.

Since ***CLEVER*** cannot handle the full layout, the elementary inverter used in the full ring oscillator is extracted, and simulated. The issued netlists with both active and parasitics elements are then embedded into a SPICE sub-circuit, duplicated 34 times and simulated with ***SmartSpice***. This approach is sensible, since the complete layout is highly symmetrical, and ***CLEVER*** boundary condition set to 'cyclic' to be consistent with the layout topology.

A table summarizing the simulated results from ***STELLAR*** and ***CLEVER*** is shown below.

	STELLAR	CLEVER
Delay (ps)	56.6	56.6
Simulation time (min)	52	47
Memory requirements (Mb)	245	425

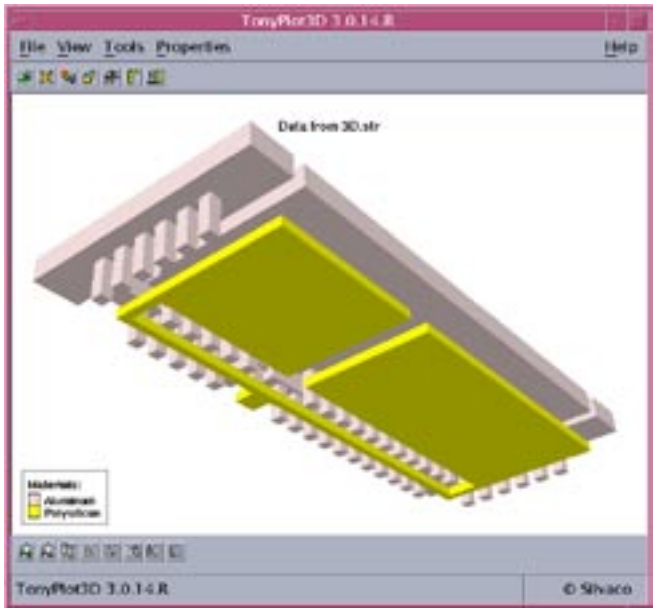

Figure 7a. Basic stage inverter (plate coupling)

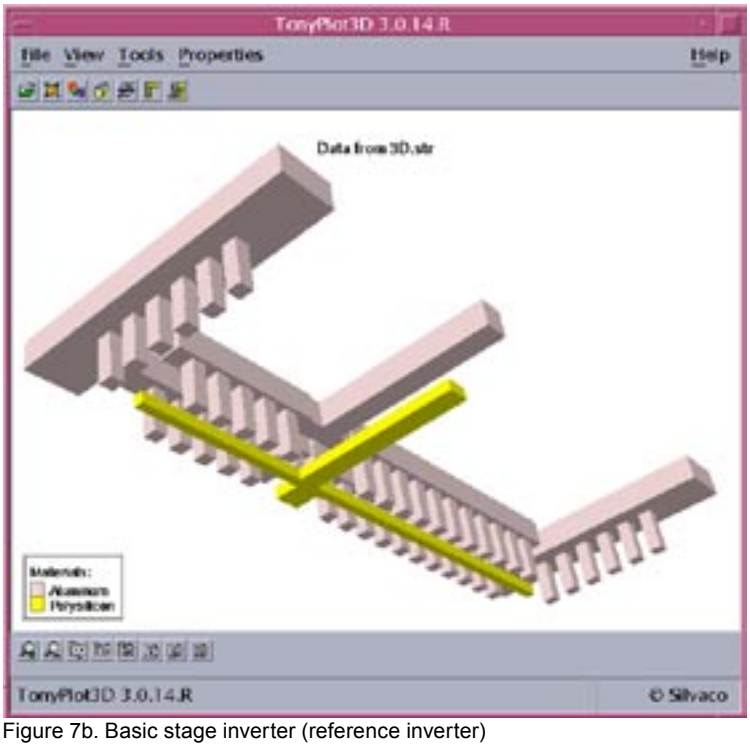

Figure 7b. Basic stage inverter (reference inverter)

Both ***STELLAR*** and ***CLEVER*** simulations were run on an Ultra 10 SPARC machine, with 1 Gb of RAM. One can see that the ***STELLAR*** simulated values are in very good agreement with thus obtained using ***CLEVER***. One can also notice the ***STELLAR*** simulation time is similar for simulating the full layout composed of 34 inverters than the ***CLEVER*** simulation time for simulating only one inverter. This exhibits the very efficient algorithm implementation and robustness. One can also see the memory requirements are 40% less compared to ***CLEVER*** for simulating a structure 34 times wider!

The second stage of ***STELLAR's*** validation used two other layout simulations.

These layouts were also ring oscillators made of chained inverters, but with different layout configurations. The 3D backend structure for each basic inverter is given in Figures 7.a and 7.b. The first structure, (Figure 7.a), layout 1 was designed in the same way as the previous one, with the idea of maximizing parasitic capacitances between the input and the output of the inverter stage (which is obviously the worst case for transit delay time).

The second layout, Figure 7.b, layout 2 was used as the reference for transit time (i.e. not increasing capacitive coupling in the layout).

The following table sums up the mean time delay per inverter.

	STELLAR	CLEVER
Layout 1	59.2 ps	58.1 ps
Layout 2	45.9 ps	43.4 ps

One can observe that again, ***STELLAR*** is able to handle such layouts associated to complex back end processes. Simulation results from the two solvers are in good agreement.

V Comparison with the Other DISCOVERY Framework Tools

The ***DISCOVERY*** framework provides various tools in order to fulfill user needs. This range is composed of the following:

- ***CLEVER*** is an accurate process based parasitics solver, which allows the extracting of parasitic netlist (both resistors and capacitors) over custom library cells.
- ***EXACT*** is used to provide capacitor models for Layout Parasitic Extractor (LPE) tools. It is based on the ***CLEVER*** simulation tool and is therefore process based and field solver based [6].
- ***QUEST*** is designed to extract frequency dependent transmission-line SPICE models [7] [8].

In order to validate the ***STELLAR*** results with the remaining tools in the ***DISCOVERY*** suite, a common structure has been designed for these three parasitics extraction tools, and the simulated results compared.

Figure 8 gives the structure cross section that has been used. This is a typical interconnect pattern, with three parallel lines over silicon wafer. Spacing 'S' between the three lines is defined as a parameter and ranges between 0.25 um and 3um. Three capacitances are plotted (Figure 9), these are described as:

- Css is the capacitance between the middle line and the substrate
- Csa and Csb are the coupling capacitances between the respective outer line and the middle conductor

One can see that despite the fact that these three tools use three different numerical methods and meshing strategies, the computed values are very close to each other.

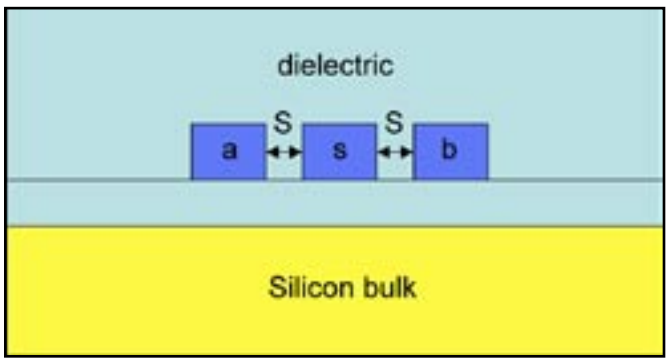

Figure 8. Three lines structure cross section.

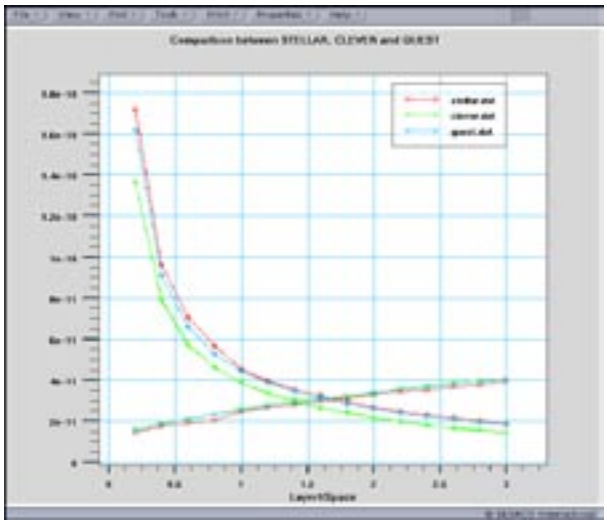

Figure 9. Comparison between ***STELLAR***, ***CLEVER*** and ***QUEST***

In Figure 9 the three capacitances between the lines and the substrate as described previously are plotted. As expected, since the structure is symmetric, both external lines exhibit the same capacitance value whatever the distance between 2 lines is (only one capacitance variation is plotted for clearity). The shape of these curves are as expected, the inverse ratio of the distance between the conductors facing each other. On the other hand, the middle line capacitance with the substrate varies less than the coupling capacitances, since distance to the substrate is kept constant. Its variation is due to the outer lines, channeling more or less electric field lines according to the distance to the middle line.

This comparison of the three tools gives an insight to the accuracy of the TCAD-based approach followed by SILVACO.

VI Targeted Structures for STELLAR

As demonstrated in the previous case study, ***STELLAR*** is targeted to handle much larger circuits than ***CLEVER***. Thanks to its new meshing and numerical schemes, accuracy is not given up to computation speed, and simulation results are in very good agreement with electrical measurements as demonstrated previously.

1) *STELLAR* New Features

STELLAR exhibits some new interesting features, which allow larger layout to be simulated. Here is a quick overview of these new functions.

The main issue with simulating large structures is obviously memory requirements. Two different techniques have been used to optimize this aspect of the simulation.

Keeping in mind that the final goal is to extract a capacitance between two conductors, a new parameter called 'effect length' has been set, which sets the distance above which the possible couplings will be considered to be insignificant. Let's call this variable 'D'. The solver will define iteratively a halo all along each conductor with the distance 'D' wrapping the considered conductor, which will determine which other conductors to take into account for capacitance calculation (all other ones will be considered being too small). This will strongly reduce domain calculation size for each conductor.

This methodology is illustrated on Figure 10, where the distance effectiveness is drawn on conductor (1). One can see that only part of conductor (2) lies within the halo, and thus only the capacitance between conductors (1) and (2) will be calculated, capacitance between (1) and (3) being considered negligible and eventually not included in the netlist.

The other technique consists in cutting the full layout into smaller parts, computing the capacitances into each domain, as well as domain boundary conditions to use for the adjacent parts (Figure 11). This technique is called domain decomposition. Its main advantage, used in conjunction with the 'halo' calculation, is to reduce the mesh to input to the solver, and then allow using very large layouts.

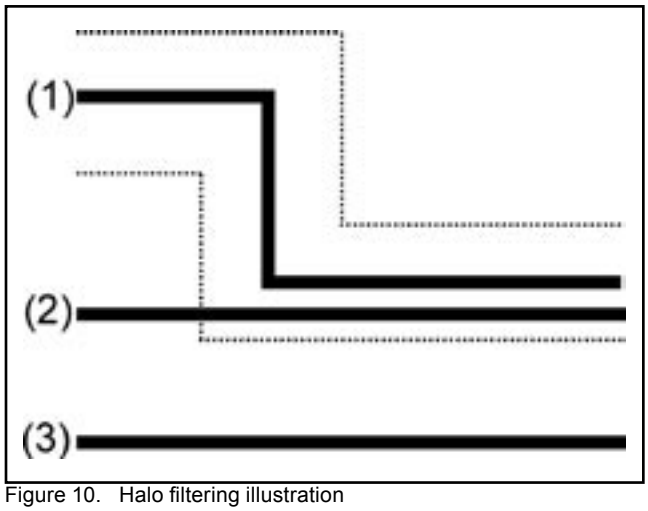

Figure 10. Halo filtering illustration

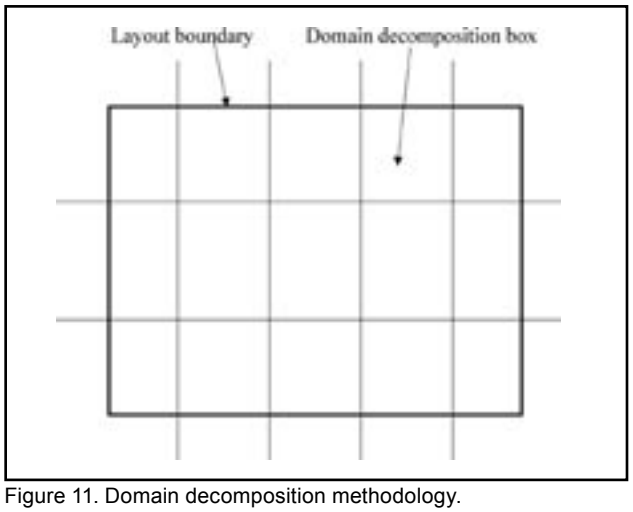

Figure 11. Domain decomposition methodology.

The other main advantage, thanks to 'halo' calculation, lies upon the fact that on certain domains, no capacitance calculation will occur, since no conductor will lie within the halo.

2) *STELLAR* New Features Validation

In order to validate the concepts used in ***STELLAR***, some simulations have been carried out using or not domain decomposition and/or using or not the 'halo filtering' method. This has been applied to the ring oscillator presented previously.

The first simulation consisted in inputting the entire layout at once. Both domain decomposition (DD) and halo methodology unset. The next simulation has been done with the ***STELLAR*** default parameters, i.e. automatic selection of DD, halo methodology set.

All the extracted netlists have been inputted to SmartSpice. The following table sums up the simulation results obtained.

	Maximum memory used (Mb)	Simulation time (min)	Delay (ps)
No DD, no halo	154	120	57.3
DD+halo	245	52	56.6

One can observe from this table that both methods give the same delay per inverter. Thanks to domain decomposition method, used in conjunction with the halo filtering, one can observe that the simulation time is decreased by almost 5 times, the maximum memory size being constant (boundary conditioning management).

The other interesting feature is that thanks to halo filtering, the computed parasitic capacitance netlist is much smaller than computing the full structure at the same time. To give an idea on the SPICE netlist reduction, with DD and halo filtering, there are 172 computed capacitances, whereas there are 634 with the classical methodology (no DD, no halo filtering). One can immediately see the advantage of the filtering, not only considering the netlist reduction, which can be achieved by other external tool like netlists reductors, but the RELEVANT netlist calculation at the solver level, which ONLY computes capacitances being influent for the SPICE simulation.

Setting these options gives the users the insurance of having the most optimized parasitics capacitance netlist (on the part number level), allowing thus fast SPICE computations not giving up accuracy to computation speed.

Figure 12. STELLAR generated 3D backend structure.

3) *STELLAR* New Features

In order to give an idea of ***STELLAR's*** potential and efficiency, a large layout has been inputted to ***STELLAR*** (50*40 um2). Interconnect density is very high (Figure 12), and this technology features four interconnection layers.

This layout has been used with its technology file as input to ***STELLAR***, and the cell's backend topology simulated. This structure exhibits state of the art technology, since in this example case, one can see that several conducting materials can be used (polysilicon, aluminum, copper…), as well as any intermetallic dielectric material (not

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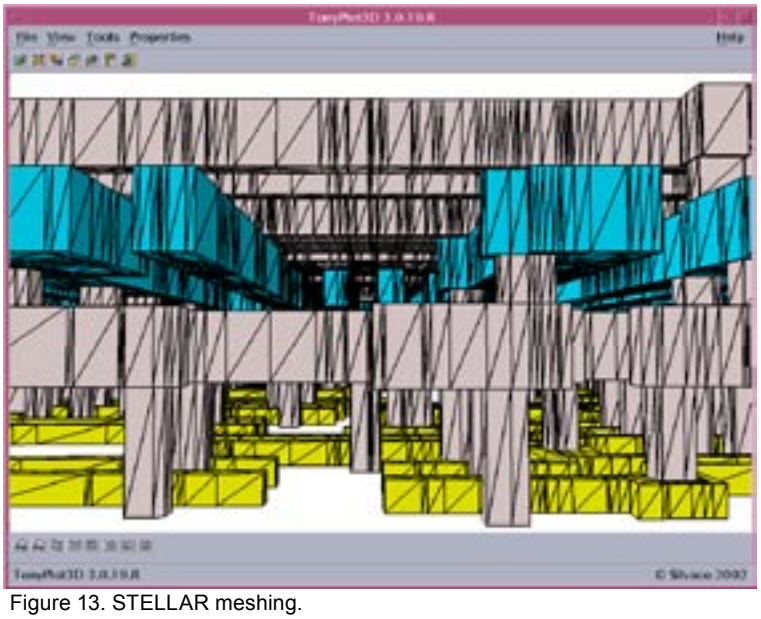

Figure 13. STELLAR meshing.

TCAD Simulation of a Dual Band Monolithic HgCdTe Infrared Photodetector

Introduction

Mercury cadmium telluride (HgCdTe) is a semiconductor material whose material properties are adjustable through altering its constitutive molar fractions. HgCdTe has found extensive use in optical detection, and in particular found wide use in infrared photodetectors over the past few decades. Applications in this area have been the main driving force for research on this material and for a good review see [1].

HgCdTe has an adjustable bandgap whose value can be altered by varying the stociometric ratio of Hg and Cd in the form $Hg_{(1-x)}Cd_xTe$. This property enables the detection of multispectral sources through the creation of multispectral infrared detectors of various bandgaps and in particular dual band photodetection [2]. Dual band photodetection in the medium wavelength infrared (MWIR) and long wave infrared atmospheric windows has been performed using HgCdTe photodiodes [e.g. 3] and for a recent example see [4]. This simulation standard will demonstrate the simulation of a dual band HgCdTe monolithic photodetector similar to [4]. The device is suitable for dual band on pixel registered infrared photodetector arrays in the atmospheric transmission window of 3-5μm and 8-12μm.

Device Description and Material Properties

The device is shown schematically in figure 1(a). The device consists of three layers of HgCdTe material with varying x and hence material bandgap situated on top of an CdTe IR transparent substrate. All HgCdTe layers are doped n type. Radiation between 2-5μm now referred to as MWIR (medium wavelength infrared) will pass through CdTe substrate and will not be absorbed due to the high bandgap energy of the CdTe material but will be absorbed by the HgCdTe material in layer 1. Radiation between 6 - 12μm now referred to as LWIR (long wavelength infrared) will also pass through the CdTe and in this case pass through layer 1 and layer 2 as it has insufficient energy to excite any electrons in these materials. However, radiation will be absorbed in layer 3 due to its smaller energy bandgap. As such it is intended that no LWIR or MWIR radiation be absorbed in layer 2, which has the widest bandgap and is referred to as an insulating layer. A simplified band diagram for the structure is shown in figure 1(b). As shown here, the presence of heterojunctions barriers in the valence band will prohibit the flow of photogenerated minority carriers between layers 1 and layer 3 thus confining them to their respective layers.

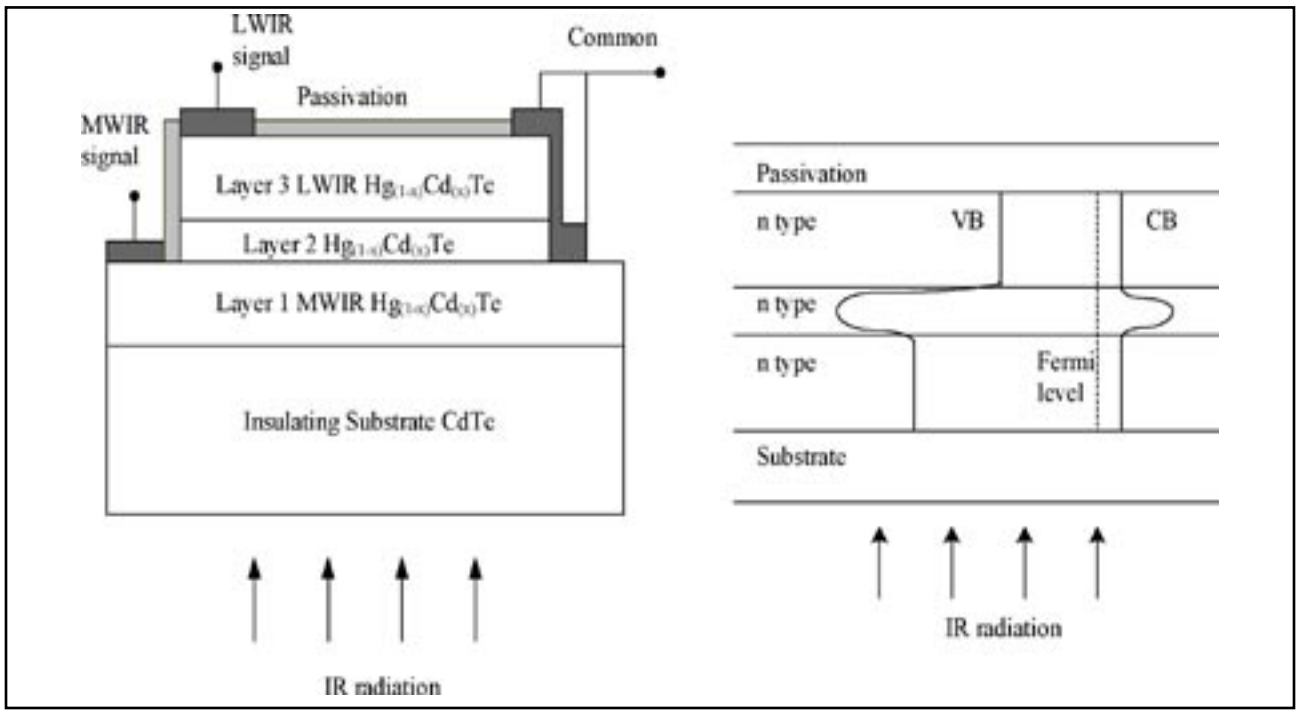

Figure 1 (a) Schematic diagram of dual band monolithic HgCdTe photodetector. (b) Energy band diagram for layer 1, layer 2 and layer 3.

The bandgap of HgCdTe is a function of the fraction of Cd in the composite material. A number of equations have been developed to summarize the empirically measured relationship and of popular choice is the expression developed by Hansen et al [5] which describes the energy bands in a parabolic form where

$$E_g = -0.302 + 1.93x - 0.810x^2 + 0.832x^3 + 5.35\times10^{-4}(1-2x)T \quad (1)$$

Here T is the temperature in degrees Kelvin and x is the molar fraction, E_g is the material bandgap in eV and x is the fractional composition value. With varying the value of x, the spectral response can be tailored to detect varying wavelengths. Consequently in order to detect long wavelength radiation, x must be altered accordingly resulting in a semiconductor having a very narrow bandgap. Applied formulae describing effective electron and hole masses are given in equations (2) and (3) respectively. The electron and hole mobilities are given by equations (4) and (5) respectively. The static dielectric constant is given in equation (6).

Here $\frac{m_e^*}{m_0} = m_e^{**}$ is the effective electron mass,

$\frac{m_h^*}{m_0} = m_h^{**}$ is the effective hole mass,

μ_e is the electron mobility in m^2/Vs, μ_h is the hole mobility in m^2/Vs and ε_s is the static dielectric constant.

$$\frac{m_e^*}{m_0} = m_e^{**} = \left[-0.6 + 6.333\left(\frac{2}{E_g} + \frac{1}{E_g + 1}\right)\right]^{-1} \quad (2)$$

$$\frac{m_h^*}{m_0} = m_h^{**} = 0.55 \quad (3)$$

$$\mu_e = 9\times10^4\left(\frac{0.2}{x}\right)^{7.5} T^{-2(0.2/x)^{10}} \quad (4)$$

$$\mu_h = 0.01\mu_e \text{ and} \quad (5)$$

$$\varepsilon_s = 20.5 - 15.5x + 5.7x^2 \quad (6)$$

Recombination models are also important to consider and in this example, Auger and radiative recombination are only considered. These expressions have been determined by Wenus et al [6] and have been used for the simulations presented here.

$$R_{Ae} = \left[2n_i^2 \frac{3.8\times10^{-18}\varepsilon_s^2\left(1+\frac{m_e^{**}}{m_h^{**}}\right)^{0.5}\left(1+2\frac{m_e^{**}}{m_h^{**}}\right)}{m_e^{**}(0.2)^2\left(\frac{kT}{E_g}\right)^{1.5}} \times \exp\left(\frac{\left(1+2\left(\frac{m_e^{**}}{m_h^{**}}\right)\right)\frac{E_g}{kT}}{1+\frac{m_e^{**}}{m_h^{**}}}\right)\right]^{-1} \quad (7)$$

$$R_{Ah} = R_{Ae}\left[\frac{6\left(1-\frac{5E_g}{4kT}\right)}{1-\frac{3E_g}{2kT}}\right]^{-1} \text{ and} \quad (8)$$

$$R_R = 5.8\times10^{-19}\varepsilon_s^{1/2}(m_e^{**}+m_h^{**})^{-1.5}(1+m_e^{**-1})\left(\frac{300}{T}\right)^{1.5} \times \left(\frac{E_g^2 + 3kTE_g}{q} + \frac{3.75k^2T^2}{q^2}\right) \quad (9)$$

The Auger recombination rate for electron and holes is given in equations (7) and (8) respectively. Optical recombination is expressed using equation (9). Here R_{Ae} is the Auger electron recombination coefficient in m^6/s, R_{Ah} is the Auger hole recombination coefficient in m^6/s, R_R is the radiative recombination coefficient in m^3/s, k is Boltzmann's constant, q is the electron charge and n_i is the intrinsic carrier concentration.

Of critical importance to modelling the absorption of incident radiation is the absorption coefficient. In general this property should be wavelength dependent in order to give realistic behavior similar to a real device. Direct bandgap semiconductors, such as HgCdTe, have a sharp onset of optical absorption as the photon energy increases above the bandgap of the material. The absorption coefficient used should therefore have similar properties to the material of choice.

$$\alpha = \frac{\sqrt{2c}}{\tau}\sqrt{\left[1-\frac{\lambda}{\lambda_g}\right]}\left(\sqrt{\frac{m_e^{**}\lambda}{h}}\right)^3 \quad (10)$$

The absorption coefficient is given in [7] and has been used in this work expressed in the form of equation (10). Here α is the absorption coefficient in m^{-1}, λ is the incident wavelength in meters, h is Plank's constant, τ is the electron lifetime in seconds, c is the speed of light and λ_g is the cut-off wavelength determined by the bandgap of the material.

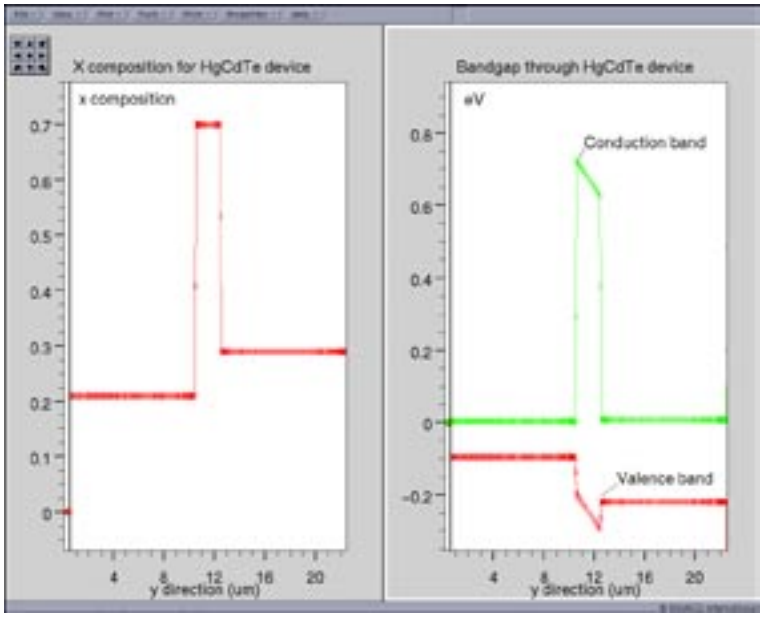

Figure 2. (a) One dimensional cutline showing fractional composition x through device. (b) Corresponding one dimensional cutline display for the energy band diagram through the device.

3 Device Simulations and Results.

ATLAS has been modified to include the mathematical definitions of the material parameters set out here. Each expression has been implicitly coded using the C-interpreter that is an ANSI C compatible environment consistent within the ***ATLAS*** framework. All calculations were performed at 77K. The photodiode was backside illuminated through the transparent CdTe substrate. Surface power density of incident radiation was set to 0.1W/cm^2. Each simulation was performed with the LWIR and MWIR electrode held at 0.1V with respect to ground.

Figure 2(a) shows the x compositional value through the device. Figure 2(b) shows the corresponding energy band diagram in eV for the x compositional values as based on equation (1). It is clear that three distinct energy bands are present. Layer 1 which has x=0.21 has the smallest band gap and is suitable for LWIR detection. Layer 3 which has x=0.29 has a larger band gap and is suitable for MWIR detection. Layer 2 has x=0.7 and as such has a significantly larger band gap thus acting as an electrically and optically isolating layer.

Figure 3 shows the photogeneration of electrons within the device for two different wavelengths. It is clear that two distinct cases are present. At a wavelength of 4.5μm the photogeneration rate is approximately three orders of magnitude higher in the MWIR detector compared to the LWIR detector. As the wavelength is increased to 9.5μm, the photogeneration rate in the MWIR detector is reduced. In contrast to this, the photogeneration rate in the LWIR detector with the lowest fractional compositional of x is seen to increase dramatically. Figure 4 details the spectral response of the device. It is clear that two distinct areas of device responsivity exist. As the wavelength is increased from 0um the current in the MWIR detector increases. This current reaches a maximum at approximately 5um then falls sharply to a smaller value. In contrast, the LWIR response in negligible in the wavelength range 0 to 5 um. As the wavelength is increased further the LWIR detectors response increases and reaches a maximum at approximately 9.5 um. The LWIR current then reduces in a similar fashion as the MWIR detector.

4 Conclusion

A dual band monolithic HgCdTe material has been successfully simulated and is shown to be capable of detecting infrared radiation. It is clear that two distinct bands of radiation, medium wavelength infrared 2-5 um and long wavelength infrared 5-12 um are easily detectable using the device described here. Non-standard expressions have been incorporated into the simulation domain

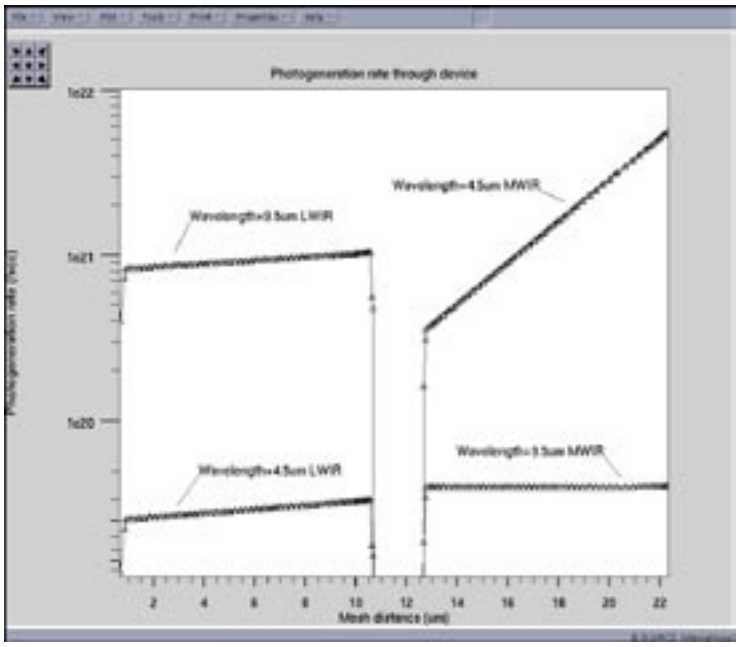

Figure 3. One dimensional cutline showing photo generated carriers within the LWIR and MWIR detector for 4.5μm and 9.5μm of incident radiation.

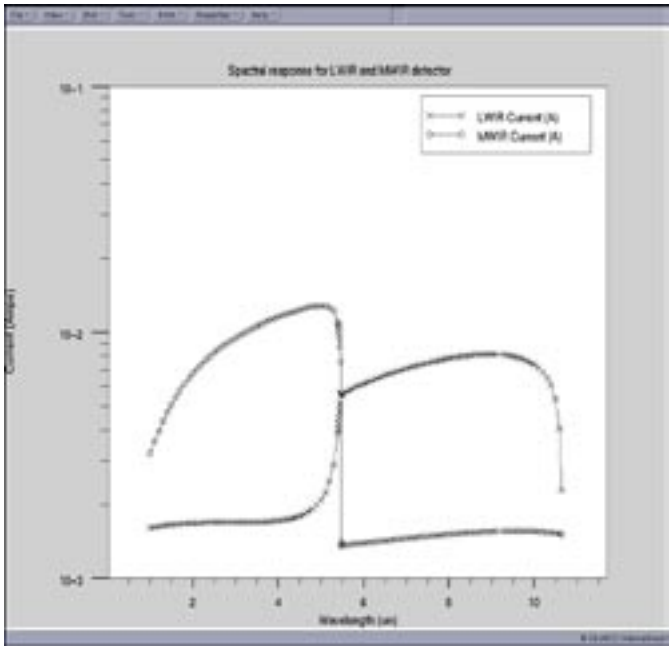

Figure 4. Spectral response of LWIR and MWIR current as a function of wavelength.

through the use of a ANSI C c-interpreter which has a seamless link with ***ATLAS***. Effective simulations have been incorporating advanced expressions for recombination mdels as a function of compositional fraction.

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...continued from page 6

shown in the 3D picture), and 45 degrees angled routing metallization (Figure 13).

The next picture shows a zoom over the backend structure side. Meshing has been overlaid to the interconnect structure (Figure 13).

The parasitics netlist has been computed in less than 55 minutes for this structure with a maximum memory use of 121Mb.

Another large layout has been inputted to ***STELLAR***, with an even larger size (153x113 um2).

Due to the large size of the layout, and the complex process used for generating the 3D backend process (4 metallization layers in this case plus multi dielectric materials), this structure will take advantage of the halo filtering technique and domain decomposition methodology. Such a large structure, with more than 5000 transistors has been successfully simulated with ***STELLAR***, giving the parasitics netlist (more than 40000 capacitances) in 36 hours, with a maximum memory use of less than 1Gb.

Conclusion and Perspectives

This paper has demonstrated ***STELLAR's*** ability to extract parasitic capacitances from large layouts. The numerical scheme and new meshing algorithm efficiency has been emphasized through comparisons with already existing SILVACO tools (***QUEST***, ***CLEVER***) and with measurements over manufactured devices.

This validates ***STELLAR*** initial targets, i.e. handling structures bigger than the ones input to ***CLEVER***, and smaller than the ones the full chip extractor ***HIPEX*** uses.

This does not mean that this TCAD based approach has to be limited to middle range layouts, and that's why the input range is being extended, since the next target is to develop a parallel scheme that will allow ***STELLAR*** to input even larger layouts.

Acknowledgements:

SILVACO wishes to thank LETI for its collaboration to this work.

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LPE Optimization with *CLEVER/HIPEX/EXACT* Linkage Methodology

1. Introduction

On the cutting edge of LSI design, the accuracy of Layout Parasitic Extraction (LPE) tools is a critical issue to miniaturized LSI design of rules measuring 0.13 um or lower. The quantitative consideration of coupling capacitance based on three-dimensional calculation is indispensable. Conventional advanced LSI design tools and methodology are limited in their ability to optimize the LPE library. As a result, the discussion of LPE tool accuracy and extracted parasitic results lack significant quantitative generality.

This article proposes a new methodology for verifying accuracy of LPE tools and optimizing the LPE library for today's 0.13 um designs and the more scaled-down next generation LSI design of nodes at 100 nm or less.

2. Simulation Flow and Methodology

Figure 1 is a LPE optimization simulation flow that links Silvaco's ***CLEVER***, ***HIPEX***, and ***EXACT*** tools. The process includes four distinct stages.

- **Stage One** - Extract: ***HIPEX***, Silvaco's hierarchical full-chip LPE tool, extracts nets and compares them to the defined layout. The thickness of each layer is also defined at this stage with the ***EXACT*** layout editor
- **Stage Two** - Simulate: ***CLEVER*** extracts particular net information through a three-dimensional simulation and exports the SPICE netlist to ***HIPEX*** 1],[2]. ***CLEVER's*** focus on detailed process conditions delivers high-accuracy extraction results that enables virtual fabrication to replace TEG fabrication [3]

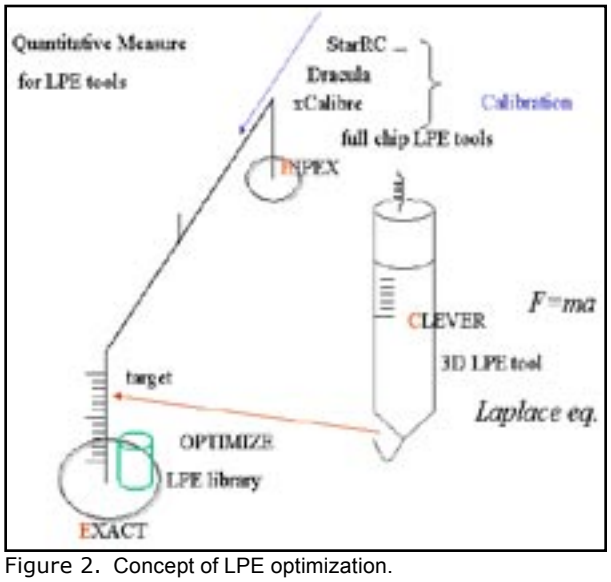

Figure 2. Concept of LPE optimization.

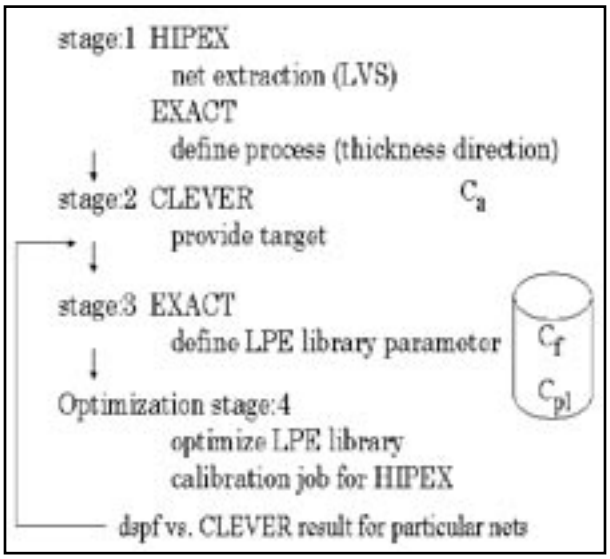

Figure 1. Simulation flow of ***CLEVER/HIPEX/EXACT*** Linkage Methodology.

- **Stage Three** - Convert: ***EXACT*** [4] coverts the input information into an LPE library for import to ***HIPEX***
- **Stage Four** - Optimize: During this stage, ***HIPEX*** executes several calibration jobs in an iterative loop based on parameter information (the LPE library prepared during Stage 3) and target benchmarks (simulated in Stage 2). The results of calibration run results are output to a DSPF. This crucial stage is detailed in the following sections

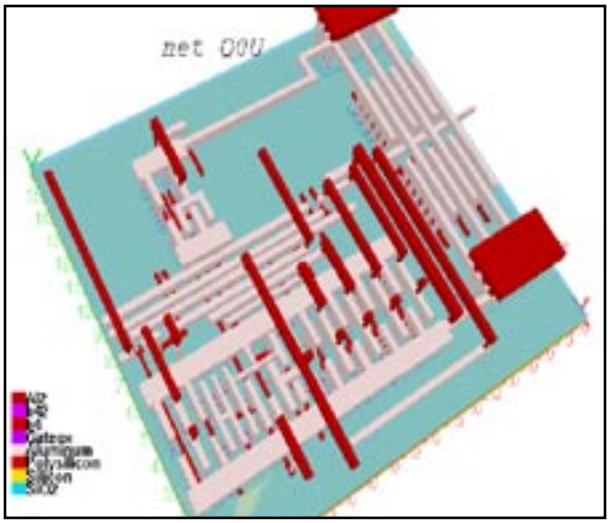

Figure 3. CLEVER simulation result showing three dimensional interconnect structure for the part corresponding to net Q0U. Net Q0U is almost crossing like + shape through this structure.

3. LPE Library Optimization

CLEVER distinguishes itself from other LPE methodologies by providing highly accurate parasitic capacitance and resistance targets for LPE library optimization (Figure 2). To demonstrate the accuracy of the ***CLEVER*** methodology, we will examine an example of a design rule scaled from 0.5um down to 0.13um.

Figure 3 is a ***CLEVER*** simulation that shows a portion of a 0.13um design rule. Coupling capacitance (Cpl) is a primary concern in a miniaturized design, so it is selected as optimization parameter. In this case, the same process condition is used for three different design rules.

4. Scaling Effect on Parasitic Capacitance

Table 1 shows the result of simulation after optimization. Four nets were selected and capacitance was extracted and compared for each scaled design. The table breaks simulated capacitance down to three components: Ca [fF/um2], Cf [fF/um], and Cpl [fF]. The simplicity respective contribution ratio (%) to DSPF is also reported.

Capacitance components are analyzed in comparison to those extracted by ***CLEVER***.

Figure 4 shows comparison of the optimized Cpl – space curve according to three different design rules. The contribution of coupling capacitance increases with scale and is dominant in Table 1 and Figure 4. However, if Cpl is decreased, or scaled down, the reported errors may fluctuate wildly between different nets, even after the optimization process. This is because ***CLEVER*** considers the Cpl contribution on each respective net, reflecting each different three-dimensional situation. In the table, net RCQ is a special reference net that is designed with the same scale (0.13um) throughout.

0.5um (scale=1) net	54	D0	Q0U	RGQ(for ref. **)	
Ca (overlap cap.)	42	31	40	34	%
Cf (fringe cap.)	49	53	47	60	%
Cpl (coupling cap.)	9	16	13	6	%
error compared to CLEVER	32	25	34	47	% *)
CLEVER (target value)	4.63	6.06	13.68	7.11	fF
0.25um (scale=0.5)					
Ca (overlap cap.)	19	11	16	16	%
Cf (fringe cap.)	43	38	38	55	%
Cpl (coupling cap.)	38	51	46	29	%
error compared to CLEVER	35	10	17	49	% *)
CLEVER (target value)	2.73	3.49	6.68	4.72	fF
0.13um (scale=0.25)					
Ca (overlap cap.)	7	4	6	10	%
Cf (fringe cap.)	30	29	30	47	%
Cpl (coupling cap.)	63	67	64	43	%
error compared to CLEVER	27	5	10	51	% *)
CLEVER (target value)	1.73	2.27	3.91	4.00	fF

*) error definition
{CLEVER - (Ca+Cf+Cpl)}/CLEVER

Table 1. Simulated capacitance.

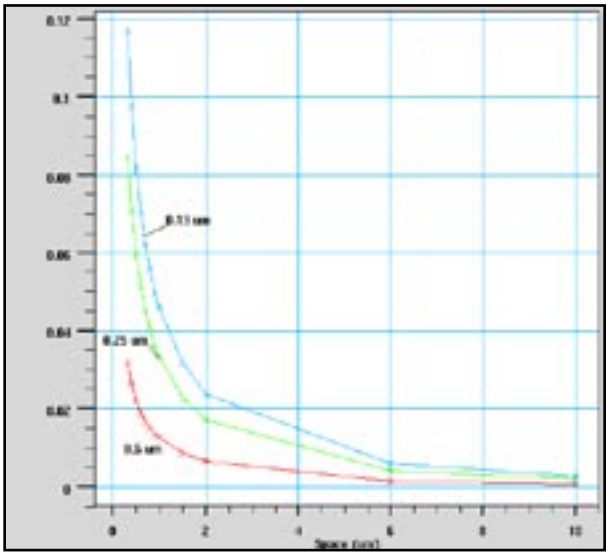

Figure 4. Optimized Cpl – space curve for Metal1 comparing three different design rules

5. Conclusion

Silvaco's optimized approach is ideal for obtaining reasonable and accurate LPE results. This method offers the following advantages:

Quantitative LPE extraction is possible when considering the three-dimensional effect and coupling capacitance effect, which are dominant with miniaturization and high integration of LSI, along with either advanced or heterogeneous process technology integration.

CLEVER's quantitative optimization target provides a physical base on which to analyze various complicated design cases with the proposed methodology.

High optimization of LPE library.

Accuracy verification of LPE extraction results.

The consistency and quality that results from this methodology fully realizes the promise of "TCAD Driven CAD".

References

[1] Simulating Accurate 3D Geometries for Interconnect Parasitic Extraction using ***CLEVER***, *Simulation Standard* August 98

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Calendar of Events

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Bulletin Board

Silvaco at DAC:

A/MS Simulation, Full-Chip Parasitic Extraction, RF Simulation, Library Characterization and Single Event Effect Reliability

Live demonstrations of Silvaco's software products will include:

- ***Harmony-AMS*** Analog/Mixed-Signal Simulation Platform delivers unsurpassed accuracy and productivity. ***Harmony-AMS*** is based on the ***Silos*** Verilog and ***SmartSpice*** Circuit simulators integrated into a single-kernel simulator that fully supports Verilog-AMS, Verilog, Verilog-A, and SPICE.
- ***SmartSpice-RF*** Harmonic Balance-Based Simulator provides a complete set of steady-state analyses to design GHz range RF wireless application ICs. ***QUEST*** High Frequency Parasitic Extractor accurately characterizes RF inductors, capacitors, resistors and transmission lines.
- ***HIPEX*** Full-Chip Parasitic Extraction products perform 3D-accurate and 2D-fast extraction of parasitic capacitors and resistors from hierarchical layouts into transistor-level netlists.
- Schematic Driven Layout Design Flows with ***Gateway*** Schematic Editor driving the ***SmartSpice*** Circuit Simulator, ***Expert*** Layout Editor, ***Guardian*** DRC/LVS/LPE, and ***HIPEX*** parasitic extraction tools supported by Silvaco's process design kits.
- Library Characterization with ***SmartCell*** and ***SmartCore*** Characterization Tools generate the accurate timing and power models required by leading synthesis, HDL simulation, routing, and analysis tools.

If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

Robin Jones Ph.D., Senior Applications and Support Engineer

Q. When solving for the static CV curve for a MOS capacitor, due to the absence of current carriers, convergence can be a real problem. Previous methods suggested in the hints and tips archive of Silvaco's simulation standard have made use of Silvaco's *Luminous* module where a small amount of light intensity is incident on the device, the idea being to generate a small amount of carriers to aid convergence.

A recent addition to Silvaco's device simulator has supplanted such means for the use of ***Luminous*** in generating the static CV curve for a MOS capacitor.

Use is made of the QSCV term in addition to the NOCURRENT term to the SOLVE statement to give the Quasi-static capacitance of the electrode being bias-ramped. This also includes electrodes linked to the electrode being bias ramped via the COMMON parameter of the CONTACT statement.

This will output capacitance summed over electrodes and capacitance for each common electrode. They are calculated by numerically differentiating charge on each contact with respect to the applied bias, and so a fine voltage increment is required for accurate results.

Such a solve statement can be described as follows:

```
solve init
solve vanode=0 vstep=0.25 vfinal=10.0
name=anode
log outfile=CV_AlGaAs_qscv.log
solve vanode=10.0 vstep=-0.1 vfinal=-10
name=anode qscv nocurrent
log off
```

giving the following CV curve for a generated MOS capacitor:

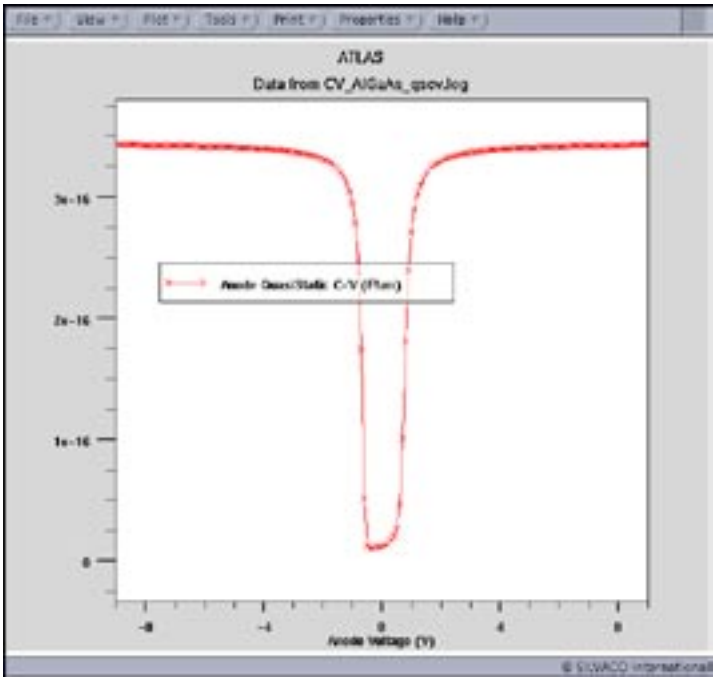

Figure 1. CV curve for MOS capacitor.

Q. Can a previously created structure, once loaded into *ATLAS*, have any of its REGION properties modified without having to recreate the complete structure?

A. If a previously created structure is loaded into ***ATLAS*** using the MESH INFILE statement properties of each individual region within the structure can now be modified. A recent addition to the REGION statement is the key word MODIFY. Use of the MODIFY statement provides a very convenient method for easily changing structure properties. By specifying MODIFY on the REGION statement any of the following parameters may be applied to that region:

```
MATERIAL, DONORS, ACCEPTORS, X.COMPOSE,
Y.COMPOSE, WELL.CNBS, WELL.VNBS, WELL.NY,
WELL.NX, WELL.GAIN, WELL.OVERLAP,
PIEZO.SCALE, QWELL, LED, WELL.FIELD,
PIEZOELEC FIXED.FERMI, and CALC.STRAIN.
```

An example highlighting the use of such a statement is given below. The example makes use of a previously created structure called xcomp035.str in which the x.comp value for the AlGaAs is 0.35. Use is then made of the MODIFY keyword to change this value in both of the regions.

Figure 2 shows the before and after structure property of the x.comp parameter obtained by taking a one dimensional cut line through the structure in ***TonyPlot***. Use of the MODIFY statement provides a very convenient method for easily changing structure properties.

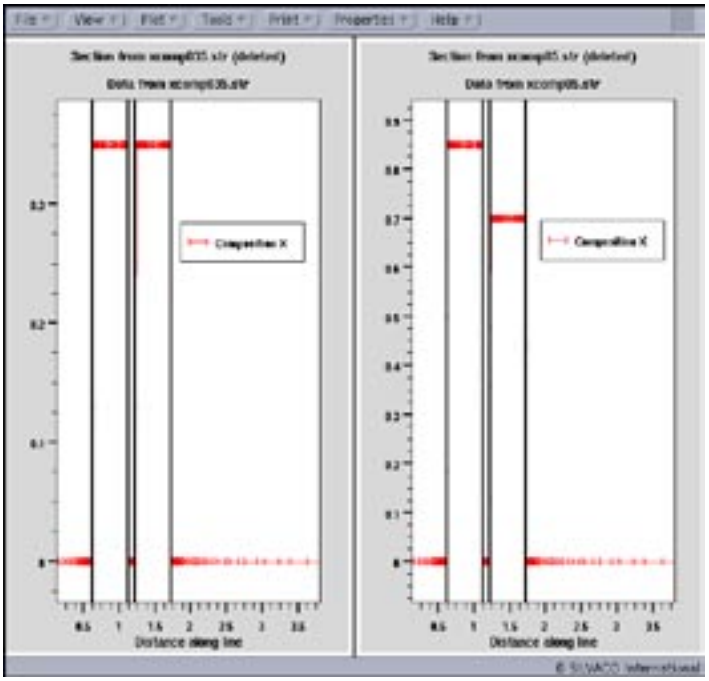

Figure 2. x.comp variation before and after modify statement.

Q. I am familiar with the functionality of *ATLAS* allowing a 1D doping profile to be specified and loaded into a structure, can I perform the same operation with a 2D doping profile?

A. The ability for a 2D doping profile to be loaded into ***ATLAS*** is made possible by the addition of the 2D.ASCII keyword to the DOPING statement. This loads a 2D doping profile defined on a rectangular Cartessian grid from a file specified by INFILE. The 2D.ASCII keyword must be specified along with either the N.TYPE, P.TYPE or NET parameter. The ASCII 2D doping profile data file must also be formatted correctly. The first column in the ASCII file must contain the x coordinates, the second column in the file must contain the y coordinates and the third column contains the doping data. An example for such a doping statement is given below together with the relevant 2D doping ASCII data file.

```
doping num=1 conc=1e15 p.type uniform
doping 2d.ascii infile=doping2d.dat
n.type
```

doping.dat:

```
0.4 0.0 1.0e18
0.4 0.1 1.0e18
0.4 0.2 1.0e18
0.5 0.0 2.0e18
0.5 0.1 2.0e18
0.5 0.2 2.0e18
0.6 0.0 3.0e18
0.6 0.1 3.0e18
0.6 0.2 3.0e18
```

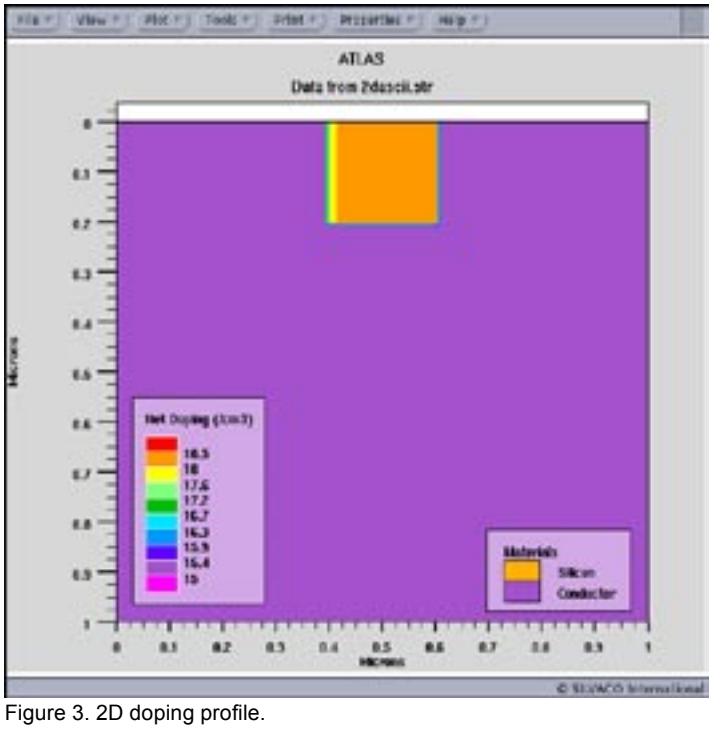

Figure 3. 2D doping profile.

Figure 3 shows the resultant pn junction formed by such a doping statement.

Call for Questions

If you have hints, tips, solutions or questions to contribute,
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