LPE Optimization with *CLEVER/HIPEX/EXACT* Linkage Methodology

1. Introduction

On the cutting edge of LSI design, the accuracy of Layout Parasitic Extraction (LPE) tools is a critical issue to miniaturized LSI design of rules measuring 0.13 um or lower. The quantitative consideration of coupling capacitance based on three-dimensional calculation is indispensable. Conventional advanced LSI design tools and methodology are limited in their ability to optimize the LPE library. As a result, the discussion of LPE tool accuracy and extracted parasitic results lack significant quantitative generality.

This article proposes a new methodology for verifying accuracy of LPE tools and optimizing the LPE library for today's 0.13 um designs and the more scaled-down next generation LSI design of nodes at 100 nm or less.

2. Simulation Flow and Methodology

Figure 1 is a LPE optimization simulation flow that links Silvaco's ***CLEVER***, ***HIPEX***, and ***EXACT*** tools. The process includes four distinct stages.

- **Stage One** - Extract: ***HIPEX***, Silvaco's hierarchical full-chip LPE tool, extracts nets and compares them to the defined layout. The thickness of each layer is also defined at this stage with the ***EXACT*** layout editor
- **Stage Two** - Simulate: ***CLEVER*** extracts particular net information through a three-dimensional simulation and exports the SPICE netlist to ***HIPEX*** 1],[2]. ***CLEVER's*** focus on detailed process conditions delivers high-accuracy extraction results that enables virtual fabrication to replace TEG fabrication [3]

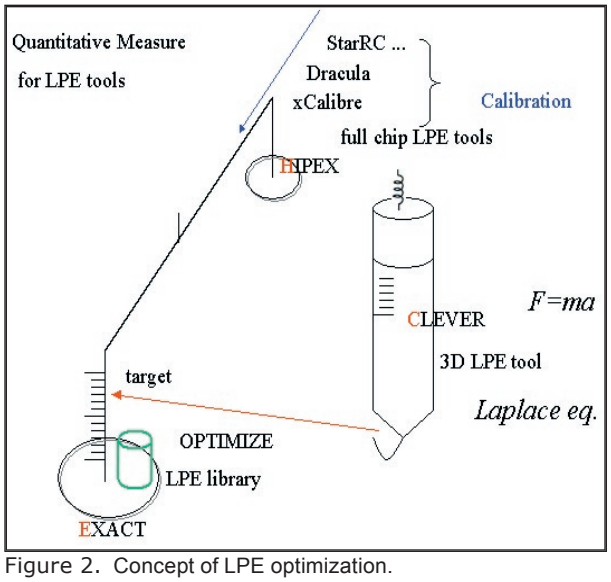

Figure 2. Concept of LPE optimization.

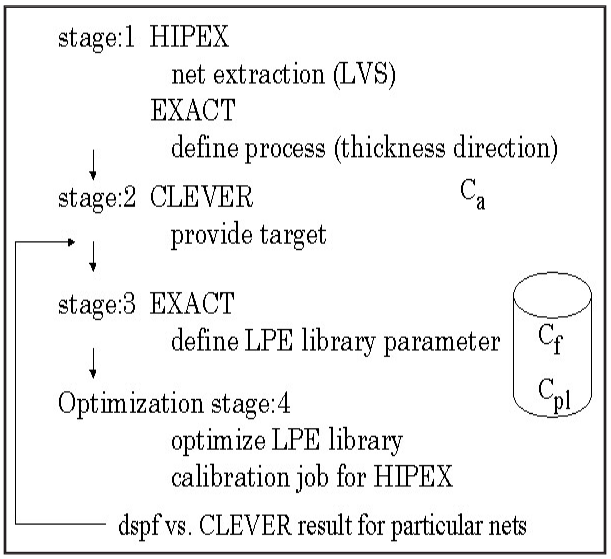

Figure 1. Simulation flow of ***CLEVER/HIPEX/EXACT*** Linkage Methodology.

- **Stage Three** - Convert: ***EXACT*** [4] coverts the input information into an LPE library for import to ***HIPEX***
- **Stage Four** - Optimize: During this stage, ***HIPEX*** executes several calibration jobs in an iterative loop based on parameter information (the LPE library prepared during Stage 3) and target benchmarks (simulated in Stage 2). The results of calibration run results are output to a DSPF. This crucial stage is detailed in the following sections

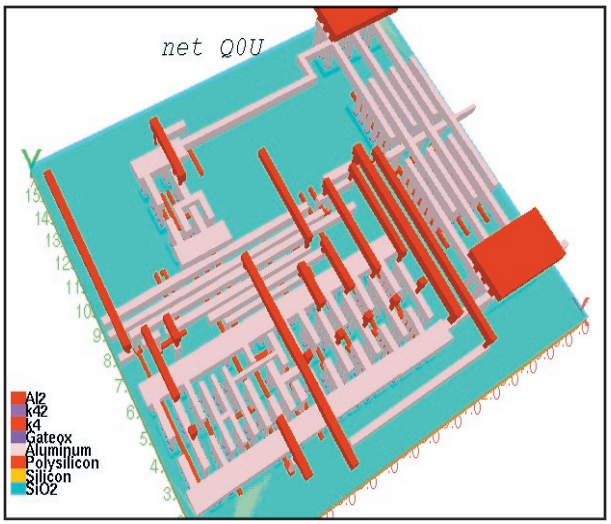

Figure 3. CLEVER simulation result showing three dimensional interconnect structure for the part corresponding to net Q0U. Net Q0U is almost crossing like + shape through this structure.

3. LPE Library Optimization

CLEVER distinguishes itself from other LPE methodologies by providing highly accurate parasitic capacitance and resistance targets for LPE library optimization (Figure 2). To demonstrate the accuracy of the ***CLEVER*** methodology, we will examine an example of a design rule scaled from 0.5um down to 0.13um.

Figure 3 is a ***CLEVER*** simulation that shows a portion of a 0.13um design rule. Coupling capacitance (Cpl) is a primary concern in a miniaturized design, so it is selected as optimization parameter. In this case, the same process condition is used for three different design rules.

4. Scaling Effect on Parasitic Capacitance

Table 1 shows the result of simulation after optimization. Four nets were selected and capacitance was extracted and compared for each scaled design. The table breaks simulated capacitance down to three components: Ca [fF/um2], Cf [fF/um], and Cpl [fF]. The simplicity respective contribution ratio (%) to DSPF is also reported.

Capacitance components are analyzed in comparison to those extracted by ***CLEVER***.

Figure 4 shows comparison of the optimized Cpl – space curve according to three different design rules. The contribution of coupling capacitance increases with scale and is dominant in Table 1 and Figure 4. However, if Cpl is decreased, or scaled down, the reported errors may fluctuate wildly between different nets, even after the optimization process. This is because ***CLEVER*** considers the Cpl contribution on each respective net, reflecting each different three-dimensional situation. In the table, net RCQ is a special reference net that is designed with the same scale (0.13um) throughout.

0.5um (scale=1) net	54	D0	Q0U	RGQ(for ref. **)	
Ca (overlap cap.)	42	31	40	34	%
Cf (fringe cap.)	49	53	47	60	%
Cpl (coupling cap.)	9	16	13	6	%
error compared to CLEVER	32	25	34	47	% *)
CLEVER (target value)	4.63	6.06	13.68	7.11	fF
0.25um (scale=0.5)					
Ca (overlap cap.)	19	11	16	16	%
Cf (fringe cap.)	43	38	38	55	%
Cpl (coupling cap.)	38	51	46	29	%
error compared to CLEVER	35	10	17	49	% *)
CLEVER (target value)	2.73	3.49	6.68	4.72	fF
0.13um (scale=0.25)					
Ca (overlap cap.)	7	4	6	10	%
Cf (fringe cap.)	30	29	30	47	%
Cpl (coupling cap.)	63	67	64	43	%
error compared to CLEVER	27	5	10	51	% *)
CLEVER (target value)	1.73	2.27	3.91	4.00	fF

*) error definition
{CLEVER - (Ca+Cf+Cpl)}/CLEVER

Table 1. Simulated capacitance.

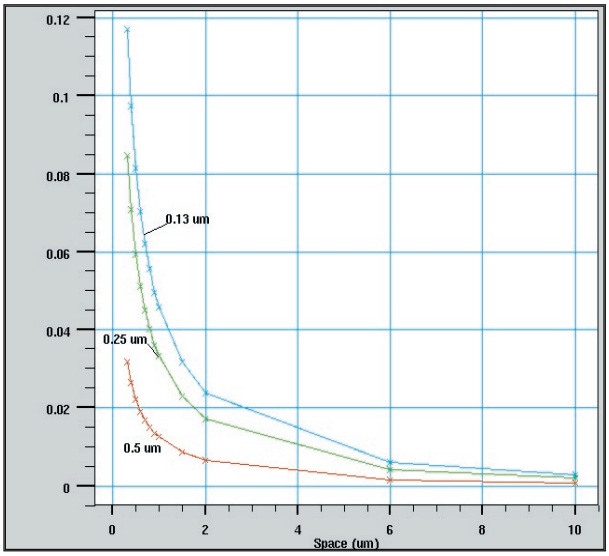

Figure 4. Optimized Cpl – space curve for Metal1 comparing three different design rules

5. Conclusion

Silvaco's optimized approach is ideal for obtaining reasonable and accurate LPE results. This method offers the following advantages:

Quantitative LPE extraction is possible when considering the three-dimensional effect and coupling capacitance effect, which are dominant with miniaturization and high integration of LSI, along with either advanced or heterogeneous process technology integration.

CLEVER's quantitative optimization target provides a physical base on which to analyze various complicated design cases with the proposed methodology.

High optimization of LPE library.

Accuracy verification of LPE extraction results.

The consistency and quality that results from this methodology fully realizes the promise of "TCAD Driven CAD".

References

[1] Simulating Accurate 3D Geometries for Interconnect Parasitic Extraction using ***CLEVER***, *Simulation Standard* August 98

[2] Validation of ***CLEVER*** Interconnect Parasitics with 0.18 um Process Measurements, *Simulation Standard* November 98

[3] G. Lecarval, et.al., Advanced Interconnect Scheme Analysis: Real Impact of Technological Improvements, IEDM 98, 31-3, p837, 1998

[4] Generating a Capacitance Coefficient Database for any Chip Level LPE Tool Using ***EXACT***, *Simulation Standard* August 99