Simulation Standard

Connecting TCAD To Tapeout

A Journal for CAD/CAE Engineers

New Features in *Expert* Node Probing

Introduction

Expert's Node Probing is powerful tool for inspection of netlist components on layout. It is designed for highlighting layout objects electrically connected with each others.

The additional features of Node Probing have been added in the new QT version of ***Expert***. Because the layout extraction is being performed by hierarchical Guardian LPE, the user has possibility to get hierarchical node names troughout node tracing. The original net name in cell instance is keeping and is displaying aditionally to net name from top cell.

Short Locator is another new feature in Node Probing. This feature simplifies connectivity investigation and shorts searching on layout.

Hierarchical Net Names

The Node Probing in preivious versions of ***Expert*** was designed to trace electricallly connected nodes throughout the hierarchy of a cell[1]. But, because ***Expert*** used the ***Maverick*** netlist extractor, which works on flatten layout only, the names of nets can be taken from flatten top cell. The original net names in low levels of hierarchy became unavailable.

New version of ***Expert*** uses hierarchical netlist extractor ***Guardian LPE***. For hierarchical extraction the original net names in cells instances are stored and are displayed when net is traced in Node Probing. This feature helps to check the hierarchical connectivity and to find possible wrong connection.

Below there is an example which demonstrates this feature. The part of hierarchical netlist is shown Figure 1 a. Subcircuit "TRA48" contains instances of "DFFC" and "OR2" subcircuits. Net with name "D1" in top subcircuit "TRA48" is connected to pin "D" of XI15 instance of "DFFC" subcircuit and to pin "Y" of XI5 instance of "OR2" subcircuit. So during net tracing in Node Probing we should see these net names for objects from different instances. Figures 1 b,c,d show the highlighted net, which has name "D1" in top cell "TRA48" and names "D" and "Y" in instances of "DFFC" and "OR2".

Figure 1a. The part of hierarchical netlist. Netlist corresponds to layout on Figure 1 b,c,d.

Continued on page 2 ...

INSIDE

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Figure 1b. Highlighted net obtained name "D1" from top cell TRA48.

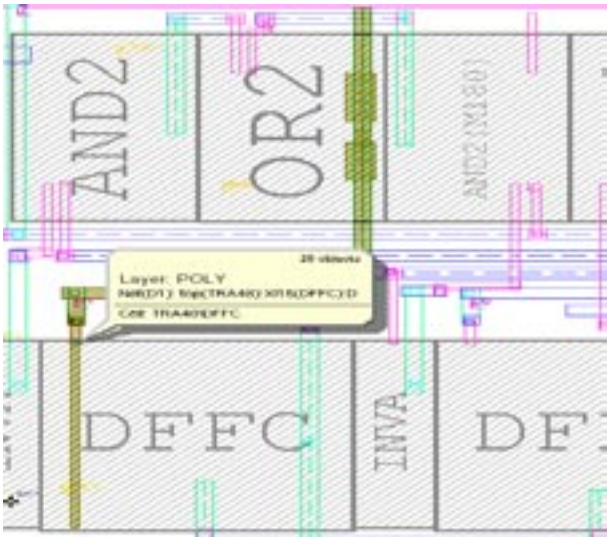


Figure 1c. Highlighted net "D1" has name "D" in the instance XI15 of cell DFFC.

Short Locator

Short Locator is a new feature of the Node Probing in ***Expert***. It permits to simplify search of shorts in layout. Short Locator is based on well known Dijkstra's algorithm for shortest-paths problem [2].

Short Locator works with the net selected by Node Probing. To build a graph for Dijkstra's algorithm the geometrical objects from highlighted net are splitted into set of trapezoids. The trapezoids from one layer touch each other but don't overlap. The middle points of common parts of edges of these trapezoids became graph vertexes. Each set of connected objects from one layer produces own subgraph. Subgraphs are combined to one graph using additional graph vertexes which are centers of overlapping area of two trapezoids from diffrent connected layers.

Figure 2 shows small example. There are three layers M1, M2 and Contact. Layer M1 has electrical connection with layer Contact and layer M2 has electrical connection with layer Contact too, but there is no direct connection between M1 and M2. Wire from layer M1 is splitted to 3 trapezoids and wire from layer M2 is splitted to 2 trapezoids. The orginal graph consists from 4 points A,B,C,D. Points 1 and 2 are added to graph when short path between these points are searched.

Really Short Locator builds the shortest paths between sequentinal pairs of points on selected net. To run Short Locator user should at first select net in Node Probing. When selected net has been highlighted, Short Locator can be run trough menu "Verification"/"Node Probing"/ "Short Locator". Clicks on left mouse button set points for short path search. The point input is finished by click on right mouse button. When points are set, Short Locator attempts to build short paths between sequentinal pairs of points, like point1 - point 2, point 2 - point 3, and so on.

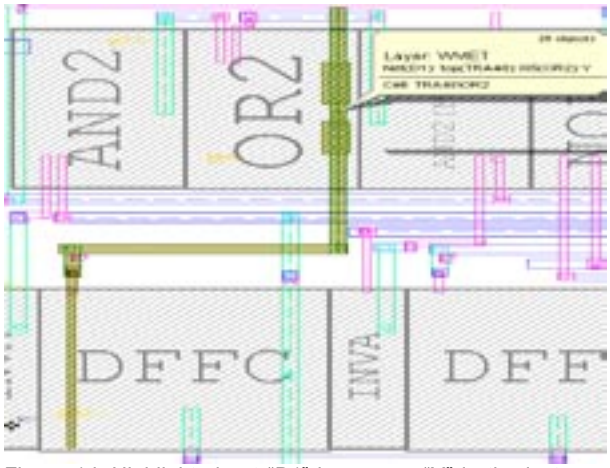


Figure 1d. Highlighted net "D1" has name "Y" in the instance XI5 of cell OR2.

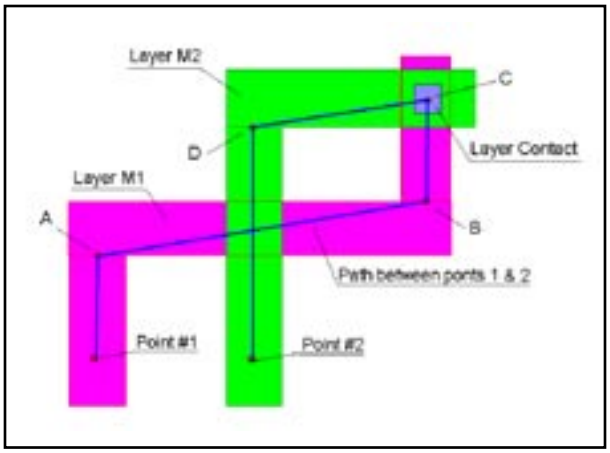


Figure 2. Path between point1 and 2. A, B, C, D are vertexes of graph which is used by Dijkstra's algorithm.

Figure 3a. First net "Q0" in original layout.

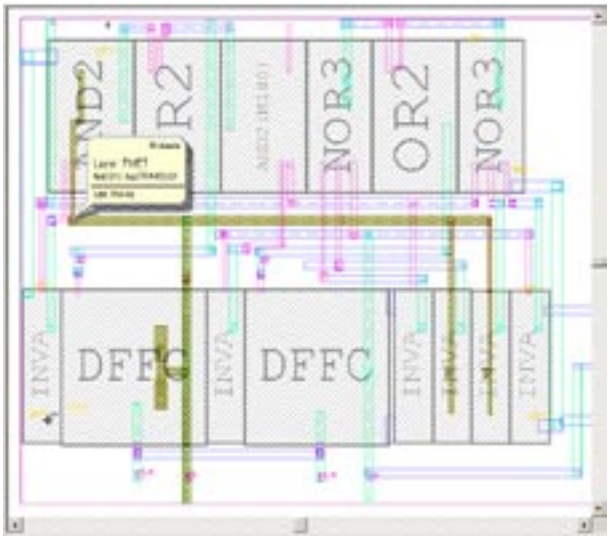


Figure 3b. Second net Q1 in original layout.

Some kinds of single shorts between two nets can be detected by building short paths between 3 points. If we know what objects should belong to different nets on shorted net, we can set first and third points on objects from one net, and second point on the object from onother net. Short locator will build two paths between first and second points, and between second and third points. Because it is single short, the both paths will go through this short and will have the common part along second net. If first and third points are placed in different ends of the first net, there is good probability that the paths will split in the place of short, and, so short will be detected very simple.

Figure 3 illustrates this feature. Figures 3 a and 3 b show two different nets in original layout. These two nets are shorted in modified layout, see Figure 3 c. Figure 3 d shows the shortest paths between 3 points. The short is located in place where shortest paths are splitted.

Conclusion

Node Probing tool in ***Expert*** Layout Editor obtained new features, that make it more powerfull. Hierarchical net naming and Short Locator are intended to simplify and accelerate layout debugging.

References

1 ."Expert: Recent Improvements in Hierarchical Layout Inspection", Simulation Standard, Volume 11, Number 9, September 2000.

2. Cormen, T. H.; Leiserson C. E.; & Rivest R. L. (1990) Introduction to Algorithms. MIT Press. ISBN 0-262-03141-8

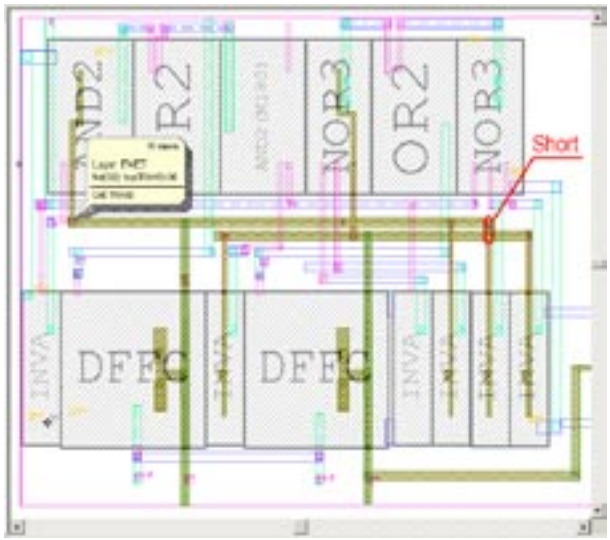


Figure 3c. Net in modified layout, which obtained from two original nets by shortening. Place of short is shown in circle.

Figure 3d. Shortest paths between points 1,2 and 2,3. Shortest paths are splitted in the place of the short.

Parasitic Capacitance Extraction with HIPEX and EXACT

Overview

To extract parasitic capacitances from a circuit layout, you need to perform the following steps:

1. Define the technology process and material data. This includes vertical order of mask layers and dielectrics, their thicknesses, conductivity, and permittivity constants.
2. Use the technology data as input to a 2D or 3D field solver to obtain capacitance coefficients.
3. Generate a rule file for a full-chip capacitance extractor using the obtained capacitance coefficients.
4. Run the capacitance extractor using the generated rule file.

Silvaco provides tools for performing all the steps above. You can use ***EXACT*** for steps from 1 to 3 and ***HIPEX-C*** for step 4.

EXACT is a 3D field solver powered by a 3D process simulator to accurately represent the cross-sections in the physical chip, rather than using square cross-sections. This maximizes the accuracy of the capacitance coefficients because the calculated capacitance is derived from realistic cross-sections and 3D shapes. See [1] for more information.

HIPEX-C is a full-chip parasitic capacitance extractor. It is a part of the ***HIPEX*** full-chip extractor, which also includes the layout netlist extractor, ***HIPEX-NET***, and the parasitic RC extractor, ***HIPEX-RC***. ***HIPEX-C*** works with a stripe database produced by ***HIPEX-NET***. This database divides the original layout into stripes making parallel processing possible. The stripes also make it easier to process huge layouts on a single host machine, one stripe at a time. ***HIPEX-C*** is a fast 2D extractor. It uses third-party coefficients to derive capacitance from the extracted parameters of parasitic area, length, and distance. See [2–3] for more information.

Built-in Model

HIPEX-C, as well as the most full-chip capacitance extractors, considers the following parasitic capacitance effects:

- Area capacitance is a surface-to-surface capacitance between two overlapping polygons on different layers (see A in Figure 1).
- Fringe capacitance is an edge-to-surface capacitance between two overlapping polygons on different layers (see Fu and Fd in Figure 1). The limit case of a fringe capacitance is a capacitance between exactly coincident edges (see Fc in Figure 1).
- Lateral capacitance is an edge-to-edge capacitance between two adjacent polygons on the same or different layers (see L1 and L2 in Figure 1).

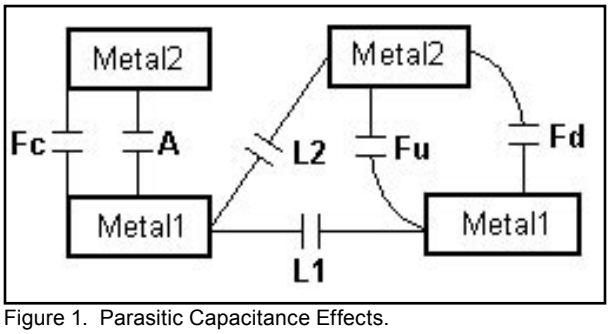


Figure 1. Parasitic Capacitance Effects.

In ***EXACT***, you use a combination of test structures to extract the coefficients for all the parasitic capacitance effects. Each of the test structures is specifically designed to highlight one of the three effects. The coefficients can then be mapped directly to ***HIPEX-C*** (or any other full-chip parasitic tool) extraction statements. ***EXACT*** provides powerful scripting capabilities to convert numeric results generated by the 3D field solver to a rule file for a full-chip extractor. ***EXACT*** comes with a set of ready-to-use scripts that generate rule files for the most popular full-chip extractors, including ***HIPEX-C*** from Silvaco.

Table 1 shows the coefficients, which ***EXACT*** calculates for ***HIPEX-C*** extraction statements (layer1 is above layer2).

All the coefficients, except K_area, are functions of lateral distance D. The area coefficient is a constant. For the lateral coefficient, the following equation is used:

K_lateral = n1 / (D + n2)^n3.

For all the fringe coefficients (K_fringe_down, K_fringe_up, and K_coincident), the equation is in the form:

K_fringe = n1 * (1 – exp(–n2*(D + n3))).

Here, n1, n2, and n3 are non-negative constants calculated by the ***EXACT*** curvefitter. These constants are different for each capacitance effect and layer combination.

The fringe coefficient equation is designed specifically to account "charge-sharing" effects. Consider Figure 1. The value of the fringe capacitor Fu is highly affected by the presence or absence of the Metal1 polygon at the left. If the left Metal1 edge is moved to the right, then some of

Coefficient	HIPEX-C Capacitance Equation	HIPEX-C Statement
K_area, pF/um^2	K_area * <overlapping layer1 and layer2 area>	CUP OVERLAP
K_fringe_ down, pF/um	K_fringe_down * <layer1 perimeter overlapping by layer2>	CUP OVERLAP
K_fringe_up, pF/um	K_fringe_up * <layer2 perimeter overlapping by layer1>	CUP OVERLAP
K_coincident, pF/um	K_coincident * <coincident perimeter of overlapping layer1 and layer2>	CUP OVERLAP
K_lateral, pF/um	K_lateral * <common length of edges within lateral effect on the same layer>	CUP LATERAL

Table 1. Capacitance Coefficients.

the electrical field lines of the capacitor Fu will run from the right Metal1 edge to the left Metal1 edge, rather than to the Metal2 surface above. Therefore, the value of the capacitor Fu decreases. In ***HIPEX-C***, the extracted value of the lateral distance D decreases, and so does the value of the fringe coefficient K_fringe_up.

Figure 2 shows a ***HIPEX-C*** rule file generated by ***EXACT***. Vertical order of layers is METAL2, METAL1, POLY1, SUBSTRATE.

User-Defined Models

In ***HIPEX-C***, you can code your own equations for each of the three parasitic capacitance effects. To do so, you use ***LISA*** (Language for Interfacing Silvaco Applications) procedures in a ***HIPEX-C*** rule file. When using your own capacitance equations, you have the additional option OUTSIDE_LAYERS for the CUP OVERLAP and CUP LATERAL statements. It specifies layers that are above and below primary layer(s). Neighboring layers affect the capacitance values due to the charge-sharing effects between capacitances of different types. ***HIPEX-C*** extracts lateral distances and widths of the specified outside layers such that you can use them in your equations.

In ***EXACT***, you can calculate capacitance coefficients for arbitrary layer configurations. Then, you can write a LISA script that converts the numeric data obtained by the 3D field solver to the user-defined equations in the ***HIPEX-C*** rule file.

```
METAL2, METAL1, POLY1, SUBSTRATE.

cup Overlap
        /layer1 = POLY1
        /layer2 = SUBSTRATE
        /k_area = 3.45313e-05
        /k_fringe_down = 2e-05, 1.23836, 0.0553951;

cup Overlap
        /layer1 = METAL1
        /layer2 = SUBSTRATE
        /inside_layers = POLY1
        /k_area = 1.15104e-05
        /k_fringe_down = 0.00431625, 0.0011,
0.454623;

cup Overlap
        /layer1 = METAL2
        /layer2 = SUBSTRATE
        /inside_layers = POLY1, METAL1
        /k_area = 6.90627e-06
        /k_fringe_down = 0.0045672, 0.0011,
0.22762;

cup Overlap
        /layer1 = METAL1
        /layer2 = POLY1
        /k_area = 3.45313e-05
        /k_coincident = 1.17109e-05
        /k_fringe_down = 2e-05, 1.59705, 5e-05
        /k_fringe_up = 2e-05, 1.70362, 5e-05;

cup Overlap
        /layer1 = METAL2
        /layer2 = METAL1
        /k_area = 3.45313e-05
        /k_coincident = 1.49762e-05
        /k_fringe_down = 2e-05, 1.85038, 5e-05
        /k_fringe_up = 2e-05, 1.62612, 5e-05;

cup Overlap
        /layer1 = METAL2
        /layer2 = POLY1
        /inside_layers = METAL1
        /k_area = 1.15104e-05
        /k_coincident = 3.15129e-06
        /k_fringe_down = 0.00768804, 0.0011,
0.213182
        /k_fringe_up = 2e-05, 0.0011, 5e-05;

cup Lateral
        /layer1 = POLY1
        /k = 0.0011, 0.0354938, 0.00018
        /vicinity = 5;

cup Lateral
        /layer1 = METAL1
        /k = 0.0011, 0.0354938, 0.00018
        /vicinity = 5;

cup Lateral
        /layer1 = METAL2
        /k = 0.0045672, 0.0354938, 0.00018
        /vicinity = 5;
```

Figure 2. Example of ***HIPEX-C*** rule file generated by ***EXACT***.

References

1] "Exact2: Interconnect Parasitic Capacitance Simulator from Silvaco", *Simulation Standard*, Volume 13, Number 2, February 2003.

2] "Parasitic Resistor Extraction with HIPEX-R", *Simulation Standard*, Volume 13, Number 9, September 2003.

3] "HIPEX-NET: New SILVACO Full-Chip LPE Tool vs. Maverick", *Simulation Standard*, Volume 13, Number 9, September 2003.

Expert Layout Editor – New Commands Focus On Easier Operation

Expert layout editor version 4.0.1R has several new commands and functions released together with the new Qt GUI interface. Most of them are developed in order to improve easier operation.

Various LSI layout editors have been released by multiple EDA vendors, but, all of them have almost same or similar functions and commands. If a user benchmarks one of these products, the focus will be the ease-of-use (operability) as one of the most important features in the comparison.

If the user is not satisfied with the basic layout editor purchased, he may customize it by combining some basic features using programming languages to reduce the number of operation steps.

Expert has been developed considering how to improve the operability, and has several new commands and functions including the new GUI.

Property Bar – Property Bar interactively displays attributes of selected objects in the design window. Values of attributes can be changed directly in this Property bar.

Add jog Points / Remove All Jog Points – Edit >> Add Jog Points command allows to draw a cut-line across polygons or wires, and add new vertices to those already-existing shapes. These vertices allow to stretch a part of segment, and make some jogs.

Edit >> Remove All Jog Points command deletes all lengthy (unnecessary) vertices created by Edit >> Add Jog Points.

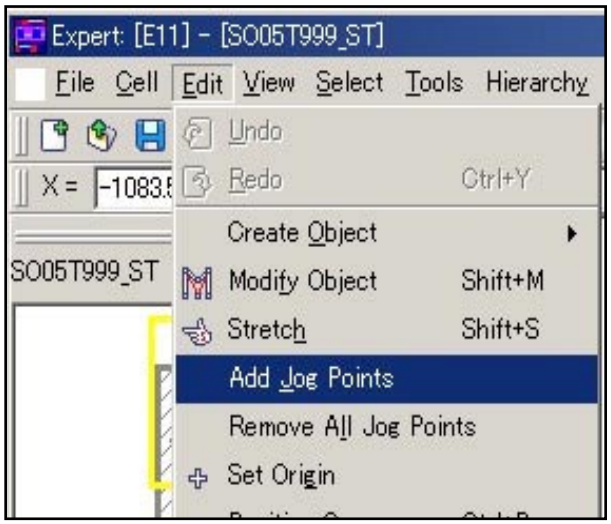


Figure 2. Add Jog Points / Remove All Jog Points

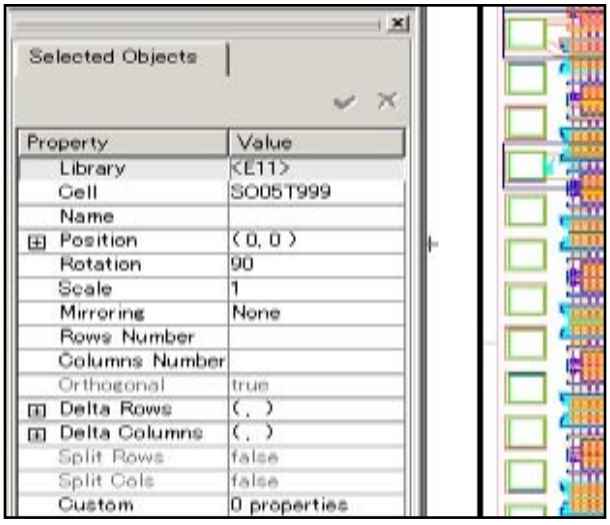


Figure 1. Property Bar

Property Bar

The chart shown in Figure 3 shows a general operation steps needed to change attribute values of already-existing object(s) in ordinary layout editors.

Manual editing is frequently required in various design levels such as chip-level or block level. The iteration of operations mentioned in the above chart decides the length of the total operation process.

Ordinary LSI layout editors have developed impressive functionalities such as visualization, but left out the improvements in operation steps (like the one in the chart below) – the capabilities that users have really wanted.

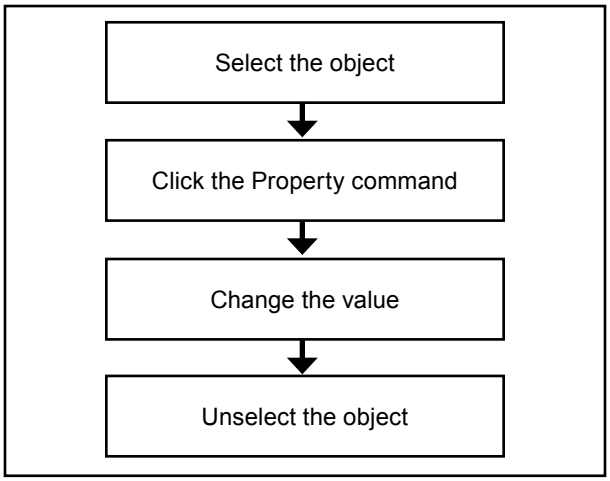


Figure 3. Operation Steps.

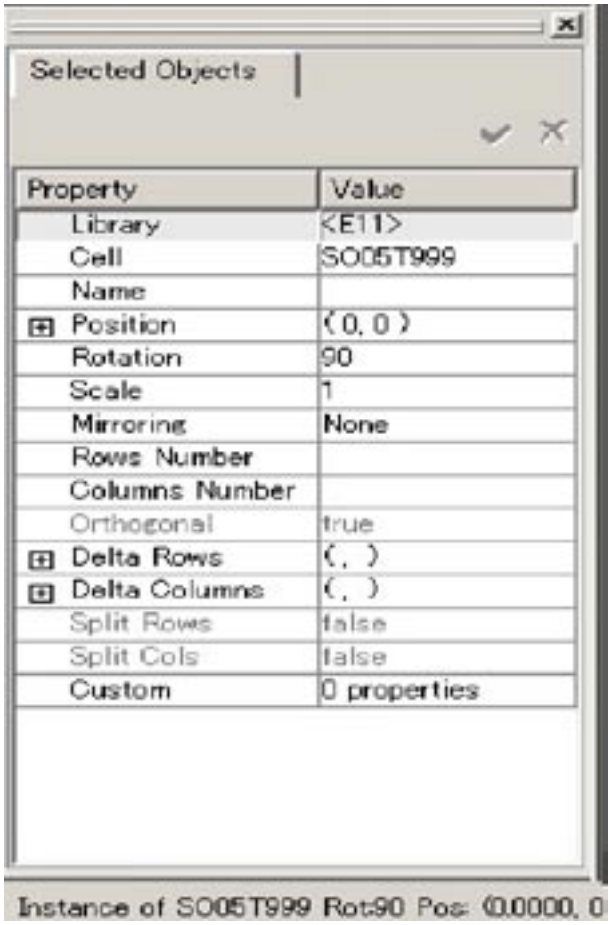


Figure 4. Property Bar.

Property bar solves the problem of reducing the number of operation steps. The total editing time is also reduced by this feature as a major benefit to the user.

The basic operation flow with Property bar is described below.

Figure 4 shows the appearance of the Property bar when a cell instance is selected.

Show / hide this Property bar by clicking the right mouse button at the frame of ***Expert*** design window and selecting Property bar in the popup menu.

When a layout object is selected, it shows all of the attributes. Select any column(s) in the Property bar to modify.

Figure 5 shows the Property bar appearance when the cell name field in the Property bar is selected. When each field is selected, a drop-down list appears to select an item out of several candidates, or a text field appears to modify the value directly.

Apply the modification to the target object by clicking the "Update" button at the top of the Property bar.

The Property bar eliminates one of the ordinary operation steps how to modify an object, and thus improves the productivity

Add Jog Points / Remove All Jog Points

In LSI manual designs, a need to insert new objects in an already-finished layout design is frequent. A typical case is stretching already-existing objects such as wires, polygons or rectangles to make a room.

In the ordinary editing environment a user would need to combine cut, stretch or move commands.

The older versions of ***Expert*** had the feature of Split wire, implemented in Edit >> Stretch as an option, allowing to add new jogs in segments. This feature does not work with polygons or rectangles and only with wires. Ordinary layout editors generally don't have a function to add those jog points to segments of polygons, wires, or rectangles.

Expert has a new feature "Add Jog Points", which solves this problem and improves much of the design productivity in the above situation. It allows to add multiple jog points at one operation on intersecting points of entered cut-line and center lines of already-existing wires, or segments of polygons or rectangles.

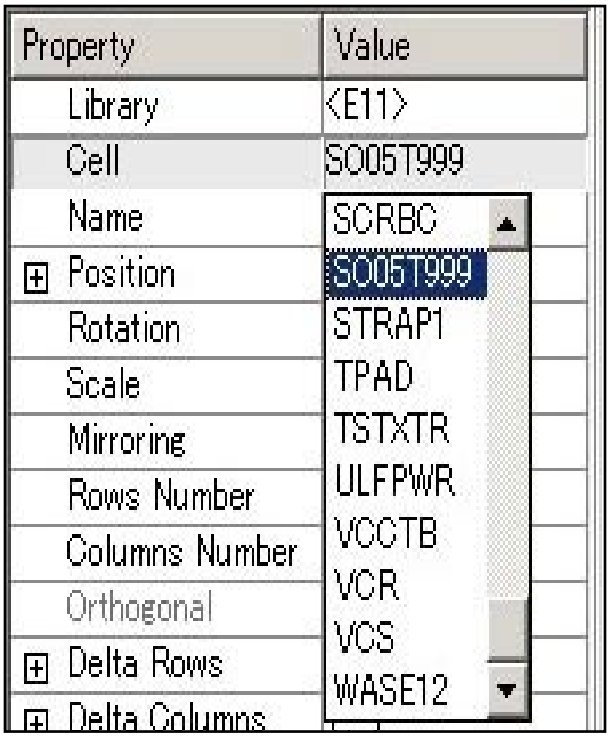
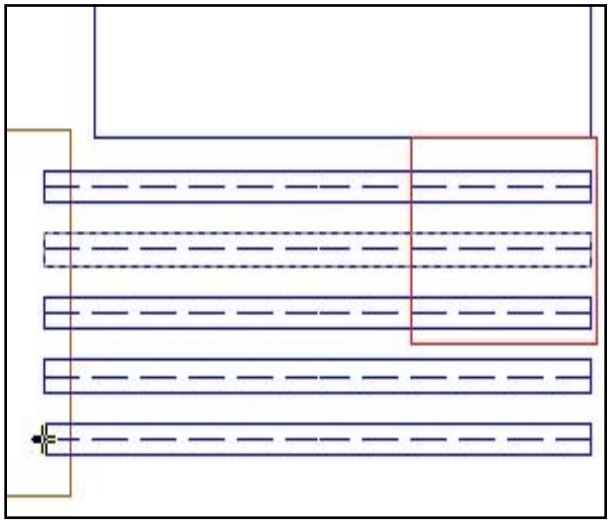
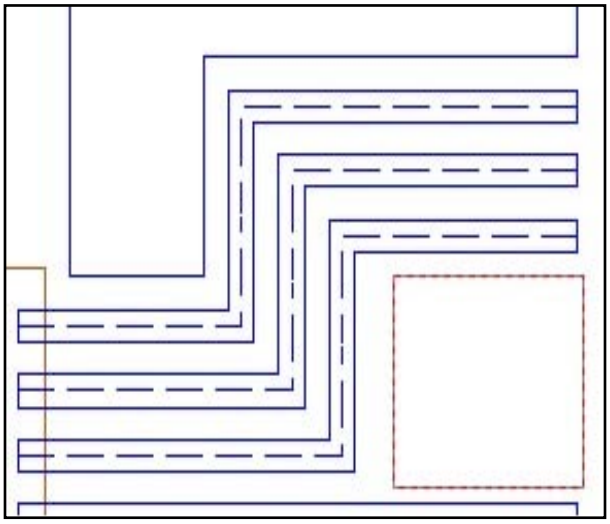


Figure 5. Property Bar.



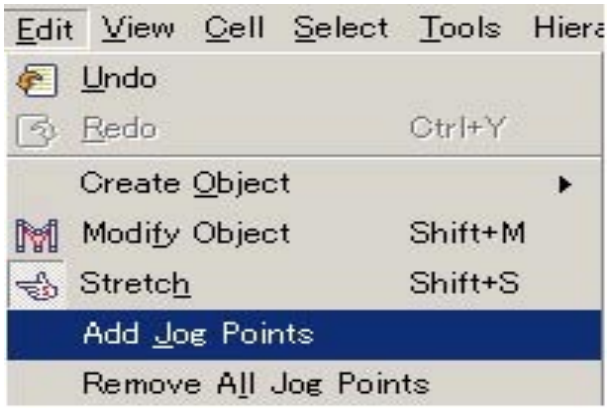
Before stretching.



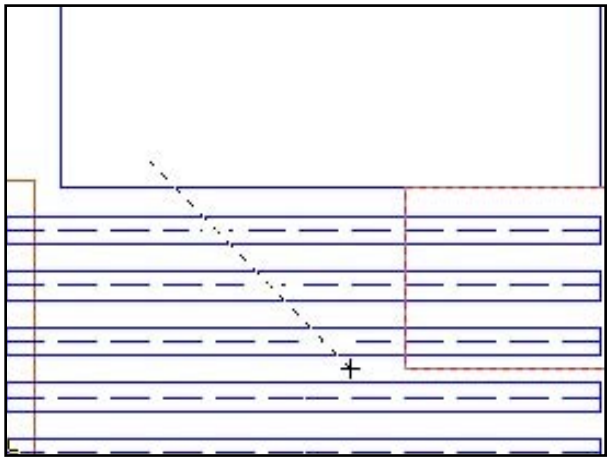
After stretching.

The Figures on this page show how wires can be stretched with this feature.

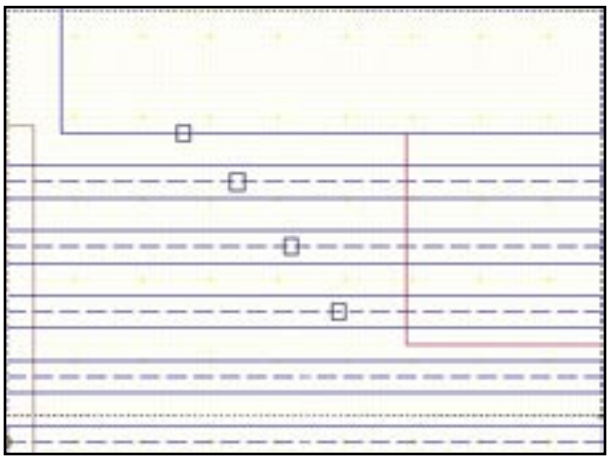
The two figures above (top left and top right) describe an example of the situation when a user wants to move the blue wires overlapping the red rectangular region in order to to make a room.



First, you run Edit >> Add Jog points command from ***Expert*** menu bar.



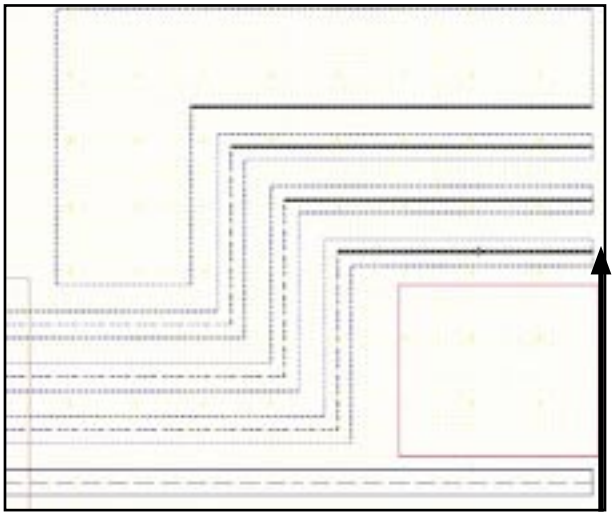
And then, enter a cut line by mouse for jog points overlapping the existing wires.



Clicking the right mouse button to apply the cut line, the command is executed and new jog points are created at the intersecting points of the cut line and wires.

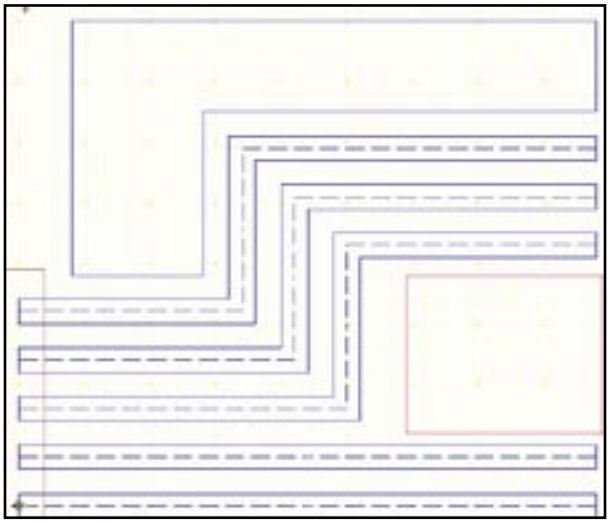
Created jog points are drawn as white dots in the above figure.

Next, run Edit >> Stretch command, and select rightward segments of wires from the created jog points.

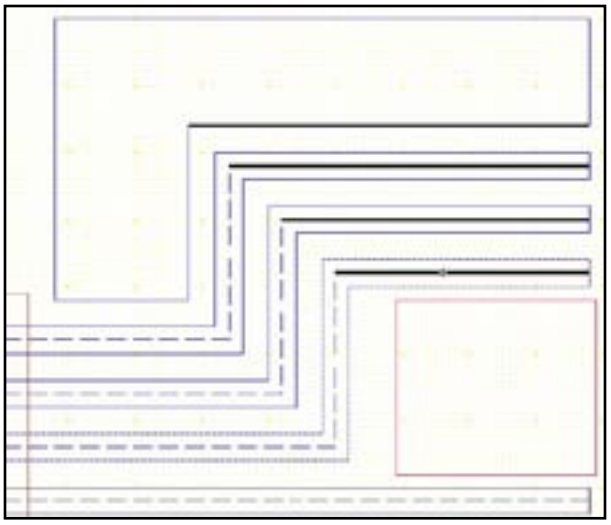


And then, move the selected center lines not to overlap on the red region. Drag those segments by pressing left mouse button.

The black arrow indicates the destination of the stretching.



Completed Design



Release the left mouse button on the destination point to finish the stretching. The target wires has new vertices as below. The same operation can be done for polygons and rectangles.

Finally, type ESC key to quit the Stretch command to finish this operation.

Conclusion

Expert version 4.0.1R has a new Qt based GUI and combined with that a large number of new commands and functions specifically developed to increase operability and user productivity

Calendar of Events

June

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Bulletin Board

Silvaco at DAC

See Silvaco at DAC with live demonstrations of new products:

Harmony-AMS Analog/Mixed-Signal Simulation Platform delivers unsurpassed accuracy and productivity. ***Harmony-AMS*** is based on the ***Silos*** Verilog and ***SmartSpice*** Circuit simulators integrated into a single-kernel simulator that fully supports Verilog-AMS, Verilog, ***Verilog-A***, and SPICE.

SmartSpice-RF Harmonic Balance-Based Simulator provides a complete set of steady-state analyses to design GHz range RF wireless application ICs. ***QUEST*** High Frequency Parasitic Extractor accurately characterizes RF inductors, capacitors, resistors and transmission lines.

HIPEX Full-Chip Parasitic Extraction products perform 3D-accurate and 2D-fast extraction of parasitic capacitors and resistors from hierarchical layouts into transistor-level netlists.

Schematic Driven Layout Design Flows with ***Gateway*** Schematic Editor driving the ***SmartSpice*** Circuit Simulator, ***Expert*** Layout Editor, ***Guardian*** DRC/LVS/LPE, and ***HIPEX*** parasitic extraction tools supported by Silvaco's process design kits.

If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

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Q. Every time I create a new project or library, an empty cell with the same name is created in my project. What do I need to setup to avoid the creation of this empty cell?

A. Under the Setup>>Editor Viewer…>Editing please uncheck the box "Create new projects with default new cell" (see Figure 1). The project/library will then open without creating any default cell, the user will have to choose Cell>New to create its first cell.

An alternative to this extra step is to simply rename the default cell created to the desired name by choosing Cell>>Rename with the default cell active.

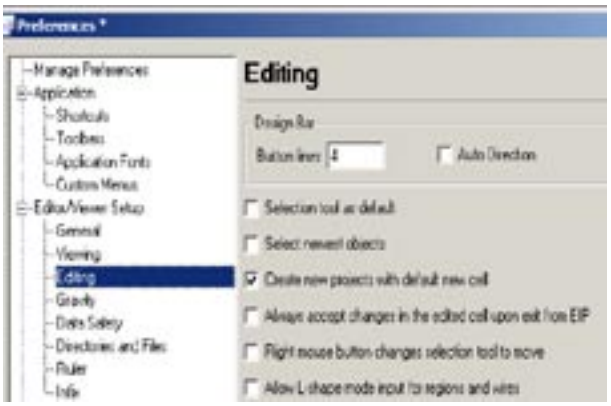

Figure 1. Creation of new projects with default cell option.

Q. When I open my *.eld project I always have to specify the technology file to use. Having a multiple user environment, I want to ensure that the project will never be open with the wrong technology file. How can I guarantee the use of the proper technology file?

A. Your default setup for the option "Use external Technology file for *.eld project" was probably changed inadvertently. Under Setup>>Technology…>General… (see Figure 2) please uncheck the box "Use external Technology file for *.eld project". The default setup for this option is "uncheck". An *.eld project contains all the technology information required. The specification of a technology file when opening an *.eld project is done only in specific cases. In order to guarantee the use of the proper technology file for a given *.eld project, you need to keep this option "uncheck" at all time.

Q. How can I improve the redrawing speed of the layout in *Expert* without changing any hardware on my machine?

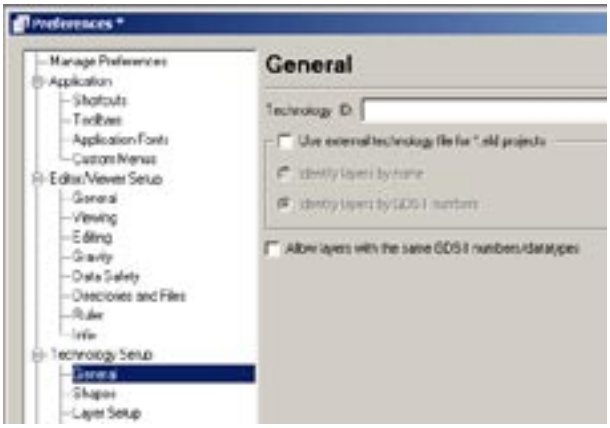

Figure 2. Use external technology file for *.eld project option

A. Many setup options are available in order to improve the redrawing speed.

1) In ***Expert***, under the tab "Setup>>Editor Viewer...>> Viewing" you can change the "Hide objects smaller than X pixels" to a larger number. It is set to 4 by default.

2) In ***Expert***, under the tab "Setup>>Editor Viewer...>> Viewing" you can check the "Data reduction" and trade Accuracy for Speed.

3) In ***Expert***, under the tab "Setup>>Technology>>Layer Wire Setup..." press the button "Stipples…" located in the bottom of the window. This will give you the choice of 3 sources for your stipple; Bitmaps, System and X-Stipples. We recommend using stipples from the System or the X-Stipples list, as the application will achieve maximum redrawing speed with these selections. If the desired stipples is not available in these lists and you elect to create your own through the Bitmaps option, we recommend using an 8X8 size when possible. Using any larger dimension will increase the required time for redrawing.

4) As a general rule only the meaningful layers should be visible, all other layers should be set non-visible (NV).

Remember that the redrawing process can be stop at any time by simply pressing "ESC".

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department
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