Parasitic Capacitance Extraction with HIPEX and EXACT

Overview

To extract parasitic capacitances from a circuit layout, you need to perform the following steps:

1. Define the technology process and material data. This includes vertical order of mask layers and dielectrics, their thicknesses, conductivity, and permittivity constants.
2. Use the technology data as input to a 2D or 3D field solver to obtain capacitance coefficients.
3. Generate a rule file for a full-chip capacitance extractor using the obtained capacitance coefficients.
4. Run the capacitance extractor using the generated rule file.

Silvaco provides tools for performing all the steps above. You can use ***EXACT*** for steps from 1 to 3 and ***HIPEX-C*** for step 4.

EXACT is a 3D field solver powered by a 3D process simulator to accurately represent the cross-sections in the physical chip, rather than using square cross-sections. This maximizes the accuracy of the capacitance coefficients because the calculated capacitance is derived from realistic cross-sections and 3D shapes. See [1] for more information.

HIPEX-C is a full-chip parasitic capacitance extractor. It is a part of the ***HIPEX*** full-chip extractor, which also includes the layout netlist extractor, ***HIPEX-NET***, and the parasitic RC extractor, ***HIPEX-RC***. ***HIPEX-C*** works with a stripe database produced by ***HIPEX-NET***. This database divides the original layout into stripes making parallel processing possible. The stripes also make it easier to process huge layouts on a single host machine, one stripe at a time. ***HIPEX-C*** is a fast 2D extractor. It uses third-party coefficients to derive capacitance from the extracted parameters of parasitic area, length, and distance. See [2–3] for more information.

Built-in Model

HIPEX-C, as well as the most full-chip capacitance extractors, considers the following parasitic capacitance effects:

- Area capacitance is a surface-to-surface capacitance between two overlapping polygons on different layers (see A in Figure 1).
- Fringe capacitance is an edge-to-surface capacitance between two overlapping polygons on different layers (see Fu and Fd in Figure 1). The limit case of a fringe capacitance is a capacitance between exactly coincident edges (see Fc in Figure 1).
- Lateral capacitance is an edge-to-edge capacitance between two adjacent polygons on the same or different layers (see L1 and L2 in Figure 1).

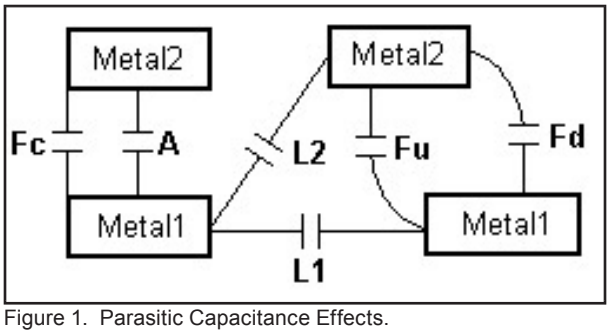

Figure 1. Parasitic Capacitance Effects.

In ***EXACT***, you use a combination of test structures to extract the coefficients for all the parasitic capacitance effects. Each of the test structures is specifically designed to highlight one of the three effects. The coefficients can then be mapped directly to ***HIPEX-C*** (or any other full-chip parasitic tool) extraction statements. ***EXACT*** provides powerful scripting capabilities to convert numeric results generated by the 3D field solver to a rule file for a full-chip extractor. ***EXACT*** comes with a set of ready-to-use scripts that generate rule files for the most popular full-chip extractors, including ***HIPEX-C*** from Silvaco.

Table 1 shows the coefficients, which ***EXACT*** calculates for ***HIPEX-C*** extraction statements (layer1 is above layer2).

All the coefficients, except K_area, are functions of lateral distance D. The area coefficient is a constant. For the lateral coefficient, the following equation is used:

$$K\_lateral = n1 / (D + n2)^{n3}.$$

For all the fringe coefficients (K_fringe_down, K_fringe_up, and K_coincident), the equation is in the form:

$$K\_fringe = n1 * (1 - \exp(-n2*(D + n3))).$$

Here, n1, n2, and n3 are non-negative constants calculated by the ***EXACT*** curvefitter. These constants are different for each capacitance effect and layer combination.

The fringe coefficient equation is designed specifically to account "charge-sharing" effects. Consider Figure 1. The value of the fringe capacitor Fu is highly affected by the presence or absence of the Metal1 polygon at the left. If the left Metal1 edge is moved to the right, then some of

Coefficient	HIPEX-C Capacitance Equation	HIPEX-C Statement
K_area, pF/um^2	K_area * <overlapping layer1 and layer2 area>	CUP OVERLAP
K_fringe_ down, pF/um	K_fringe_down * <layer1 perimeter overlapping by layer2>	CUP OVERLAP
K_fringe_up, pF/um	K_fringe_up * <layer2 perimeter overlapping by layer1>	CUP OVERLAP
K_coincident, pF/um	K_coincident * <coincident perimeter of overlapping layer1 and layer2>	CUP OVERLAP
K_lateral, pF/um	K_lateral * <common length of edges within lateral effect on the same layer>	CUP LATERAL

Table 1. Capacitance Coefficients.

the electrical field lines of the capacitor Fu will run from the right Metal1 edge to the left Metal1 edge, rather than to the Metal2 surface above. Therefore, the value of the capacitor Fu decreases. In ***HIPEX-C***, the extracted value of the lateral distance D decreases, and so does the value of the fringe coefficient K_fringe_up.

Figure 2 shows a ***HIPEX-C*** rule file generated by ***EXACT***. Vertical order of layers is METAL2, METAL1, POLY1, SUBSTRATE.

User-Defined Models

In ***HIPEX-C***, you can code your own equations for each of the three parasitic capacitance effects. To do so, you use ***LISA*** (Language for Interfacing Silvaco Applications) procedures in a ***HIPEX-C*** rule file. When using your own capacitance equations, you have the additional option OUTSIDE_LAYERS for the CUP OVERLAP and CUP LATERAL statements. It specifies layers that are above and below primary layer(s). Neighboring layers affect the capacitance values due to the charge-sharing effects between capacitances of different types. ***HIPEX-C*** extracts lateral distances and widths of the specified outside layers such that you can use them in your equations.

In ***EXACT***, you can calculate capacitance coefficients for arbitrary layer configurations. Then, you can write a LISA script that converts the numeric data obtained by the 3D field solver to the user-defined equations in the ***HIPEX-C*** rule file.

```
METAL2, METAL1, POLY1, SUBSTRATE.

cup Overlap
        /layer1 = POLY1
        /layer2 = SUBSTRATE
        /k_area = 3.45313e-05
        /k_fringe_down = 2e-05, 1.23836, 0.0553951;

cup Overlap
        /layer1 = METAL1
        /layer2 = SUBSTRATE
        /inside_layers = POLY1
        /k_area = 1.15104e-05
        /k_fringe_down = 0.00431625, 0.0011,
0.454623;

cup Overlap
        /layer1 = METAL2
        /layer2 = SUBSTRATE
        /inside_layers = POLY1, METAL1
        /k_area = 6.90627e-06
        /k_fringe_down = 0.0045672, 0.0011,
0.22762;

cup Overlap
        /layer1 = METAL1
        /layer2 = POLY1
        /k_area = 3.45313e-05
        /k_coincident = 1.17109e-05
        /k_fringe_down = 2e-05, 1.59705, 5e-05
        /k_fringe_up = 2e-05, 1.70362, 5e-05;

cup Overlap
        /layer1 = METAL2
        /layer2 = METAL1
        /k_area = 3.45313e-05
        /k_coincident = 1.49762e-05
        /k_fringe_down = 2e-05, 1.85038, 5e-05
        /k_fringe_up = 2e-05, 1.62612, 5e-05;

cup Overlap
        /layer1 = METAL2
        /layer2 = POLY1
        /inside_layers = METAL1
        /k_area = 1.15104e-05
        /k_coincident = 3.15129e-06
        /k_fringe_down = 0.00768804, 0.0011,
0.213182
        /k_fringe_up = 2e-05, 0.0011, 5e-05;

cup Lateral
        /layer1 = POLY1
        /k = 0.0011, 0.0354938, 0.00018
        /vicinity = 5;

cup Lateral
        /layer1 = METAL1
        /k = 0.0011, 0.0354938, 0.00018
        /vicinity = 5;

cup Lateral
        /layer1 = METAL2
        /k = 0.0045672, 0.0354938, 0.00018
        /vicinity = 5;
```

Figure 2. Example of ***HIPEX-C*** rule file generated by ***EXACT***.

References

1] "Exact2: Interconnect Parasitic Capacitance Simulator from Silvaco", *Simulation Standard*, Volume 13, Number 2, February 2003.

2] "Parasitic Resistor Extraction with HIPEX-R", *Simulation Standard*, Volume 13, Number 9, September 2003.

3] "HIPEX-NET: New SILVACO Full-Chip LPE Tool vs. Maverick", *Simulation Standard*, Volume 13, Number 9, September 2003.