Simulation Standard

Connecting TCAD To Tapeout

A Journal for Circuit Simulation and SPICE Modeling Engineers

Silvaco's RFIC Design Suite

Introduction

This article focuses on the use of Silvaco's RFIC Design Suite including PDK, ***SmartSpice-RF***, and Gateway.

Silvaco Process Design Kits (PDKs) have been developed to help start the analog and mixed signal design cycles. The design kit supplies you with all the foundry process specific models, symbols, simulation setup for the Silvaco set of design tools.

SmartSpice-RF Harmonic Balance based Simulator provides a complete set of steady-state analyses and measurements to design GHz range RF wireless application ICs. It accurately and efficiently simulates noise, gain compression, harmonic distortion, oscillator phase noise, and intermodulation products in non-linear circuits using SPICE netlists.

Gateway is the schematic entry for the Analog/Mixed Signal/RF Design design environment. The ***Gateway*** schematic is netlisted for ***SmartSpice-RF*** and tightly integrated for running simulations concurrent with the schematic.

This article shows the basic steps needed to take a design from schematic entry to simulation using the TSMC 018 MM/RF process and a set of Silvaco tools. These steps can be broken down into the following tasks.

- Set up ***Gateway*** with the TSMC 018 MM/RF schematic files to load an example circuit. The example here is the Low Noise Amplifier (LNA) Circuit
- Perform the circuit simulation from the ***Gateway*** Schematic Window. Before you perform a simulation, include the TSMC_cm018 model library from TSMC into the netlist. The LNA circuit is simulated and waveforms are displayed within ***SmartView***

How to Run *SmartSpice-RF* in *Gateway*

To use the environment for schematic, simulation, and post-processing, the following licenses are required:

- ***Gateway***
- ***SmartSpice -RF***
- ***SmartView***

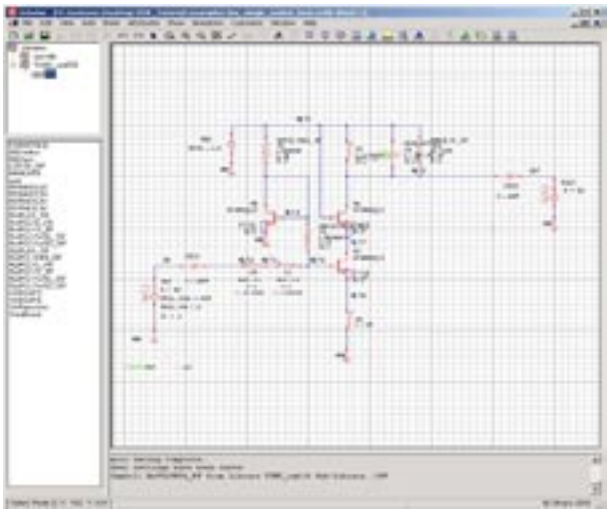

Figure 1. Schematic and Symbol Libraries.

The following example is for an LNA simulation using ***SmartSpice-RF***:

1. To create a schematic in ***Gateway***, first load one or more schematic symbol libraries. The example circuit that we've designed, the LNA Circuit, uses two different symbol libraries: spicelib and TSMC_cm018. The TSMC_cm018 kit symbol library contains process dependent symbols. spicelib (Silvaco's library) contains basic schematic symbols for example, pins, and grounds. (Figure 1)
2. Open the control deck window by selecting Simulation → Input Deck→ Control Deck … in the ***Gateway*** pull-down menu banner to set up simulation environment. (Figure 2)

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INSIDE

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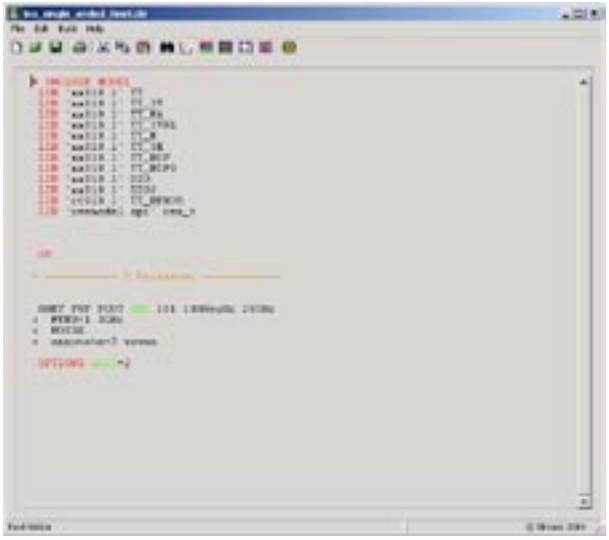

Figure 2. Control Deck.

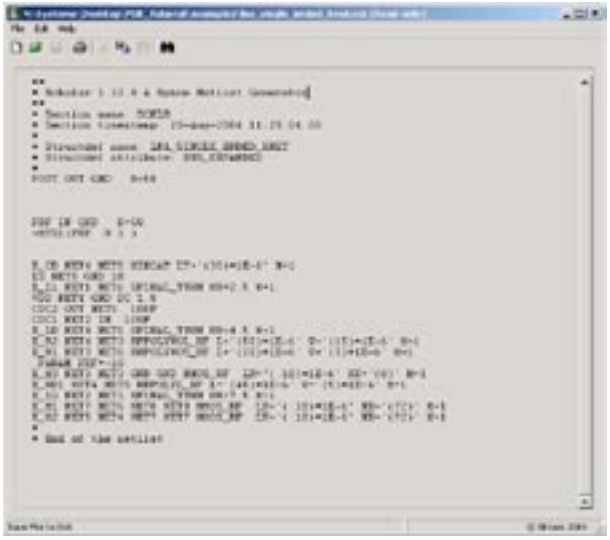

Figure 3. The netlist in ***SmartSpice-RF*** format.

3. Then, generate a ***SmartSpice-RF*** netlist from the Gateway menu banner by selecting Simulation-->Netlist-->SmartSpice. The ***SmartSpice-RF*** netlist will then appear (Figure 3).
4. Simulate the schematic and view the waveform. (Figure 4) (Figure 5) (Figure 6)

Conclusion

By using PDK, ***SmartSpice-RF*** and ***Gateway*** together, some of the specs for LNA like S-Parameter, Noise Figure, P1dB and IP3 can be easily simulated with high accuracy and reasonably run-time. In addition to those simulation capabilities, ***SmartSpice-RF*** can also characterize other RF circuits as well which really provides designers with the means to reduce time to market.

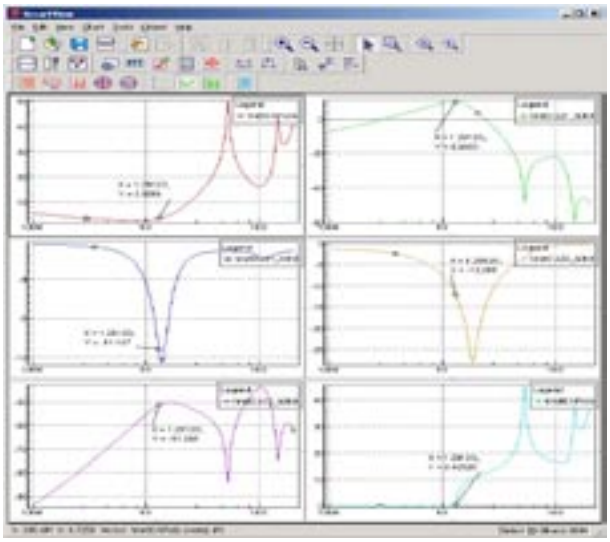

Figure 4. Noise Figure and S-Parameter plots displayed in ***SmartView.***

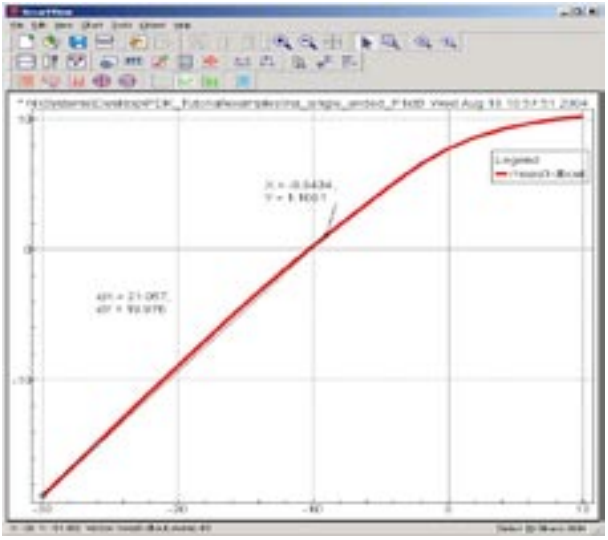

Figure 5. P1dB curve displayed in ***SmartView***.

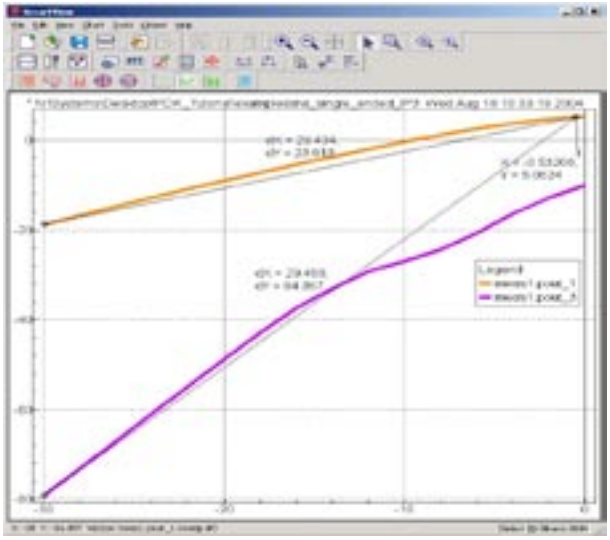

Figure 6. IP3 curves displayed in ***SmartView***.

A Family Portrait of the BSIM Models

1. Introduction

BSIM1, the first model of the BSIM series was released about ten years ago. Some major improvements have been made since that time, making the BSIM3v3 and BSIM4 models become worldwide standards. This article presents the evolutions brought to BSIM models from BSIM3v3 to BSIM5 and BSIMDG, as well as their applications and differences.

2. Models Technologies : Threshold Voltage or Surface Potentials?

The first MOSFET models computations were based on Threshold voltage. It was the case until BSIM4. This technique divides the whole operating region of a MOSFET into pieces, each one described with its own set of equations. To provide a correct transition between these different equations, some smoothing functions are used.

Even when all regions are unified into one equation, smoothing functions are used. These functions are pure mathematics, and are not related to physics.

This is a key point especially at moderate inversion since MOSFET devices keep shrinking ever and ever, supply voltages are down-scaled accordingly. Therefore, devices are now operated in the region near threshold voltage. At this precise point, equations rely on smoothing functions, which are not physical.

The release of BSIM5 brought a totally different approach in the BSIM models. It is based on a new core (Surface Potential Plus), which contains equations for surface potential along the channel, instead of threshold voltage. The major advantage is to get only one equation valid over the whole operating range. Transition issues disappear, as well as empirical parameters needed to fine-tune smoothing functions.

When other models (for example MOS11 or HiSIM) compute surface potentials either iteratively or directly (using an approximation), BSIM5 was designed to simply avoid the question. Instead of computing surface potential at source and drain sides (ϕS, ϕD), it computes charges (Q_S, Q_D). Another improvement is that solving charge equations does not require precision up to microvolts, which are needed by regular surface potential formulations.

The equations for channel currents are following, for both formulations :

Equations for Ids using surface potentials.

$$I_{ds0} = \frac{W \cdot \mu_{eff} \cdot C_{ox}}{L_{eff}} \left[\left(V_{gs0} - V_{th0} \right) \left(\Phi_D - \Phi_S \right) - \frac{1}{2} \left(\Phi_D^{\,2} - \Phi_S^{\,2} \right) - \frac{2}{3} \gamma \left(\Phi_D^{\,3/2} - \Phi_S^{\,3/2} \right) \right]$$

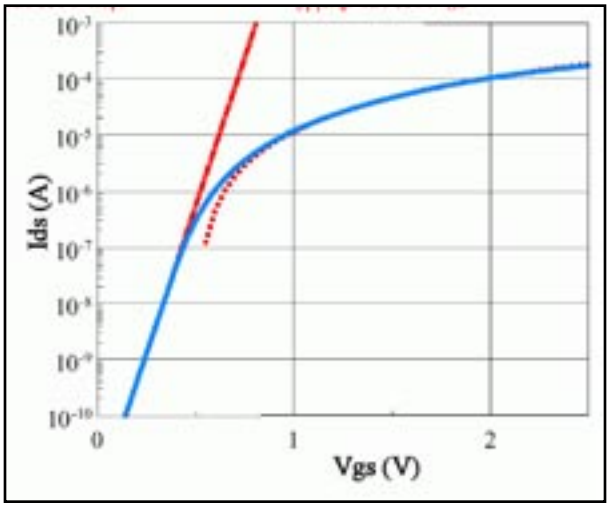

Figure 1. Illustration of smoothing functions between two operating regions

$$I_{ds0} = \frac{W \cdot \mu_{eff} \cdot C_{ox}}{L_{eff}} \left[V_T \cdot \left(\Phi_D - \Phi_S \right) + V_T \cdot \gamma \cdot \left(\Phi_D^{\,3/2} - \Phi_S^{\,3/2} \right) \right]$$

BSIM5 IDS equation

$$I_{ds0} = \frac{W \cdot \mu_{eff}}{L_{eff}} \left[\frac{Q_S^{\,2} - Q_D^{\,2}}{2 \cdot n \cdot C_{ox}} + V_T \left(Q_S - Q_D \right) \right]$$

This new SPP core is now used in recent BSIM models : BSIMDG shares the same core as BSIM5. Presumably, it will be used in next models.

3. Geometry and Temperature Scalability

It is of great importance for a compact model to be valid over different device sizes. The first feature trying to fulfill this requirement is binning. It involves several model cards, each one being valid for a given range of sizes. This is completed by a set of model parameters describing the dependence of core parameters with regard to length (L), width (W) and product ($L \times W$).

Several model parameters are now binnable. The number of binnable parameters is increasing, while in the meantime the model card is kept as small as possible. The temperature dependence was also improved with a number of parameters dedicated to temperature variations. Extracting a whole model card becomes a tough task as the number of parameters increases, but it assures good accuracy with regard to device size and operating temperatures.

4. Models' Complexity and its Influence on Simulation Time

The increasing complexity of models through the years should have logically lead to models more and more time-consuming. This is not totally the case, because in the meantime some major improvements were made to modeling techniques.

For example, the introduction of unified equations to describe all operating regions of a device improved convergence. The removal of smoothing functions helped with difficult convergence cases, since they could contain discontinuities and such mathematical issues. Removing purely mathematical formulations helps to concentrate on physics.

When changing from threshold-voltage to surface potentials (i.e. from BSIM3v3- BSIM4 to BSIM5 and BSIMDG), the main concern is to use an iterative algorithm to solve surface potential equations or not. Since the SPP core is not based on surface potentials but on charges, Berkeley simply did not need to question about this. The equation solved in this core brings the same performances as other models using surface potentials, without the issues raised by iterative solvers or approximations. Questions such as "what to do if the iterative process fails ?" or "is the approximation still valid for this bias ?" are not to be asked.

The simulation of a circuit containing 60 BSIM devices gives the results shown in Figure 2.

These results show that :

- The iteration number for BSIM4 and BSIM5 is lower than the one for BSIM3v3. Convergence is improved in the recents models, with the help of better equations formulation and continuity.
- Simulation time keeps increasing, due to the fact that models are more and more complex and use highly physical equations, whereas old models are assembled with simple equations.

The conclusion of this measure is that a model is a trade-off between the complexity of physics to be solved, and an improved formulation to make convergence easy.

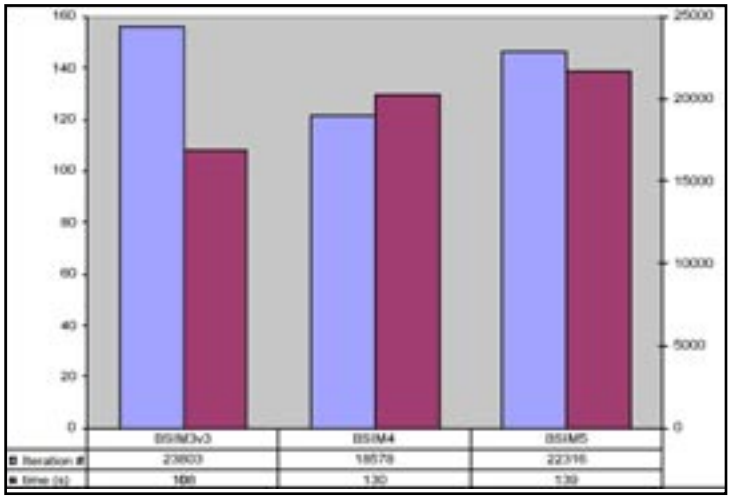

Figure 2. Simulation time and iterations number for a circuit containing 60 BSIM devices.

The experience of Berkeley University certainly played a role to make the latests models powerfull with regard to earlier ones.

5. Specific Applications

5.1 Double-Gate Devices

If BSIM3v3, BSIM4 and BSIM5 have been designed to adress the requirements of general-purpose devices, it is not the case of BSIMDG. Because the scaling limit for bulk CMOS devices is reaching its limit, it is important to search for new structures fulfilling the need for small devices. Double-Gate MOSFET is considered a good candidate, but the physics involved are more difficult to describe because of its very small dimensions.

The double-gate technology has the advantage to suppress short-channel effects (at a given equivalent oxide thickness), and to remain scalable. BSIMDG has been created to provide answers to designers willing to explore this area.

BSIMDG has been developed to be used with various devices geometries, making a compromise to provide both flexibility and accuracy. The different device geometries accounted in BSIMDG model shown in Figures 3, 4 and 5.

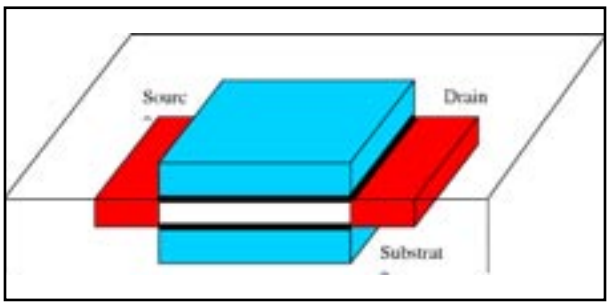

Figure 3. Planar double-gate MOSFET.

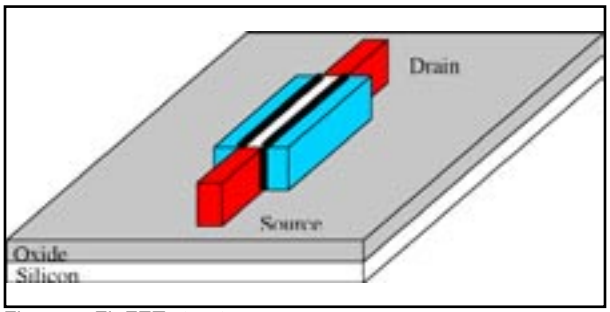

Figure 4. FinFET structure.

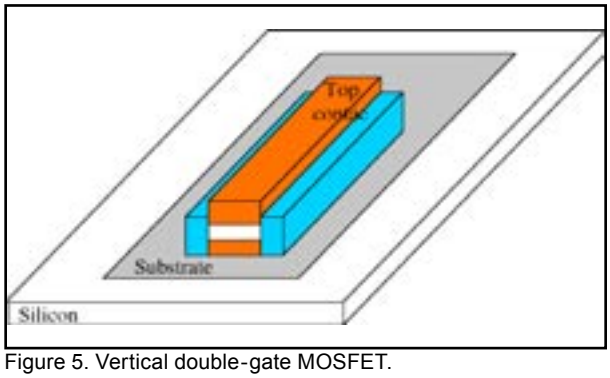

Figure 5. Vertical double-gate MOSFET.

5.2 High frequencies

It is not a surprise to see radio-frequencies modeling as part of today's compact models requirements. BSIM3v3 was the first model of the BSIM-series to provide a Non-Quasi-Static (NQS) mode to account for phenomenons occurring during simulation involving high frequencies. This is important because the need for accurate device description is acute near cut-off frequency, which is critical for designers.

The purpose of this NQS mode is to account for the fact that carriers take a finite time to build up in the channel. Neglecting this time has no or little consequence when frequencies are low, but it becomes important for RF simulations. This special NQS mode is implemented for transient analyses. It extends the capabilities of these models, since it is not a problem anymore to run transient simulation containing high-frequency sources or signals. In the BSIM models, the NQS mode is implemented using a companion-sub circuit, as shown on Figure 6. In this sub circuit, the node Qdef(t) represents the deficit or surplus of channel charge needed to reach equilibrium. The current icheq(t) represents the equilibrium channel charging effect. The value for passive components is determined by relaxation time τ for R, and is fixed for C to get the best simulation accuracy.

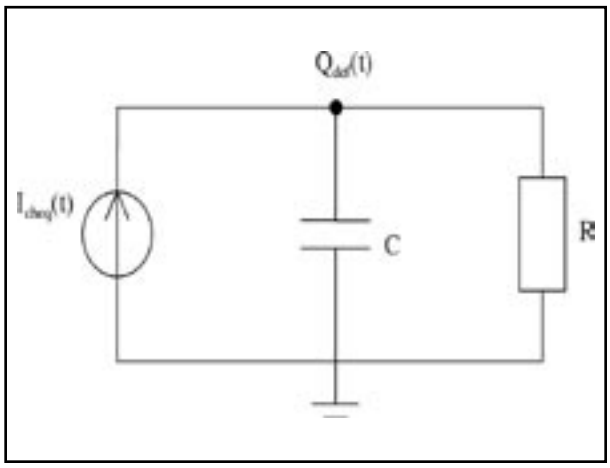

Figure 6. Sub circuit used for NQS mode.

In addition to this simulation mode dedicated to RF, the models contain some elements designed for high frequencies, a network for substrate resistance, a model for intrinsic input resistance (IIR) as well as current models for the gate electrode. These features can be combined or used separately thanks to dedicated selectors. These features were improved in BSIM4, making the BSIM family of models suitable for this kind of simulations, which demands high performance.

6. Status in SmartSpice

The versions available in ***SmartSpice*** are :

BSIM3v3	BSIM3v3.2.4 - 3.2.3 - 3.2.2 - 3.2.1 - 3.2.0 - 3.1.0 - 3.0.0
BSIM4	BSIM4.5.0 β - 4.4.0 - 4.3.0 - 4.2.1 - 4.2.0 - 4.1.0 - 4.0.0
BSIM5	BSIM5.0.0 β
BSIMDG	Implementation in progress (v1.0α)

All implementations benefit from :

- Full compliance with Berkeley original code. All Silvaco improvements can be disabled (specifying SMART=0 restores Berkeley compatibility). Before an error is fixed or an improvement is made, it is first submitted to Berkeley Labs. This way, always the best improvements are made to the model.
- Alternative geometries and extrinsic elements (such as bulk diodes), using dedicated selectors (ACM, DIOLEV, ...)
- ***SmartSpice*** improvements and options (VZERO option, convergence aids, enhanced parameter checking...)

7. Conclusion

Berkeley models have been improved through the years and now provide a full set of models suitable to different technologies and purposes. Older models can deal with well-proven technologies while models such as BSIM5 or BSIMDG allow to explore new devices capabilities. Even if the research is concentrated on innovating models, the old models such as BSIM3v3 still continue to be maintained. This way, the user can choose either very mature and reliable models, or new models for emerging technologies.

HiSIM-1.2 Parameter Extraction with the Revised UTMOST-III Local Optimization Strategies

1. Introduction

HiSIM-1.2 parameter extraction methodology was discussed in detail in a previous issue of Silvaco *Simulation Standard* [1]. This article is meant to provide the precise ***UTMOST-III*** local optimization strategies to *UTMOST-III* users who are interested in HiSIM-1.2 parameter extraction. The developed strategies were applied to the actual 90 nm technology devices [2]. The HiSIM-1.2 proved the capability to give the scalable model down to 100 nm from 10 um channel length with no parameter binning.

HiSIM-1.2 model parameters [3] are capitalized with the bold letters in this article.

2. Required Geometries for the Parameter Optimization

As the HiSIM model is based on the device physics [3], the geometry selection is quite significant to obtain the scalable parameter set. Large device with the long and wide channel is the starting point. Then, the length array(L-array) devices with the varied channel lengths under the fixed width should be prepared, preferably under the wide width, if the width dependent leakage current such as due to a shallow trench isolation (STI) isn't prominent. The channel length spacing should be small enough to represent the channel length effects such as a reverse short channel (RSC) and a short channel (SC) effects. The HiSIM-1.2 RSC and SC parameter extractions are found to require the threshold voltage dependency on the channel length, even though no explicit threshold voltage parameter is used in HiSIM-1.2 [1].

The width array (W-array) devices with the varied channel widths under the fixed length are also necessary. The small devices are used for the model verification, not for the parameter extractions. Neither dedicated parameters for small devices nor the parameter binning are defined in HiSIM-1.2.

3. Required Current Voltage Characteristics

Id/Vg at several drain voltages with the varied body biases should be measured. The drain voltages should cover the low linear, the linear to the saturation transition and the saturation regions. Id/Vd at several body voltages under the operating voltage range are used mainly for the high field mobility tuning. Most of HiSIM-1.2 parameter extractions are done with Id/Vg curves.

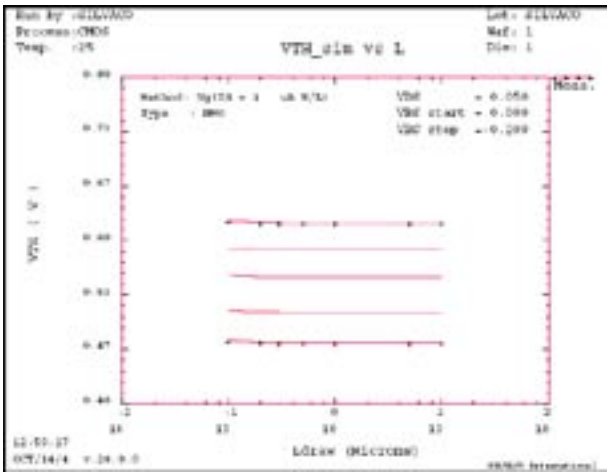

Figure 1. The NSUBP is the same as the NSUBC with 1e-6 of the LP.

The threshold voltage versus the channel length plot should be observed at key steps described detail in below such as # 30: idvg_large_HiSIM, #31: idvg_middle_HiSIM, #32: idvg_short_HiSIM, and #33: idvg_high-VT_HiSIM.

UTMOST-III Validate routine [4] is useful to review the Vth vs. Ldraw Curves.

4. *UTMOST-III* Local Optimization Strategy Description

A. User Initial Input Parameters

The TOX must be defined by the user. Also, the LP value should be put as the initial guess according to the threshold voltage versus the channel length characteristics. There would be two inflection points. The reverse short channel region would be slightly concave with the threshold voltage roll-up, while the transition of the voltage roll-up to the roll-off area would be rather convex.

The LP initial value should be selected inside the concave portion where the slope of the threshold voltage roll-up increases in comparison to the longer channel length devices, or becomes pronounced. And the HiSIM-1.2 users should recognize no structural constraint exists for the LP value [1], even though the name is given as pocket penetration length [3].

The other HiSIM-1.2 parameters should be the default values described in HiSIM-1.2 users manual [3].

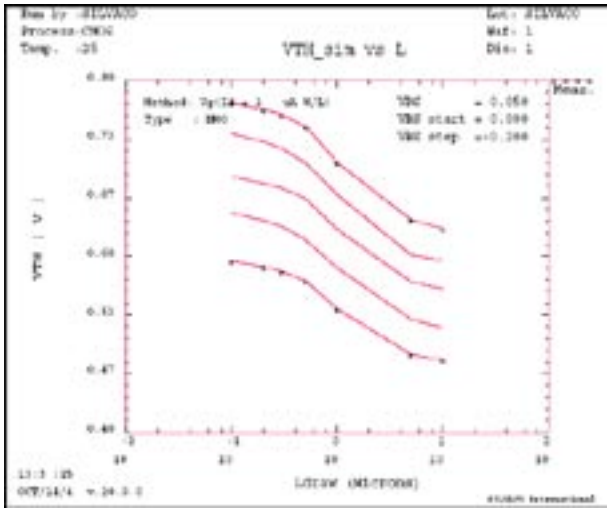

Figure 2. The larger NSUBP value than that of the NSUBC is specified.

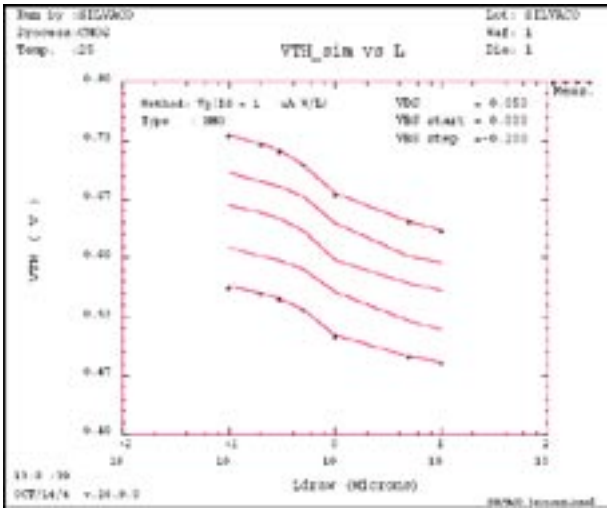

Figure 3. The SCP1 modifies the Vth roll-up phenomenon at the shorter channel length than the LP(1e-6). The SCP1 is arbitrary to highlight the effect.

B. Strategy Definition

 # 30: idvg_large_HiSIM

parameters: NSUBC and VFBC

target: Id/Vg at the low linear region(at the low Vds) with the narrow drain current range around the onset of the strong inversion (threshold voltage region) to avoid STI leakage region

geometry: the large device

NOTE:

The parameter effects are as following.

VFBC: entire Id/Vg curve shift

NSUBC: both entire curve and the body effect shifts

The NSUBP should be linked to the NSUBC as the ratio of one during the optimization in order to set the initial value of the NSUBP. The NSUBC should be optimized several times after the following "#31: idvg_middle_HiSIM strategy" which optimizes the NSUBP, so that the total substrate concentration is modified.

#31: idvg_middle_HiSIM

parameters: NSUBP, SCP1, SCP3, (LP)

target: same as #30 strategy

geometries: NSUBP for the reverse short channel effect (RSCE) devices which have the longer channel length than the LP value. SCP1 and SCP3, the RSCE devices with the shorter length than the LP point

NOTE

The step is quite significant.

The NSUBP is for the Vth roll-up tuning. And the NSUBP value influences the averaged substrate concentration [3] which modifies the large device Id/Vg curve. Optimize the NSUBC and the NSUBP several times to meet the threshold voltage regions for both the large and the middle devices.

The SCP1 is for the convex part of the RSCE on the threshold voltage versus the channel length plot. The transition from the concave to the convex shape occurs around the LP point. The initial value of LP might require the re-optimization to match the transition. Just use the LP only for the purpose.

The SCP3 is related to the Vbs in the equation of the RSCE lateral field gradient equation [3]. However, the SCP3 could have the larger effect than the SCP1 for the entire RSCE, not only for the high Vbs region, which depends on the balance of the SCP1 and the SCP3 values. The high Vbs region for the RSCE devices using the SCP3 could become a bit insufficient fit which might need further investigation.

#32: idvg_short_HiSIM

parameters: PARL2, SC1, SC3

target: same as #30 strategy

geometry: the short channel effect (SCE) devices

NOTE:

The inflection point of the threshold voltage shift from the RSCE to the SCE could become difficult to be expressed with them. In that case, try the different value of the LP. If the Vth vs. Ldraw simulation curves could resemble the data, re-optimize the NSUBP under the new LP. In that case, the NSUBC should also be optimized again.

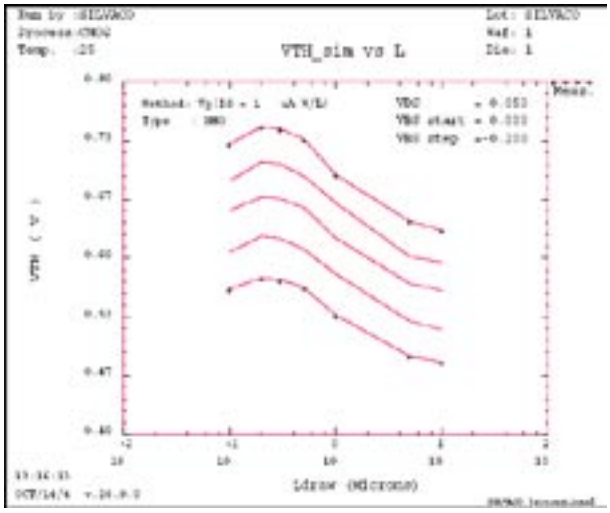

Figure 4. The SC1 expresses the standard short channel effect(Vth roll-off).

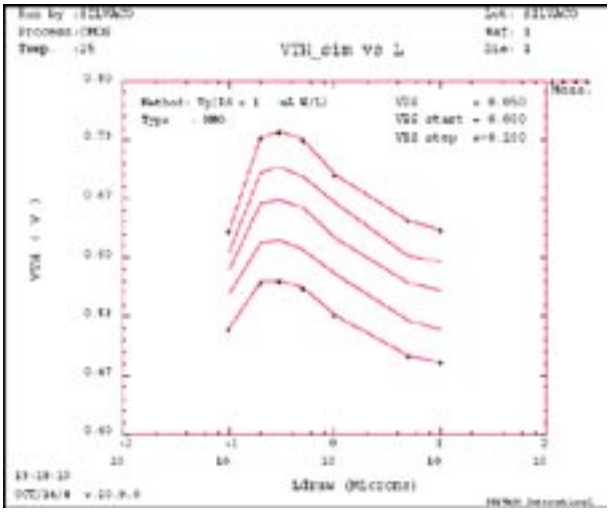

Figure 5. The SC3 modifies the Vth roll-off mainly for the body bias region.

As of the SCP1 and SCP3 relation, the SC1 and the SC3 have the compatible effect on the characteristics.

#33: idvg_highVT_HiSIM

parameters: SC2, SCP2

target: Id/Vg at the saturation region(at the high Vds) The drain current region is the same as #30 strategy.

geometry: the reverse short channel effect devices for SCP2 with the short channel effect devices for SC2

NOTE:

Watch the Vth vs. Ldraw simulations for the high drain bias region.

#34: idvg_lowMue_HiSIM

parameters: MUECB0, MUECB1, MUEPH1, MUESR1

targets: Id/Vg at the low linear region(at the low Vds) MUECB0 for the subthreshold region, avoid the STI leakage part MUECB1 for the on-set of strong inversion MUEPH1 for around the maximum slope of Id/Vg curve MUESR1 for the degradation of Id/Vg at the high Vgs

geometries: large and sometimes large middle devices which show the small threshold voltage roll-up.

NOTE:

Observe the short channel characteristics during the optimization. Even though the large device would be sufficient, the shorter ones might not. Tuning the bias region might be required. Or, the HiSIM substrate parameters, the RSC and the SC parameters might be insufficient. The threshold voltage vs. the channel length should be observed carefully. Because the HiSIM low field mobility model depends on the vertical electric field which are determined by the previously optimized parameters.

With these optimization steps completed, the Id/Vg curves at the low linear region simulated by HiSIM-1.2 should fit well to the measurement data.

Users could use the strategy #34 right after the strategy #30 to get the initial value. Because the HiSIM-1.2 default parameter values are for N channel devices.

#35: idvg_highVD_HiSIM

parameters: VMAX, VOVER, VOVERP

targets: Id/Vg at the saturation region(at the high Vds) with the strong inversion region geometries: the short channel effect devices

NOTE:

HiSIM-1.2 high field mobility adjustment appears to be rather manageable with Id/Vg at the saturation region than using Id/Vd characteristics. However, the Id/Vd curves at the saturation region could be used as the optimization targets. The acceptable optimization fit should be obtained fairly easily. If not, the users should review the previous optimization results through the threshold voltage versus the channel length plot. Because, the high field mobility depends both on the low field component and the lateral electric field. The Vth shift with the channel length is the significant index of the electric field effect.

#36: idvg_narrow_HiSIM

parameters: WFC

targets: Id/Vg at the linear region(at the low Vds) with the threshold voltage region, avoid the STI leakage region

geometries: the narrow channel effect devices

NOTE:
Only one parameter for the threshold voltage roll-off due to the narrow channel effect is prepared in HiSIM-1.2.

#37: idvg_STI_HiSIM

parameters: WVTHSC, NSTI, WSTI

targets: Id/Vg at the linear region, or the saturation region with the current hump area in the subthreshold region geometries: the short channel devices

NOTE:
The hump leakage characteristics due to the STI can be expressed with these parameters. But the users should be careful to varify various devices.

5. Observation of HiSIM-1.2 Parameter Effects

Threshold voltage versus channel length plot has been referred frequently as the index of the electric field effect of HiSIM-1.2 in this article. The following figures will illustrate the HiSIM-1.2 parameter influence on the threshold voltage versus channel length (Ldraw) using ***UTMOST-III*** Validate routine [4].

6. Summary

UTMOST-III local optimization strategies for HiSIM-1.2 model were developed. Although no explicit threshold voltage parameter is used in HiSIM-1.2, the modeling engineer has to specify the target current range around the threshold voltage region for most of the parameter optimization steps, especially for devices with the STI effects.

As HiSIM-1.2 model behavior strictly follows the electric field, and the gradient expression of MOSFET devices, the users should take care of the substrate related parameters.

6. Acknowledgments

The author would like to thank Prof. Mitiko Miura-Mattauch, Hiroshima Univ., Japan, for her valuable suggestion in pointing the significance to track the threshold voltage behaviors during the parameter optimization steps.

Also, he would like to express the gratitude to Semiconductor Technology Academic Research Center (STARC) for allowing to use the device data for HiSIM-1.2 parameter extraction development.

7. References

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Calendar of Events

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Bulletin Board

NSREC

The IEEE Nuclear and Space Radiation Effects Conference (NSREC) is an annual meeting of engineers and scientists presents the latest techniques for enhancing the performance of microelectronic devices and circuits that are used in radiation environments. Silvaco TCAD, ICCAD and circuit simulation tools are used by engineers and scientists to study and model nuclear and space radiation effects on electronic and photonic materials, devices, circuits, sensors, and systems, as well as semiconductor processing technology and techniques for producing radiation-tolerant (hardened) devices and integrated circuits.

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If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

Colin Shaw, Applications and Support Engineer

1. Customers are starting to use 64bit machines with large hard drives and Gigs of RAM and tend to forget the limitations imposed by a 32bit operating system. If you have more than 2Gigs of RAM in a system the extra is not used by the 32bit compiled program as it is not possible to address a contigeous memory space bigger than this when you have 1 parity bit and 31 data bits (2^31). If you are however using our 64bit compiled version of ***SmartSpice*** then you can use as much memory (RAM) as you care to put into the system (2^63 is a huge number compared to the 32 bit case).

2. Some customer have experienced SFLM 6 License problems. The first clue you have a License problem is the "splash screen" of ***SmartSpice*** comes up and eventually disappers without any other window being generated. In this case ***SmartSpice*** has not retrieved a valid License. You will notice on the "splash screen" we write some status messages like "Initilizing" etc. which gives some clue to what is happening in the background. The best way to check your License server is to run a browser window on the License machine using the URL *"http://localhost:3162"*. You can use the IP address or the server name in place of the word "localhost". Since SFLM 6 encompasses both a local License and an EECAD pay by use License it is also usefull to run "sflm_access" to check that your primary server (first one on list is the right one). Sometimes customers have a local Licence but are only pointing at the EECAD server on the web causeing the software not to start.

3. A common problem is to have the wrong syntax in a deck. For example Pspice uses the symbol "$" as part of the node name or sometimes part of a variable name. SmartSpice by default uses the "$" as an in line comment character. This means any text after this point is ignored by the "parser" which is interpreting the deck syntax into a set of mathmatical conditions to be solved. ***SmartSpice*** allows the change of in line comment character by specifying in the deck (.OPTION inlinecc="#") which in this case would set the character used to a "#" and therfore node names are interpreted correctly. The other way is to invoke ***SmartSpice*** from the command line in the right way eg (SmartSpice - pspice).

Sometimes the syntax is less obvious but attention to detail can save a lot of confusion. Unix for example has different types of the quote mark one is straight (') and another is like a backslash (`) and it matters what type is used and that they are paired up if the parser is to interpret the meaning correctly. (You will have the same issue if you ever write scripts in a C shell for example).

```
e.g. [set i = `expr $1 + 1`] in a control loop
```

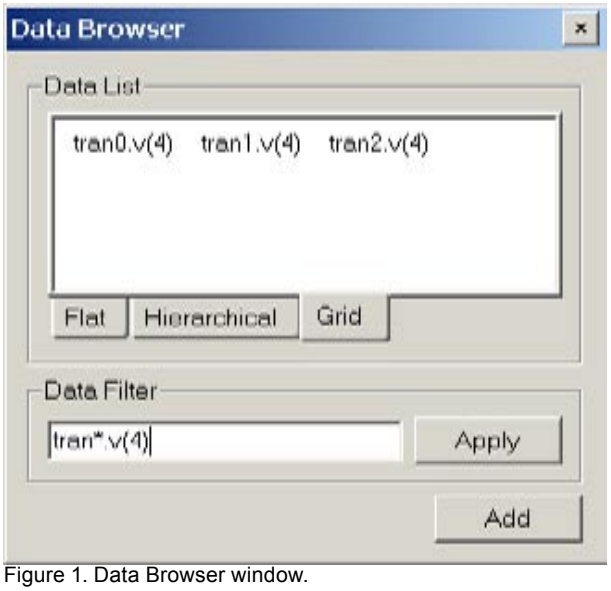

Figure 1. Data Browser window.

4. When you get as far as plotting out a set of vectors in ***SmartView*** people have often wanted to plot the same named vector from a number of analysis runs. This is best done by opening ***SmartView*** and from the menu bar go to "File - Open" and select the RAW data file (data generated by a ***SmartSpice*** simulation run). A "Data Browser" window is opened showing the anlyses runs performed and that can be opened up to reveal the associated individual vectors. A set of associated tabs are along the bottom of this sub-window select the "Grid" tab. You will now see an array of vector names in a winsdow that is sizeable. By use of this window and the filter section below you can display the vectors of interest. Now do an area select and you have the vectors to be plottted by pressing the "Add" button. A simple case is shown in the attached picture but illustrates the power of this feature. Without this you would need to select and open each anlysis and the select the vector and repeat this many times through the contents of the file.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

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