Simulation Standard

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BSIM4 Model Verilog-A Implementation

BSIM4 Model

The Verilog-A hardware description language opens many areas to SPICE users in the field of compact models, allowing manufacturers and universities to study or customize the existing models.

Berkeley BSIM4 model is developed to explicitly address many issues in modeling sub-0.13 microns CMOS technologies and RF high-speed CMOS circuit simulation. Due to its forefront use, BSIM4 was a good candidate for Verilog-A porting.

```
module mosfet(drain, gate, source, bulk);
inout drain, gate, source, bulk;
...
parameter MOBMOD=0;  // Mobility model selector
parameter RDSMOD=0;  // Bias-dependent S/D resistance model selector
parameter IGCMOD=0;  // Gate-to-channel tunneling current model selector
parameter IGBMOD=0;  // Gate-to-substrate tunneling current model selector
parameter CAPMOD=2;  // Capacitance model selector
parameter RGATEMOD=2;// Gate resistance model selector
parameter RBODYMOD=0;// Substrate resistance network model selector
parameter DIOMOD=1;  // Source/drain junction diode IV model selctor
parameter TEMPMOD=0; // Temperature mode selector
parameter GEOMOD=0;  // Geometry-dependent parasitics model selector
parameter RGEOMOD=0; // S/D diffusion resistance and contact model selector
parameter PERMOD=1;  // Source/Drain perimeter model selector
```

Figure 1.

The Silvaco Verilog-A porting is based on the BSIM4 version 3.0 released on May, 9th 2003. The version 2.6.0.R of ***SmartSpice*** Verilog-A interface has been used.

Verilog-A Porting

Silvaco BSIM4 Verilog-A implementation includes all the major physical effects and associated parameters of the original Berkeley version 4.3.0: short/narrow channel effects on threshold voltage, non-uniform doping effects, mobility reduction due to vertical field. All the equations and related parameters have been implemented in a Verilog-A module. The result is a 4,400 lines Verilog-A module.

As in Berkeley code, physical effects model selectors are accessible in the Verilog-A module with the parameters shown in Figure 1.

These model parameters are accessible in the ***SmartSpice*** netlist in the Verilog-A module model card:

```
.MODEL MOSN VLG MODULE = mosfet TYPE = 1 TNOM = 27
+ MOBMOD = 0
+ RDSMOD = 0
+ IGCMOD = 0
+ IGBMOD = 0
...
```

The link with the Verilog-A module is done with `MODULE = mosfet` parameter assignment. The devices are instanciated in the netlist, for example :

```
YVLGm1 node1 node2 0 0 MOSN W=5U L=1.3U
```

The parameters set on this line become instance parameters.

Additional model features like drain/source inversion, N/P MOS type, GMIN convergence improvement and bulk diodes have been implemented. Bulk diodes model can be selected through the model parameter `DIOMOD` shown in Figure 2.

SPICE simulator GMIN option has also been added as a model parameter to improve the convergence properties. The GMIN conductance is taken into account in bulk-drain and bulk-source currents.

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```
case(DIOMOD)
  0:
    begin
      ...
      cbd = isbd * (evbd + xexpbvd - t1 - 1.0) + GMIN * vbd_jct;
    end
  1:
    begin
      ...
      if (t2 < -`EXP_THRESHOLD)
          cbd = isbd * (`MIN_EXP - 1.0) + GMIN * vbd_jct;
      else if (vbd_jct <= vjdmfwd)
          cbd = isbd * (evbd - 1.0) + GMIN * vbd_jct;
      else
          cbd = ivjdmfwd - isbd + t0 * (vbd_jct - vjdmfwd) + GMIN * vbd_jct;
    end
  2:
    ...
endcase
```

Figure 2.

Bulk diode currents contribution is added with <+ operator :

```
I(drainb, drainp) <+ TYPE * cbd;
```

N/P MOS type is accounted for with TYPE model parameter.

Model Convergence

Limitation functionalities have been enabled to help the model to converge with large circuits simulation. maxdelta is a voltage nature attribute which has been added recently in the ***SmartSpice*** Verilog-A interface. This new feature allows to limit the per-iteration voltage change and is disabled by default.

For using voltage limitation, one must set in Verilog-A file:

```
`define  VOLTAGE_MAXDELTA <value>
`include "discipline.h"
```

<value> is the greatest voltage change allowed between 2 consecutive Newton-Raphson iterations. The preprocessor directive `define VOLTAGE_MAXDELTA <value> is a shortcut: it overrides the maxdelta default voltage nature attribute and must be set before including discipline.h file.

BSIM4 ***SmartSpice*** internal model has been successfully replaced by the Verilog-A model in the simulation of a 72-devices two-bit MOSFET adder, as shown in the output display Figure 3.

The results fit the simulation with ***SmartSpice*** internal model level=14. In AC analysis, the model has been validated using an operational amplifier benchmark file supplied by Berkeley University team.

Conclusion

Berkeley BSIM4.3.0 model has been successfully implemented in Verilog-A HDL at SILVACO. The voltage limitation feature recently implemented in Verilog-A interface improves convergence significantly when simulating large circuits, with an acceptable simulation time. The Verilog-A model is freely available on SILVACO website **(http://www.silvaco.com).**

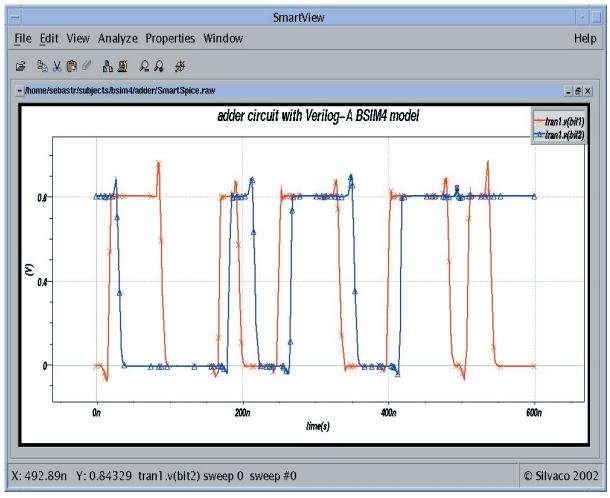

Figure 3. Verilog-A BSIM4.3.0 model based two-bit MOSFET adder.

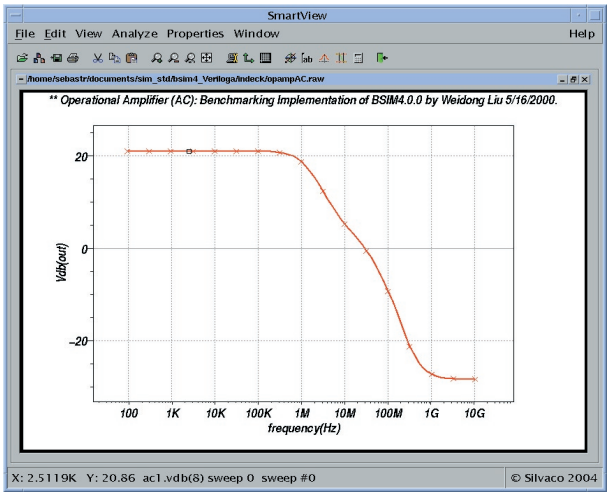

Figure 4. AC analysis of an operational amplifier with BSIM4 Verilog-A model.