

Simulation Standard

Connecting TCAD To Tapeout

A Journal for Process and Device Engineers

Schrödinger Approach and Density Gradient Model for Quantum Effects Modeling

A.Ferroni¹, B.Cottle², G.Curatola³, G.Fiori³, E.Guichard¹

¹ Silvaco Data Systems, 55 rue Blaise Pascal, 38330 Montbonnot Saint-Martin, France

² Silvaco International, 4701 Patrick Henry Dr., Santa Clara, CA 95054, USA

³ University of Pisa, Via Diotisalvi 2, I-56122, Pisa, Italy

Abstract

We describe here two approaches to model the quantum effects that can no more be neglected in actual and future devices. These models are the Schrödinger-Poisson and Density-Gradient methods fully integrated in the device simulator *ATLAS*. Simulations based on such methods are compared to each other on electron concentration and C-V curves in a MOS-capacitor.

1. Introduction

Advanced silicon technology tends towards ever thinner and shorter gate oxide resulting in significant quantum effects. The most relevant effect is the confinement of the carriers. For instance, in a Metal-Oxide-Semiconductor capacitor C-V characteristic, the threshold voltage is shifted and the apparent oxide thickness is increased compared to the C-V characteristic expected with a semi-classical approach. To model this confinement accurately in a device simulator based on a drift-diffusion approach, two methods are treated in this paper. The first one, and the most accurate, is to include the Schrödinger equation into a self-consistent computation with the Poisson equation. Unfortunately this solution, due to its non-locality, has a significant numerical cost and cannot be efficiently coupled with the continuity equations giving the current flow in practical applications. All the same this method is used in 1D as a reference: the C-V characteristic and the carrier density profiles are useful to validate simpler methods. Different simpler methods compatible with the drift-diffusion approach have been developed [1, 2]. In this paper we describe a density gradient model which introduces a quantum potential correction in the continuity equations. In the following, we present first the Schrödinger-Poisson model, then the density gradient model and the comparison to each other.

2. Schrödinger-Poisson Model (S-P)

The confinement effect appears in very thin oxide devices where the barrier of potential at the interface SiO₂/Si is larger and deeper than a thick oxide device. This quantum confinement is well described by solving the single particle Schrödinger equation. Solved self-consistently with the Poisson equation, it provides the eigenvalues and eigenvectors along the three directions of the k-space. Considering m_l, m_{t1} and m_{t2} the electron longitudinal effective mass and the electron transverse effective masses respectively, the electron density is written as:

$$n(x) = \frac{2k_B T}{\pi \hbar^2} \left\{ \sqrt{m_l m_{t1}} \sum_i |\Psi_{li}(x)|^2 \ln \left[1 + \exp \frac{E_F - E_{li}}{k_B T} \right] + \sqrt{m_l m_{t2}} \sum_j |\Psi_{t1j}(x)|^2 \ln \left[1 + \exp \frac{E_F - E_{t1j}}{k_B T} \right] + \sqrt{m_{t1} m_{t2}} \sum_k |\Psi_{t2k}(x)|^2 \ln \left[1 + \exp \frac{E_F - E_{t2k}}{k_B T} \right] \right\}$$

where x is the position along a vertical slice (normal to the gate oxide), Ψ_{li} , E_{li} (resp. Ψ_{tj} , E_{tj}) are the i-th longitudinal (resp. transverse) eigenvector and eigenvalue, k_B is the Boltzmann

Continued on page 2 ...

INSIDE

Mocasim – A Versatile Monte Carlo Simulator for III-Nitride Transport Properties	4
Simulation of Silica Microlenslet Formation by Etch and Reflow Using Elite and Ssuprem4	6
Instructional Approach to Writing Parasitic Capacitance Rules Files Using Exact	8
Calendar of Events	13
Hints, Tips, and Solutions	14

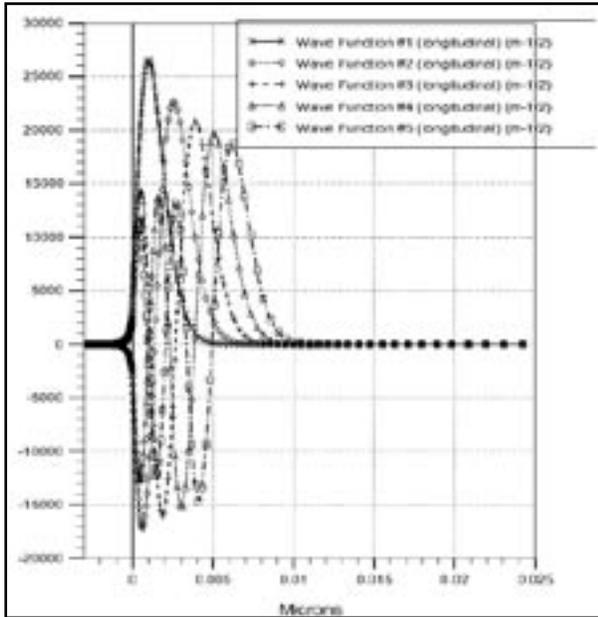


Figure 1a. 5 first longitudinal wave functions.

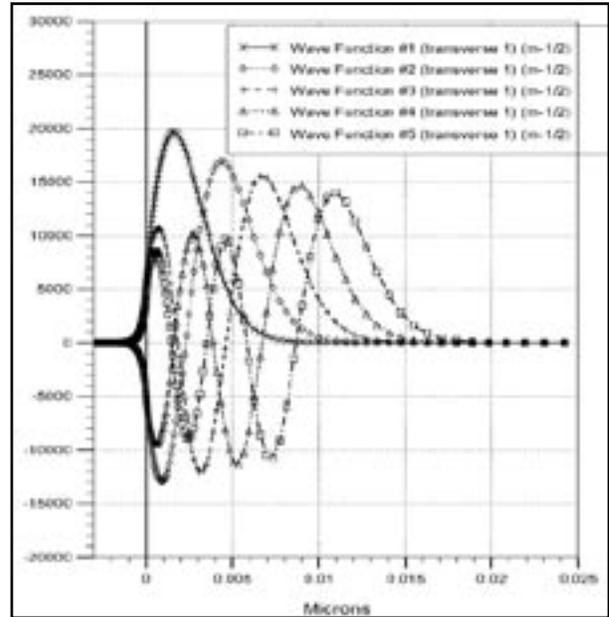


Figure 1b. 5 first transverse wave functions.

constant, T is the temperature, \hbar is the Planck constant and E_F is the Fermi level. For the holes, a similar expression is obtained with the light and heavy holes effective masses. For a 2D device, the S-P equation is solved along a set of 1D parallel slices under the gate. At the ends of each slice an infinite potential is set as a boundary condition. As this assumption is unphysical at the SiO_2/Si interface, the S-P model has been designed to include the gate oxide in the solver so that the eigenvectors and thus the carriers could penetrate in the oxide. In the silicon oxide effective masses for electrons and holes have been defined, with value 0.3 and 1.0, respectively. A full description of this S-P model is presented in [3] with the works presented in [4, 5].

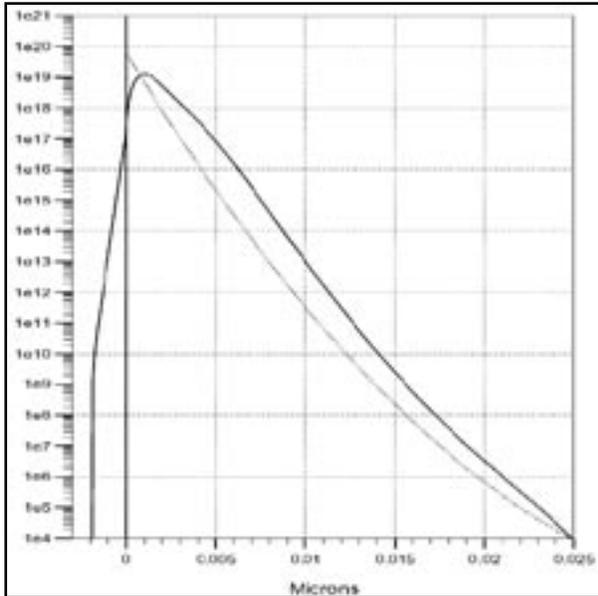


Figure 2. Semi-classical (dotted line) and quantum (solid line) electron concentration in log scale.

To illustrate this model, one defines a MOS-capacitor with $1e18 \text{ cm}^{-3}$ p-type doped substrate and a 3 nm gate oxide thickness. In inversion mode ($V_{\text{gate}}=1.0 \text{ V}$), Figure 1 shows the 5 first longitudinal and transverse eigenvectors ($m_1=0.98$, $m_{t1}=m_{t2}=0.19$ have been set). The corresponding electron concentration is depicted in Figure 2 and compared with a semi-classical profile. It shows the peak in the quantum simulation is no more at the interface ($x=0$ coordinate) as in the semi-classical simulation. The quantum confinement is correctly modeled.

3. Density Gradient Model (DG)

The density gradient method is an approach compatible with the drift-diffusion treatment used in device simulator. Different methods have been proposed [6-8], one presents here one of these models. It applies a quantum potential correction Λ in the density current expression:

$$\vec{J}_n = qD_n \vec{\nabla} n - qn\mu_n \vec{\nabla} (\Psi - \Lambda) - \mu_n \hbar k_n T \vec{\nabla} \ln n_e$$

with:

$$\Lambda = -\frac{\gamma \hbar^2 \nabla^2 \sqrt{n}}{6m \sqrt{n}}$$

where:

$$D_n = \frac{k_B T}{q} \mu_n \quad (\text{if Boltzmann statistics is assumed}),$$

μ_n is the electron mobility,

Ψ is the electrostatic potential,

n_{ie} is the intrinsic carrier concentration,

m is the electron effective mass,

γ is a fit factor.

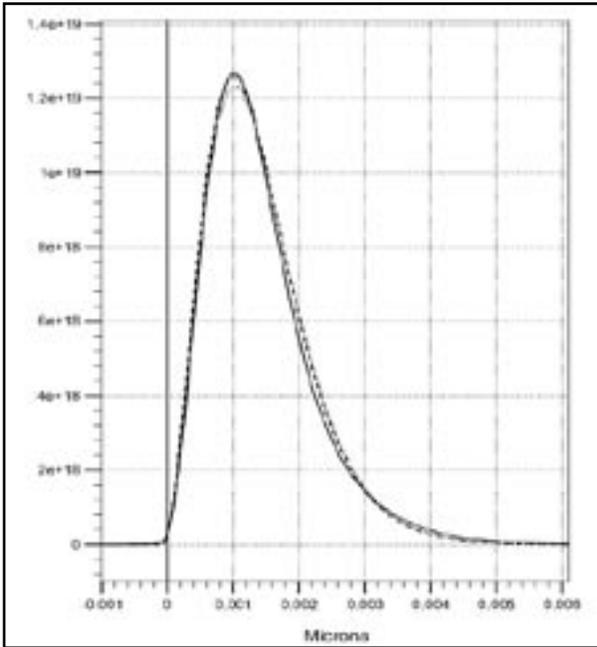


Figure 3. S-P (solid line) and DG (dashed and dotted lines) electron profiles.

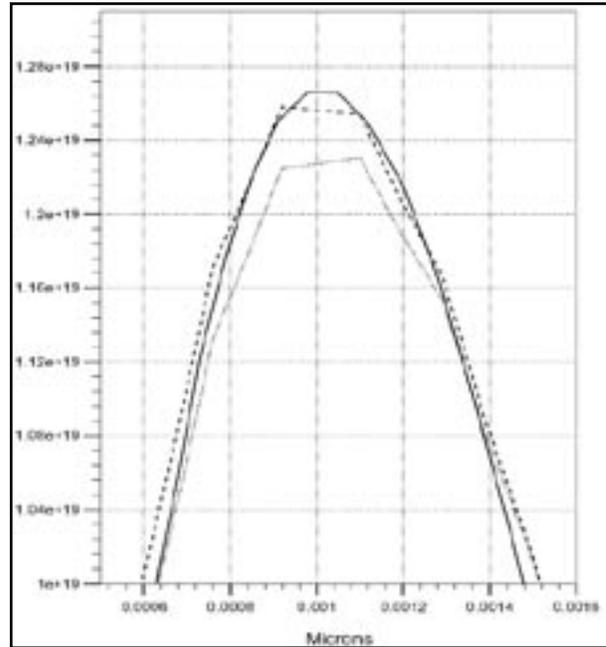


Figure 4. Electron profiles, zoom of Figure 3 around the peak, S-P in solid line, DG/ $\gamma=3.4$ in dashed line and DG/ $\gamma=3.6$ dotted lines.

The factor γ has been introduced to adjust the quantum correction which has been obtained after a few simplifications. Discussions about its introduction can be found in [7-9]. In this way it accounts the fact only one mass is used in DG model whereas three are used in S-P model. It could also be adjusted depending on the temperature of operation and the device (bulk, SOI, double gate).

Concerning the boundary conditions, they are the same as in a semi-classical scheme. The only boundary condition is that at contacts, the quantum correction is zero.

This model is compared to S-P model in Figure 3. The same device as described in section 2 has been used, the γ factor has been set to 3.6 (its default value as indicated in [8]) and 3.4 which fits better the S-P electron profile. The electron concentration is displayed in a linear scale and the $x=0$ coordinate corresponds to the interface. The Figure 4 is a zoom around the peak and it shows a difference between S-P and DG with $\gamma=3.4$ less than 1% at the peak. It confirms the DG model is suitable to capture quantum effects.

Then for each approach, semi-classical, Schrödinger-Poisson and Density-Gradient, we display in Figure 5 the C-V characteristics. The device used is the same as described in section 2 and $\gamma=3.4$ has been set for the DG model.

We clearly note the shift of the threshold voltage near 0.5 volt and the reduction of the quantum capacitance in inversion mode ($V_g > 0.5$ V). The difference observed between S-P approach and DG model in strong accumu-

lation is explained by the fact the charge is treated in a full quantum scheme in S-P solver whereas a part of the charge should be treated semi-classically. However this small error is not really important because the more strongly doped the substrate, the less the carriers are confined [9], moreover the mode of operation of an actual MOSFET is in inversion mode, and Figure 5 shows the very good agreement between the DG model and the S-P approach in this case.

Continued on page 7 ...

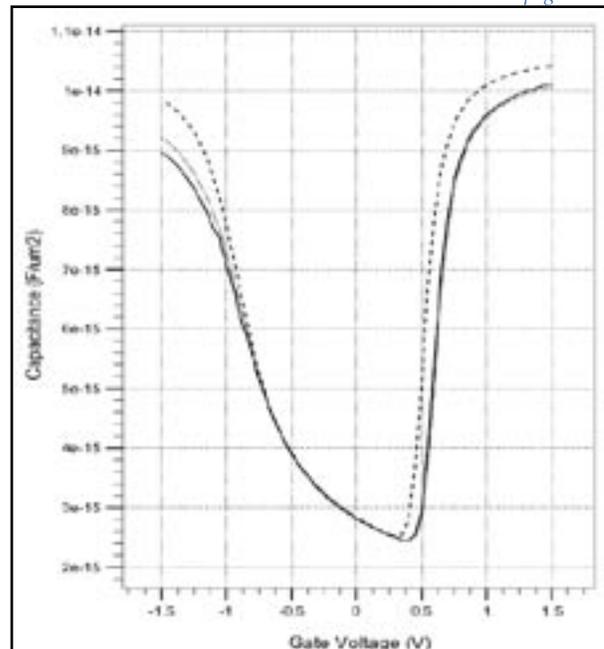


Figure 5. C-V curves, semi-classical in dashed line, S-P in dotted line and DG in solid line.

Mocasim – A Versatile Monte Carlo Simulator for III-Nitride Transport Properties

III-Nitrides have recently attracted attention as a promising material class for high-power, high-frequency microelectronic applications at elevated temperatures. They possess large band gaps, relatively small effective masses in the conduction band minimum, large offsets to the conduction band satellite valleys, and high polar optical phonon frequencies. The large band gaps provide high-breakdown field strengths, while the other basic physical properties result in high low-field mobilities and high saturation velocities.

Monte Carlo Generated Materials Transport Parameters

For this report, we utilized the *Mocasim* Monte Carlo simulator to derive carrier velocity characteristics for common III-Nitride binaries and their ternary alloys ($\text{Al}_x\text{Ga}_{1-x}\text{N}$, $\text{In}_x\text{Ga}_{1-x}\text{N}$, and AlIn_xN in their wurtzite phase). Material model parameters are derived as a function of field, doping, mole fraction, and temperature. The example in Figure 1 shows the electron velocity as a function of electric field strength for $\text{Al}_x\text{Ga}_{1-x}\text{N}$ at room temperature.

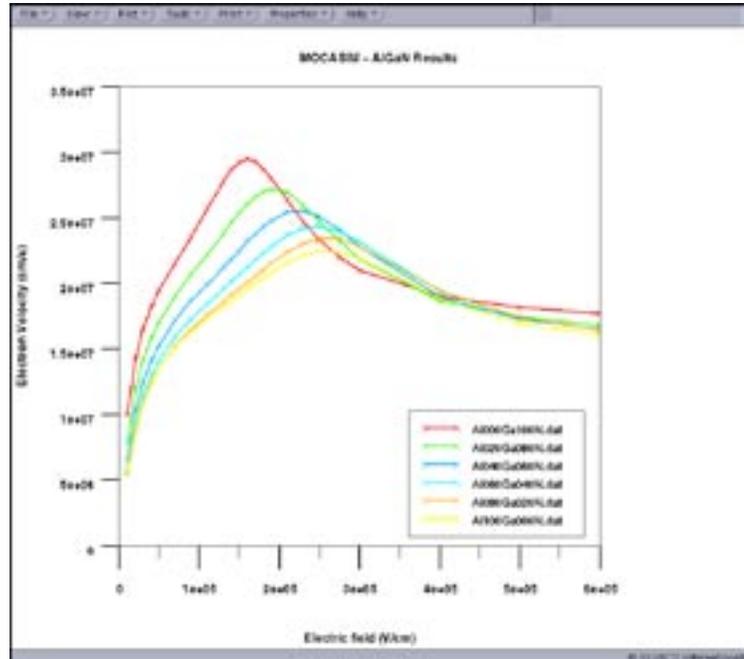


Figure 1. Electron drift velocity in bulk $\text{Al}_x\text{Ga}_{1-x}\text{N}$ as a function of electric field strength at room temperature.

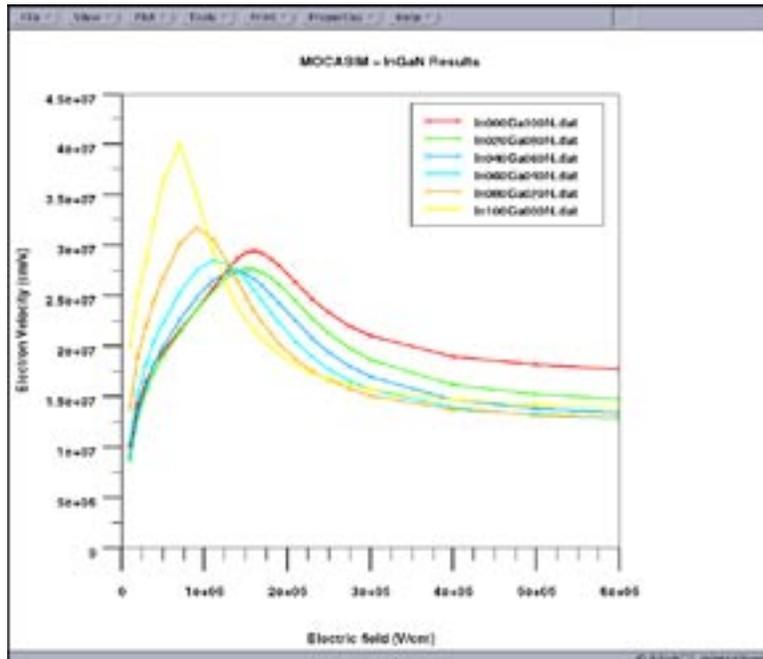


Figure 2. Electron drift velocity in $\text{In}_x\text{Ga}_{1-x}\text{N}$ as a function of electric field strength for various alloy concentrations x at room temperature.

Energy, momentum relaxation times, and other basic transport parameters that form the physical basis for advanced *FastBlaze* energy balance simulations are also calculated from *Mocasim* as a function of carrier energy, doping, mole fraction and temperature. These quantities, calculated directly from band structure data and all relevant scattering mechanisms, provide an accurate representation of velocity overshoot and non-local transport effects within *FastBlaze* energy balance simulations.

Drift Velocities in III-Nitrides

$\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloys are the materials most widely used in the fabrication of III-Nitride FETs. The drift velocities of electrons as a function of electric field strength in this material family are depicted in Figure 1 for various alloy concentrations x . Starting from $\text{Al}_x\text{Ga}_{1-x}\text{N}$ with $x=0$, a decrease in low field drift mobility as well as a decrease in peak-velocity with increasing Al content is observed. Both effects are primarily

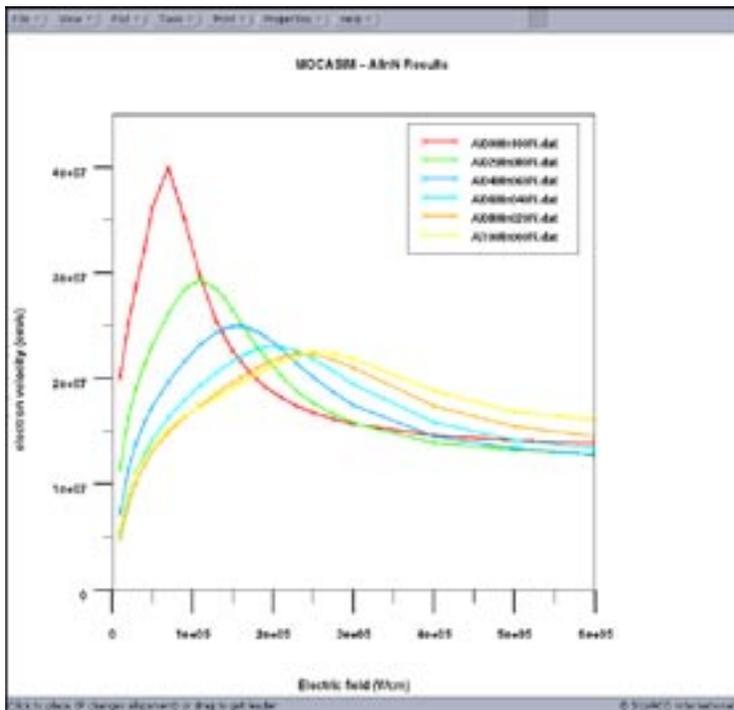


Figure 3. Electron drift velocity in $\text{Al}_x\text{In}_{1-x}\text{N}$ as function of electric field strength for various alloy concentrations x at room temperature.

a direct consequence of the increasing effective mass of the central valley. The saturation drift velocities, on the other hand, remain nearly constant over the entire range from one binary to the other.

InN contains the smallest effective mass of the three binaries (GaN, AlN and InN), so that InGaN channel FETs are considered as a candidate for very high frequency applications. To exploit the potential of the $\text{In}_x\text{Ga}_{1-x}\text{N}$ alloy in terms of mobility and drift velocities, we performed *Mocasim* calculations of this material family. In contrary to the alloys $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and $\text{In}_x\text{Al}_{1-x}\text{N}$, the favorable influence of the decreasing effective mass of the alloy is overcompensated by the increasing influence of $\text{In}_x\text{Ga}_{1-x}\text{N}$ alloy scattering. This results in a decrease of the low field mobility as well as the peak drift velocity by increasing the In content up to about 40%.

A simplified version of a tight binding-based model [1] that is similar to the standard model [2,3] for alloy scattering was implemented for this study. *Mocasim's C-interpreter* Capability was used in order to implement user-defined scattering mechanisms. The saturation velocity is reduced primarily as a result of the lower energetic separation of the satellite valleys from the central conduction band minimum. A slightly higher deformation potential also enhances this effect. Despite the negative transport features of $\text{In}_x\text{Al}_{1-x}\text{N}$, the additional degree of freedom for band profile engineering originates in the high polarization induced fields in lay-

ered structures. $\text{In}_x\text{Ga}_{1-x}\text{N}$ remains a promising alloy for MODFET applications.

$\text{Al}_x\text{In}_{1-x}\text{N}$ displays a similar, but less pronounced behavior for the drift velocities of electrons than is otherwise found in $\text{In}_x\text{Ga}_{1-x}\text{N}$. The low field mobility decreases slightly, with an increase of In content that results from scattering due to alloy fluctuations. This overcompensates for the effect of the decreasing effective mass in the central conduction band minimum. For the same competing mechanisms, peak velocity remains almost constant for In contents up to 20%, while steadily increasing for higher In concentrations. The threshold field to the regime of negative differential mobility, on the other hand, monotonically shifts to smaller field values by increasing the In content of the alloy. This is a consequence of the decreasing effective G-valley mass and the decreasing energetic separation to the satellite valleys. The saturation velocities are reduced for the same reasons as for $\text{In}_x\text{Ga}_{1-x}\text{N}$ with increasing In content, whereby alloy scattering results in a lowering of the saturation drift velocity for intermediate alloy concentrations.

Another key property of nitrides is that they possess large spontaneous, piezoelectric polarization fields that induce high channel densities in HFETs without doping. Such polarization fields are added to *FastBlaze* HFET simulations by including fixed sheet charges that are induced by the abrupt change of pyro- and piezoelectric polarization at the heterointerfaces.

References

- [1] P. A. Fedders and C. W. Myles, Phys. Rev. B 29(2), 802 (1984)
- [2] J. W. Harrison and J. R. Hauser, J. Appl. Phys. 47(1), 292 (1976)
- [3] M. Fahramand et al., IEEE Trans. On Electron Dev. 48(3), 535 (2001).

Simulation of Silica Microlenslet Formation by Etch and Reflow Using *Elite* and *SSuprem4*

I. Introduction

In response to high demand, device designers are developing silica microlenslets that offer efficient coupling between optical fiber bundles and arrays of photodetectors, LEDs, or VCSELs. Microlenslet design involves precise control of the surface curvature in order to place the focus in the optimal region.

ATHENA, Silvaco's physically based process simulation software, helps device designers to simulate the entire fabrication sequence and to determine the effectiveness of the design through ray tracing and device simulation. The software also checks prospective designs and helps calibrate relevant material parameters with lenslet profiles that are easily imported from microscopy or raw calculations.

II. Device Operation

As an example, let's take a single photodetector with a surface-integrated silica microlenslet that forms a compact device with focusing and photon detection capabilities. The microlenslet collects the light signal from the optical fiber and focuses the light into the absorption region of the detector. The signal strength is the strongest at the focal point and so is the photogeneration rate. Consequently, the coupling efficiency and the sensitivity of the device are improved.

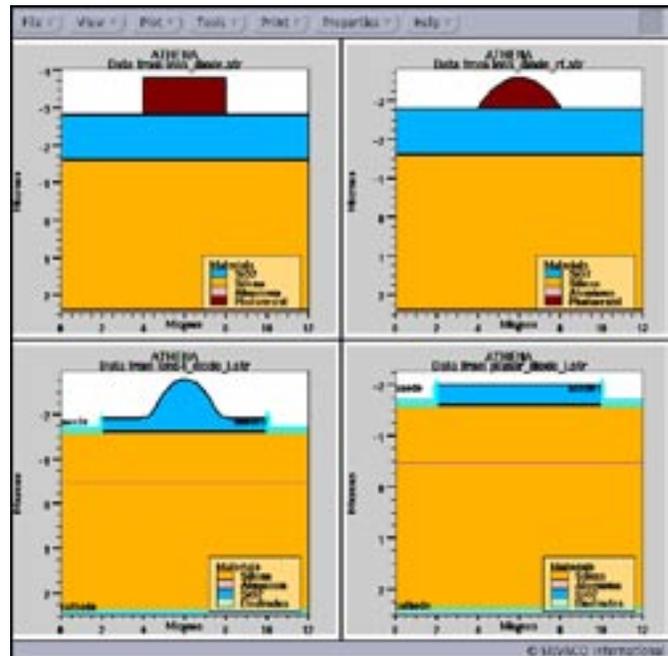


Figure 1. Microlenslet formation with *SSuprem4*.

III. Device Fabrication Processes (*SSuprem4* and *Elite* required)

The simulated formation of this detector-lenslet device begins with the process simulation of the detector, including metal electrodes and a protective glass covering. The formation of the microlenslet in this example involves depositions, reactive ion etching, and a low-temperature reflow that has no effect on the underlying detector.

The starting point for lenslet formation is on top of the photodetector array after the overglass or planarization layer. At this point, a layer of silica that features the desired refractive index and appropriate thickness is laid down. A photoresist layer of the necessary thickness, viscosity, and surface tension properties covers the silica. The outline of the microlenslet is defined by exposing and removing the unwanted portion of the photoresist layer defines (Figure 1).

The next step is to anneal the structure so that the remaining portion of the photoresist is allowed to reflow and form a precisely shaped curved surface (Figure 1). The shape of this surface depends on the viscosity and surface tension of the photoresist layer relative to the silicon oxide layer, the reflow temperature, and the time. All of these parameters can be set with *SSuprem4*, which then more accurately simulates this crucial step.

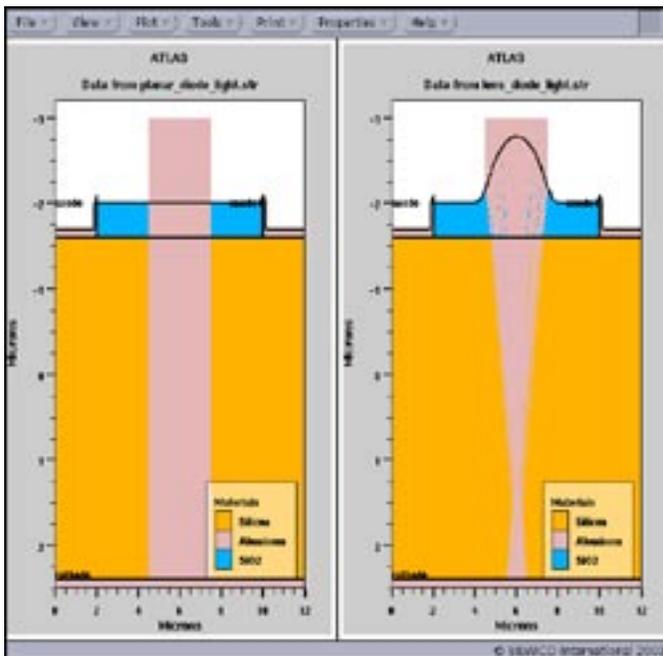


Figure 2. An optical beam with the ray tracing through the structure. The microlenslet is seen to focus the light within the silicon.

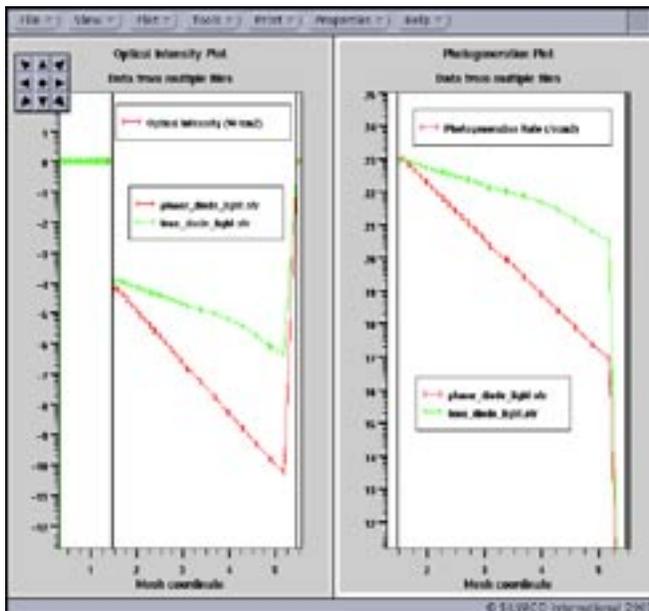


Figure 3. Optical intensity of the beam (left) and photogeneration rate (right) for both the planar device and a microlenslet device.

Following the anneal, reactive ion etching (RIE) will carve a replica of the photoresist into the silica. The precise shape of the silica lenslet depends on the difference between the etch rate in both the photoresist and in the silica. The final microlenslet shape is defined by using the *Elite*-provided RIE model to separately set the etch parameters for the photoresist and silicon oxide.

Elite also simplifies surface profile definition by importing profile data in ASCII text format. These profiles are then used to shape the photoresist and silica layers. A designer calibrates the layers' relevant material parameters by comparing the simulated profiles with those taken

from the microscopy of previous fabrication examples. A designer also auditions specific lenslet shapes with this approach.

A completed device is shown in Figure 1 and is compared with a photodetector without the microlenslet.

IV. Device Simulation and Ray Tracing (*S-Pisces* and *Luminous* required)

A reverse bias is applied to the anode of the photodetector both in the dark and under illumination for comparison. A beam representing the light signal from an optical signal source is shone overhead for the lighted simulation. A comparison of the beam shape and path within a detector with and without a microlenslet integrated onto it is easily obtained with the ray trace feature of *Luminous* (Figure 2). The microlenslet focuses the light onto the depletion region where photon absorption takes place. With a focused light beam, the signal intensity is concentrated to a smaller region (Figure 3), increasing the photogeneration rate within that region. This is verified by plotting the photogeneration rate along the middle line of both devices (Figure 3). The photogeneration rate in the depletion region of a photodetector with a microlenslet is much higher than that of the "planar" photodetector without a lenslet.

V. Conclusion

Silvaco's physically based process simulator *ATHENA*, and its associated module *Elite*, help to simplify of complicated and arbitrary surface profiles and lens curvature implementation. *ATHENA* and *Elite's* versatile features ease the workload of device designers and helps to exercise precise control of microlenslet device geometry.

... continued from page 3

4. Conclusion

We have presented the different approaches to model quantum confinement in MOSFET implemented in the commercial device simulator *ATLAS*. The Schrödinger-Poisson model is suitable for any kind of 1D or 2D devices (with planar or non-planar gate oxide) in which quantum effects are important and with bias conditions not too far from equilibrium (for instance, a small bias on the drain can be applied). This solver has been developed in collaboration with the University of Pisa, and has shown excellent agreement with their in-house code. Then a density gradient model has been described and its results, based on carriers' profiles and C-V curves, have proven its capability to model correctly the quantum confinement with an adjustment of the γ factor.

References

- [1] W.Hänsch et al., "Carrier transport near the Si/SiO₂ interface of a MOSFET", *Solid-State Electron.*, vol.32, p.839, 1989.
- [2] M.J van Dort et al., "A simple model for quantization effects in heavily-doped silicon MOSFET's at inversion conditions", *Solid-State Electron.*, vol.37, p.411, 1994.
- [3] *Simulation Standard*, Volume 12, Number 11, November 2002 on <http://www.silvaco.com>
- [4] S.Gennai, G.Iannaccone, "Detailed calculation of the vertical electric field in thin oxide MOSFETs", *Electronics Letters*, 35, p.1881, 1999.
- [5] G.Iannaccone, F.Crupi, B.Neri, S.Lombardo, "Suppressed shot noise in trap-assisted-tunneling of metal-oxide-capacitors", *Appl. Phys. Lett.* 77, pp.2876-2878, 2000.
- [6] M.G.Ancona, H.F.Tiersten, "Macroscopic physics of the silicon inversion layer", *Physical Review B*, vol.35, 15, pp.7959-7965, 1987.
- [7] M.G.Ancona, "Density-gradient theory analysis of electron distributions in heterostructures", *Superlattices and Microstructures*, vol.7, No.2, 1990.
- [8] Andreas Wettstein et al., "Quantum Device-Simulation with the Density-Gradient Model on Unstructured Grids", *IEEE Transactions On Electron Devices*, vol. 48, No.2, February 2001.
- [9] G.Chindalore et al., "An experimental study of the effect of quantization on the effective electrical oxide thickness in MOS electron and hole accumulation layers in heavily doped Si", *IEEE Transactions On Electron Devices*, vol. 47, No.3, March 2000.

Instructional Approach to Writing Parasitic Capacitance Rules Files Using Exact

1. Introduction

The *Exact* analysis stage extracts the user-required information necessary for the respective parasitic capacitances by probing the Exact database. This is performed via script files written in *LISA* (Language for Interfacing Silvaco Applications). This article demonstrates a systematic approach for writing analysis script files.

2. Full Working *LISA* script file

Firstly a full workable analysis script file is detailed; explanatory discussion then follows.

```
! *****BEGIN LISA SCRIPT*****
!Performs numerical fit to determine near body
effect on fringe down capacitance data. Text
!following an exclamation mark is a comment.
Layouts referred to in the script are Parallel
!Plate.pml (termed PP...) and OneArray.pml
(termed OA...).

!Load in the internal database
db = DatabaseLoad(".");

!Create capacitance variables and assign capaci-
tance values to them
extract_name("PP_Ctotal", "B_gnd", "Plate");
extract_name("OA_Ctotal", "B_gnd", "Llp");

!Decide which combinations are to be examined
and included in the tables.
PP_combinations = {1};
OA_combinations = {1};

!create table for parallel plate information
table_PP= select(db, "ParallelPlate", PP_combina-
tions, {"ParallelPlatePlateWidth"},
{"PP_Ctotal"});

!change units of capacitance to fF
column_scalar_op(table_PP, "PP_Ctotal", table_PP,
"PP_Ctotal", "*", 1e15);

!save the table for reference purposes
save_table(table_PP, CSV, "PPa.csv");

!create table for fringe down capacitance in-
formation.
table_OA= select(db, "OneArray", OA_combinations,
{"OneArrayPlateWidth",
"OneArrayLayer1Space", "OneArrayLayer1Width"},
{"OA_Ctotal"});

!change capacitance units to fF
column_scalar_op(table_OA, "OA_Ctotal", table_OA,
"OA_Ctotal", "*", 1e15);

!save output table for reference purposes
save_table(table_OA, CSV, "OAa.csv");

!Perform operations on table_OA to obtain fringe
down capacitance.

merge(table_PP, "PP_Ctotal", table_OA);
```

```
save_table(table_OA, CSV, "OAb.csv");

column_vector_op(table_OA, "PP_Ctotal", table_OA,
"OneArrayLayer1Width", table_OA, "OA_Carea", "*");
column_vector_op(table_OA, "OA_Ctotal", table_OA,
"OA_Carea", table_OA, "OAFD_alpha", "-");
column_scalar_op(table_OA, "OAFD_alpha", table_OA,
"OAFD", "/", 2.0);

save_table(table_OA, CSV, "OAc.csv");
save_table(table_OA, TONYPLOT, "OAc.str");

!Equations for fringe down with near body ef-
fect.

equationFD="OAFD=1.0*K1[0.01]*(1.0-exp(- K2[0.09]*
({OneArrayLayer1Space}+K3[0.03])))";

res_OA = (calculate_fit(equationFD)(table_
OA)(sum_combinations(OA_combinations))("FD_
OA.rsm")("Downhill-Simplex"));

save_table(res_OA, CSV, "OAFDcoeff.csv");

! Header notes
write_parameters("eg1.xcl", table_PP, {"\n// Ex-
ample script for Exact2 manual\n"});
write_parameters("eg1.xcl", table_PP, {"\n\n"});
write_parameters("eg1.xcl", table_PP, {"UNIT
LENGTH um\nUNIT CAPACITANCE fF\n\n"});

!Write text for area capacitance expression and
fringe down capacitance expression

write_parameters("eg1.xcl", table_PP, {"CAPACI-
TANCE CROSSOVER PLATE ", "LAYER0", " ", "LAYER1",
"\n\n[\n\n C =", "PP_Ctotal", "*area()\n\n]\n\n"});
write_parameters("eg1.xcl", res_OA, {"CAPACITANCE
CROSSOVER FRINGE ", "LAYER0", " ", "LAYER1", "\
n\n[\n\n C =length()*", "k1", "(1.0-exp(-", "k2",
"(distance()+", "k3", "))\n\n]\n\n"});

!*****END SCRIPT FILE*****
```

Main output from the script file: capacitance rule file eg1.xcl

```
UNIT LENGTH um
UNIT CAPACITANCE fF

CAPACITANCE CROSSOVER PLATE metal1 metal2

[
  C =0.0345313*area()
]

CAPACITANCE CROSSOVER FRINGE metal1 metal2

[
  C =length()*0.0454768*(1.0-exp(-0.444801*(dis-
tance()+0.0874414)))
]
```

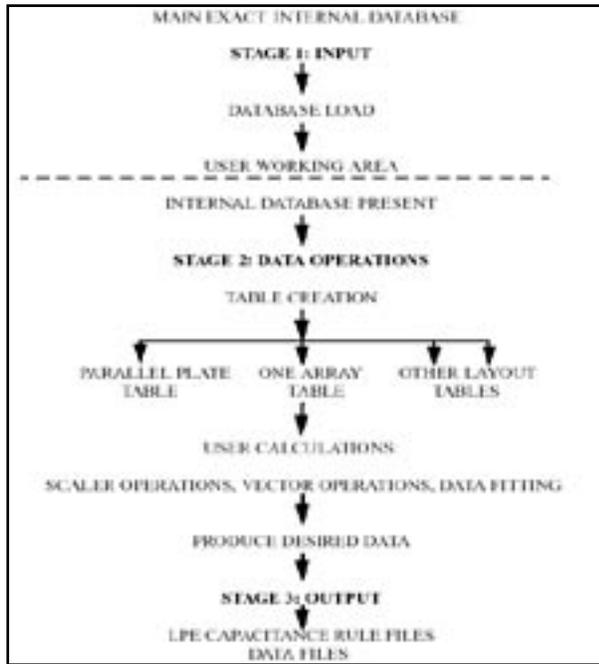


Figure 1. Schematic diagram of the stages within an analysis script

3. Script Discussion

There are three dominant stages in a full workable *Exact* script file, (see Figure 1):

- Stage 1: input. This creates a table containing all the required data.
- Stage 2: data operations. Manipulate the table in order to produce specific capacitance information.
- Stage 3: output: This creates capacitance rule files for use in layout parasitic extraction (LPE) tools.

3.1 Stage 1: Input commands.

```
db = DatabaseLoad("/home/.../....etc");
or
```

```
db = DatabaseLoad(".");
```

The input stage's main aim is to build a data table or several data tables. Firstly, it is necessary to load in the database where the output from *Exact* has been saved. DatabaseLoad performs this task via the user specifying to it the path of the database and the name to use for a variable to store it in. This path must match that in the output stage of the *Exact* experiment, see Figure 2. Once the internal database has been loaded into the analysis stage, the next task of the input stage is to create a table. The *LISA* command used to create a table is:

```
table_OA= select(db, "OneArray",
OA_combinations, {"OneArrayPlate-
Width", "OneArrayLayer1Space",
"OneArrayLayer1Width"}, {"OA_Ctotal"});
```

The syntax must follow:

- 1) Name of table to create.
- 2) Keyword select (arguments inside the parentheses must follow)
 - a) Database name
 - b) Layout name
 - c) Specific layout combinations

This is a sequence of integers. The analysis stage is informed what layout-specific combinations to include in the table. We use OneArray_combinations = {1} is used since only combination 1 is present. While a string of numbers for the layout combinations argument would suffice, the use of a variable is more intuitive, especially to another user reading the script.

- d) Structure information argument

This is a set of comma separated strings which must be contained within braces. The strings form a list of specific structure parameter values that the user requires to be stored in the table.

- e) Capacitance list argument

This is a set of comma-separated strings contained within braces. The strings form a list of user-required capacitance values to store in the table after extraction from the database. The key word extract_name is used for this purpose:

```
extract_name("OA_Ctotal", "B_gnd", "L1p");
```

The parameters inside the parentheses (from left to right) are the user-specified capacitance name (target capacitance) to include in the table, the wire 1 name, and the wire 2 name. While the target capacitance name is chosen arbitrarily, the names of the wires must correspond to those of the respective layout.

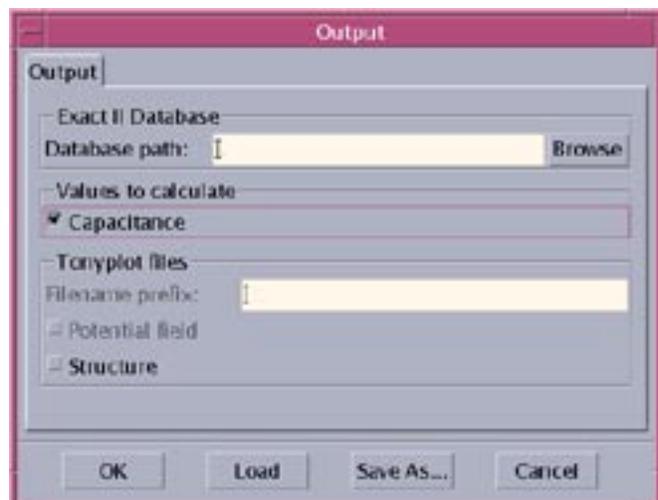


Figure 2. Output GUI from main *Exact* experiment.

3.2 Stage 2: Data Operations

The goal of this stage is to calculate specific capacitance effects with the generated table. This manipulation is necessary since the capacitance calculated between any two wires is the total capacitance between them. However, a user may wish to ascertain how much capacitance pertains to fringe down capacitance..

Figure 3(a) shows the ParallelPlate.pml test structure. Figure 3(b) shows the OneArray.pml test structure, representing three single conductors over a ground plane. The total capacitance calculated between L1p and B_gnd conductors in Figure 3(b) includes fringe capacitance, termed OA_FD, and area capacitance, termed OA_Carea. The total capacitance between L1p and B_gnd is writable as:

$$OA_Ctotal = OA_Carea + 2 \times OA_FD, \quad 2.1$$

where the fringe capacitance is written as:

$$OA_FD = (OA_Ctotal - OA_Carea) / 2. \quad 2.2$$

OA_Carea in equation 2.2 is obtained from using the test structure of figure 3(a), where

$$PP_Ctotal = PP_Carea. \quad 2.3$$

PP_Carea must be scaled by the width of L1p to obtain OA_Carea, therefore:

$$OA_Carea = OneArrayLayer1Width \times PP_Carea. \quad 2.4$$

After obtaining the area capacitance component of the total capacitance between L1p and B_gnd, the fringe capacitance component is easily calculated from Equation 2.2.

It is evident from the description above that a user must:

- identify what capacitance effect to examine
- identify which test structures are required for effect examination
- identify what respective user calculations are required

A demonstration of the *LISA* commands used to obtain the fringe capacitance is detailed below:

```
column_vector_op(table_OA, "PP_Ctotal", table_OA,
  "OneArrayLayer1Width", table_OA, "OA_Carea",
  "**");
```

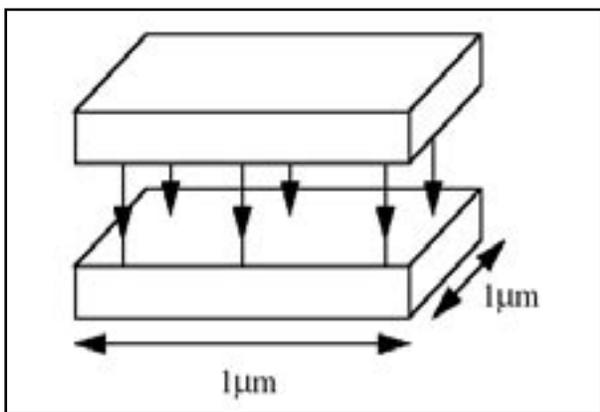


Figure 3(a). ParallelPlate.pml test structure. Capacitance effects are indicated by bold arrows.

```
column_vector_op(table_OA, "OA_Ctotal",
  table_OA, "OA_Carea", table_OA, "OA_FD_
  alpha", "-");
column_scalar_op(table_OA, "OA_FD_alpha",
  table_OA, "OA_FD", "/", 2.0);
```

The above commands highlight scalar operations and vector operations that exist in a *LISA* analysis script.

3.2.1 Scalar Operation

A Scalar operation involves a number operating on a quantity in the table. The for-mat for a scalar operation must follow:

- 1) Key word: column_scalar_op.
- 2) Inside the parentheses: SOURCE ADDRESS: specific table name, column in table.
- 3) Inside the parentheses: ADDRESS TO WHICH RESULTS ARE WRITTEN: specific table name, column in table.
- 4) Inside the parentheses: operation to perform
- 5) Inside the parentheses: number to use

3.2.2 Vector operation.

A vector operation involves a quantity in a table operating on a quantity in a table. The column_vector_op format must follow:

- 1) Key word: column_vector_op
- 2) Inside the parentheses: SOURCE 1 ADDRESS: specific table name, column in table
- 3) Inside the parentheses: SOURCE 2 ADDRESS: specific table name, column in table
- 4) Inside the parentheses: ADDRESS TO WHICH RESULTS ARE WRITTEN: specific table name, column in table
- 5) Inside the parentheses: operations to perform

3.2.3 Data fitting.

In addition to the capacitance effects in Figure 3(b), there are additional effects in test structure OneArray.pml (Figure 4). A comparison of the fringe capacitance in Figures 3(b) and 4 shows that some of the would be

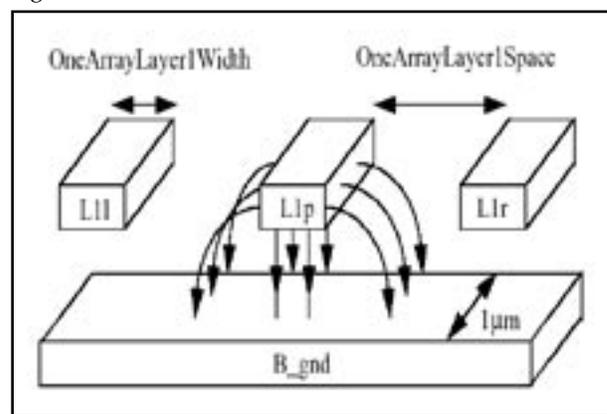


Figure 3(b). OneArray.pml layout. Capacitance effects are indicated by the bold arrows.

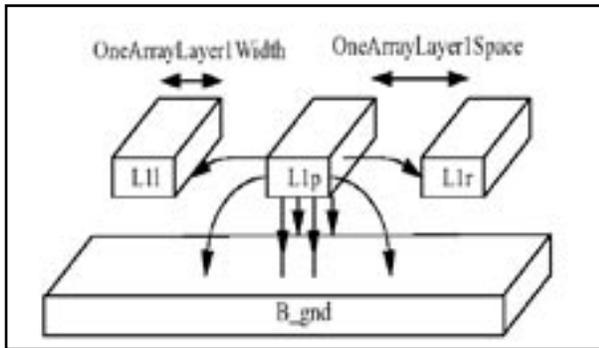


Figure 4. Test structure OneArray.pml. Capacitance effects are indicated by the bold arrows.

fringe down field lines from L1p now terminate on L1l and L1r. Since this significant only when the two conductors are sufficiently near to one another, this is termed a near body effect.

The requirement is to obtain an analytical expression for the fringe capacitance between L1p and B_gnd, while taking the near body effect into account. These well-known expressions are typically obtained from the specific LPE manual, but require the process-specific capacitance coefficients obtained through *Exact's* fitting routines.

In this example, the expression takes the form:

$$C_{\text{fringe}} = K1 * (1.0 - \exp(-K2 * (\text{distance} + K3)))$$

where the coefficients K1, K2 and K3 are calculated by the fitting routine. For example, in the DOE of the *Exact* experiment, OneArrayLayer1Space varies from 0.1 to 5 microns (Figure 5). The capacitance between wires L1p and B_gnd is calculated over this range. Since Exact calculates the total capacitance between any two conductors, it is first necessary to obtain the values of fringe down capacitance as a function of near body distance. Once done, a column containing this capacitance information as well as column containing conductor spacing information appears in the table.

To then perform a numerical fit on the data, used the equation that is described in the *LISA* script. For example:

$$\text{equationFD} = \text{"OA_FD} = 1.0 * K1 [0.01] * (1.0 - \exp(-K2 [0.09] * (\text{\${OneArrayLayer1Space}} + K3 [0.03])))\text{"};$$

OA_FD and OneArrayLayer1Space are variables in the table that identifies, respectively, the fringe down capacitance data and the spacing between the two conductors. The variable equationFD holds the description of the equation. The conditions for fitting routine calculated coefficients are set via []. Once the equation is described, the numerical is performed with:

```
res_OA = (calculate_fit(equationFD)(table_OA)
(sum_combinations(OA_combinations))("FD_OA.rsm")
("Downhill-Simplex"));
```

In this command, res_OA is used to store the values of the calculated coefficients. Within the parentheses of the key word calculate_fit are the following:

- 1) The name of the fitting routine equation described in the *LISA* script
- 2) The name of the table that contains the data
- 3) The number of combinations for the fit
- 4) The name of the response surface model, which in this case is FD_OA.rsm. Users can choose to not save the RSM file by giving a file name of "".
- 5) The name of the chosen fitting method

On completion of the fitting routine, the user saves the file containing the coefficients by using the following *LISA* syntax

```
save_table(res_OA, CSV, "OA_FDcoeff.csv");
```

A extract from this file is detailed below:

```
AVG_ERROR, K1, K2, K3, LAYER0, LAYER1, MAX_ERROR
0.963929, 0.0454768, 0.444801, 0.0874414, metal1, metal2,
6.01101
```

The analytical expression that describes the fringe down capacitance with near body effect is plotted against the actual calculated data using these coefficients (Figure 6).

3.3 Stage 3: Output

After completing the data manipulation, it may be necessary to write out capacitance rule files to use with a layout parasitic extraction (LPE) tool. The *LISA* command form for writing to these files remains the same for any LPE tool. Users must consult the respective LPE manual for the required syntax. An example *LISA* command for writing out a string is:

```
write_parameters("eg1.xcl", table_PP, {"\n/
/ Example string\n"});
```

Each write_parameters command follows:

1. Key word write_parameters

Continued on page 14 ...

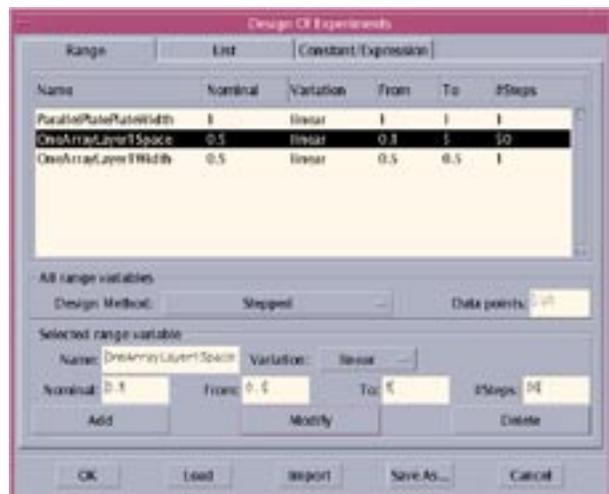


Figure 5. Design of Experiments layout GUI.

Calendar of Events

February

1
2 DesignCon - Santa Clara, CA
3 DesignCon - Santa Clara, CA
4 DesignCon - Santa Clara, CA
5 DesignCon - Santa Clara, CA
6
7
8
9
10
11
12
13
14
15
16 DATE - Paris, France
17 DATE - Paris, France
18 DATE - Paris, France
19 DATE - Paris, France
20 DATE - Paris, France
21
22
23
24
25
26
27
28
29

March

1
2
3
4
5
6
7 NanoTech - Boston, MA
8 NanoTech - Boston, MA
9 NanoTech - Boston, MA
10 NanoTech - Boston, MA
11 NanoTech - Boston, MA
12
13
14
15 GOMACTech - Monterey, CA
16 GOMACTech - Monterey, CA
17 GOMACTech - Monterey, CA
18 GOMACTech - Monterey, CA
19
20
21
22 ICMTS - Hyogo, Japan
23 ICMTS - Hyogo, Japan
24 ICMTS - Hyogo, Japan
25 ICMTS - Hyogo, Japan
26
27
28
29
30
31

Bulletin Board



NSTI Nanotechnology Conference

Nanotech is the largest Nanotechnology conference in the world providing collaborative direction to the growing community of nano science, technology and business. The Nanotech conference is the singular event where these emerging technologies first reach reality. Nanotech provides a full four-day conference program with keynotes, workshops and breakout sessions.



DATE Conference in Paris France

DATE has become the pre-eminent European conference addressing research and development activities in the field of design technology. World leading companies in multimedia, wireless communications, and automotive industries have led to the emergence of recognised European strengths in System-on-Chip Technologies, particularly Embedded Systems with a strong analogue and mixed-signal content.



Request for Feedback

Simulation Standard has been published in basically the same format for over 10 years. In an effort to increase the value of Simulation Standard to our readers, we would appreciate your feedback on how we can improve the publication in terms of content, distribution or organization as we move it from a paper document to a web publication. We appreciate your feedback.

ken.brock@silvaco.com

If you would like more information or to register for one of our workshops, please check our web site at <http://www.silvaco.com>

The Simulation Standard, circulation 18,000 Vol. 14, No. 2, February 2004 is copyrighted by Silvaco International. If you, or someone you know wants a subscription to this free publication, please call (408) 567-1000 (USA), (44) (1483) 401-800 (UK), (81)(45) 820-3000 (Japan), or your nearest Silvaco distributor.

The following trademarks and service marks are the property of Silvaco International. Registered Marks:® Virtual Wafer Fab, Silvaco. Trademarks:™ Simulation Standard, ATHENA, Analog Alliance, Legacy, Manufacturing Tools, Automation Tools, SFLM, VICTORY, Ranger3D Nomad, VYPER, SmartSpice, PSTATS, UTMOST IV, Measure, DISCOVERY, MERCURY, Optolith, TCAD Driven CAD, TonyPlot3D, RESILIENCE, Flash, ATHENA Interpreter, Interactive Tools, DeckBuild, DevEdit, ANALOG EXPRESS, CELEBRITY, SSuprem3, ATLAS, ATLAS Interpreter, Luminous2D/3D, MC Implant, S-Pisces, TonyPlot, FastLargeSignal, SmartStats, Ferro, DevEdit3D, Interpreter, Quantum2D/3D, SDDL, Circuit Optimizer, MaskViews, TFT2D/3D, Radiant, SSuprem4, Elite, FastBlaze, Mocasim, Silicides, MC Depo/Etch, FastNoise, Clarity, Blaze/Blaze3D, Device3D, Frontier, TwinSim, MixedMode2D/3D, VCSELS, Maverick, Envoy, Giga2D/3D, FastGiga, Guardian, Scout, FastMixedMode, Laser, Dragon, Expert, Spirit, Beacon, Savage, Harm, Zenith, Vision, Scholar, SN, UTMOST, UTMOST II, UTMOST III, UTMOST IV, PROMOST, SPAYN, ExpertViews, UTMOST IV Fit, FastSpice, Twister, Blast, MixSim, SmartLib, TestChip, Promost-Rel, RelStats, RelLib, Ranger, LISA, QUEST, EXACT, CLEVER, STELLAR, HIPEX-RCR, HIPEX-Net, HIPEX-RC, Connecting TCAD to Tapeout, and UTMOST IV Spice Modeling. All other product or company names are trademarks of their respective owners.

Hints, Tips and Solutions

William French Ph.D., Applications and Support Manager

Q. How can I use the EXTRACT commands to find the depletion widths in my MOSFET at different drain biases ?

The EXTRACT feature within the *DeckBuild* application is a powerful feature but requires experience to write the correct syntax. We shall show how it may be used on a structure file to find depletion widths.

To illustrate the use of this statement to find depletion widths we have used the standard MOSFET example *mos1ex01.in* to first create the structure. Then the drain voltage was swept to 5V and a structure was saved at this bias. Figure 1 shows this structure and has plotted the junction and the depletion edges.

To extract the depletion width from a particular structure we must first define what is the edge of the depletion region. Typically the depletion edge is assumed to be where the majority carrier concentration is equal to one half of the doping concentration. Once the location of the two edges are found the depletion width can be calculated. We shall now describe how this can be translated into EXTRACT syntax.

First EXTRACT is initialised with the appropriate file which in this case is the device with 5V applied. Any following EXTRACT statements will operate on this two-dimensional structure file.

```
extract init inf="vd5v.str"
```

Next we calculate from the surface of the silicon the depth at which the calculated electron carrier concentration is equal to one half of the donor doping concentration. We have selected a point at $x = 1.1\mu\text{m}$ to extract the depletion edge "Dxn"

```
extract name="Dxn" x.val from curve(depth, \  
(impurity="Electron Conc" material="Silicon" mat.occno=1 x.val=1.1) \  
/ (impurity="Donor Conc" material="Silicon" mat.occno=1 x.val=1.1)) \  
where y.val=0.5
```

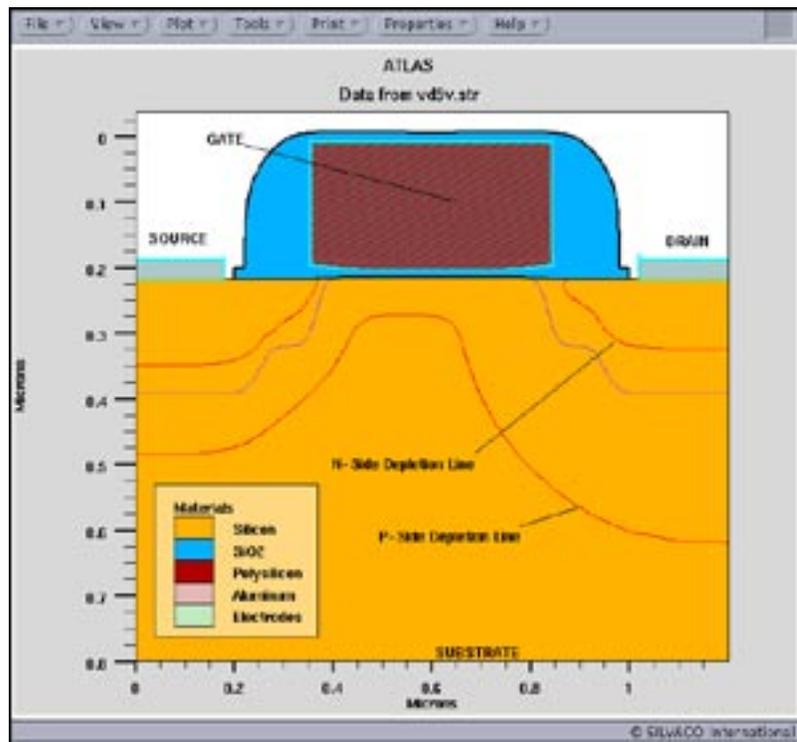


Figure 1. The standard MOSFET structure with the drain biased to 5v that shows the depletion regions.

Next we calculate from the surface of the silicon the depth at which the calculated hole carrier concentration is equal to one half of the acceptor doping concentration. We have selected a point at $x = 1.1\mu\text{m}$ to extract the depletion edge "Dxp"

```
extract name="Dxp" x.val from curve(depth, \  
(impurity="Hole Conc" material="Silicon" mat.occno=1 x.val=1.1) \  
/ (impurity="Acceptor Conc" material="Silicon" mat.occno=1 x.val=1.1)) \  
where y.val=0.5
```

Finally we can use the ability of EXTRACT to perform calculations on EXTRACT variable names to find the depletion width.

```
extract name="Depletion Width @ x=1.1um" = "$Dxp - $Dxn"
```



Figure 2. DeckBuild window that shows the runtime output of the EXTRACT commands.

For the device in Figure 1 the results from this extraction are shown in Figure 2. The depletion width of 0.29um is the same as the depletion width shown in Figure 1. This analysis allows an easy way for the depletion width to be extracted either at different x coordinates or from different structures which have different applied voltages.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department
 Phone: (408) 567-1000 Fax: (408) 496-6080
 e-mail: support@silvaco.com

Hints, Tips and Solutions Archive

Check our our Web Page to see more details of this example plus an archive of previous Hints, Tips, and Solutions
www.silvaco.com

...continued from page 11

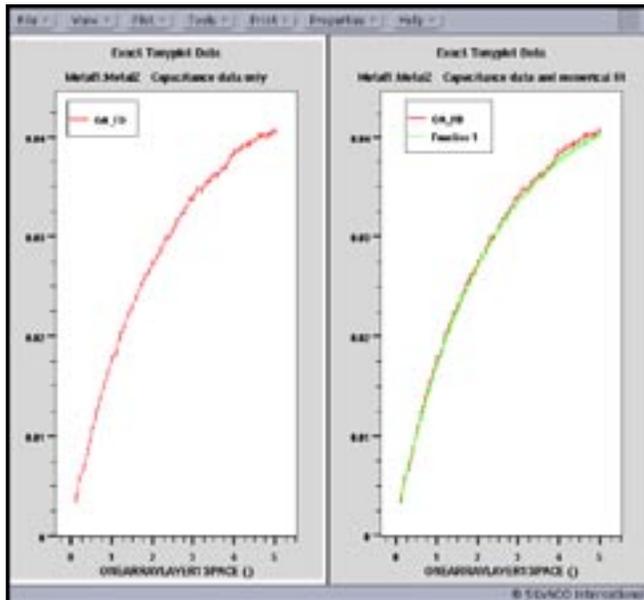


Figure 6: Calculated capacitance data (left figure) and calculated capacitance data with numerical fit (right figure).

The arguments inside the parentheses follow:

- The file to write the text string to
- The table containing the data referred to in the text string, if applicable
- The actual string within braces

Another example for writing out a string is given:

```
write_parameters("eg1.xcl", res_OA, {"CAPACITANCE
CROSSOVER FRINGE ", "LAYER0", " ", "LAYER1", "\
\n\n\n C =length()*", "k1", "(1.0-exp(-", "k2",
"*(distance()+", "k3", "))\n\n\n\n});
```

The expression contains the fitting routine's calculated coefficients, so the coefficient values must appear in the text. This output requirement is obtained by parsing the entire string with segments of the text and coefficients contained within braces. Each segment must reside within inverted commas and is separated from other segments by commas. If the format is not strictly followed, then nothing will appear in the string output.

Output operations are performed throughout the *LISA* script. In addition, simpler output commands exist (to output a table, for example):

```
save_table(table_PP, CSV, "PPa.csv"); or directly
in Tonyplot format by:
```

```
save_table(table_OA, TONYPLOT, "OA_c.str");
```

4. Conclusion

Exact's analysis stage is algorithm-intensive and benefits greatly from proper scripting techniques. This article should help users to easily write scripts for a specific process technology.

Join the Winning Team!

- PROCESS AND DEVICE APPLICATION ENGINEERS
- SPICE APPLICATIONS ENGINEERS
- CAD APPLICATIONS ENGINEERS
- SOFTWARE DEVELOPERS

EMAIL TO: CAREERS@SILVACO.COM



SILVACO

INTERNATIONAL

USA Headquarters:

Silvaco International

4701 Patrick Henry Drive, Bldg. 2
Santa Clara, CA 95054 USA

Phone: 408-567-1000

Fax: 408-496-6080

sales@silvaco.com

www.silvaco.com

Contacts:

Silvaco Japan

jpsales@silvaco.com

Silvaco Korea

krsales@silvaco.com

Silvaco Taiwan

twsales@silvaco.com

Silvaco Singapore

sgsales@silvaco.com

Silvaco UK

uksales@silvaco.com

Silvaco France

frsales@silvaco.com

Silvaco Germany

desales@silvaco.com

*Products Licensed through Silvaco or e*ECAD*

