Simulation Standard

Connecting TCAD To Tapeout

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Resistor and Capacitor L/W Parameters in LVS Comparison

Introduction

In the design of VLSI circuits the situations occur very often when a single schematic device is implemented in the layout by the group of several devices connected in parallel or series. Such groups of devices must be reduced to a single device in the layout and the circuits must be compared in terms of the single devices taking into account their geometrical characteristics. In this article we introduce some methods of calculation and comparison of geometrical parameters of resistors and capacitors connected in parallel or series, when LVS verification is performed.

Resistor L/W parameters

Guardian LVS reduces the group of parallel resistors to a single resistor, if the **Parallel merge** option in **Models Settings** panel for resistors is on. All resistors in the group must have the same type, the same number of terminals and each terminal of a resistor must be connected to the same or swappable terminal of another resistor (see Figure 1). All optional (bulk) terminals of resistors must be connected to the same net.

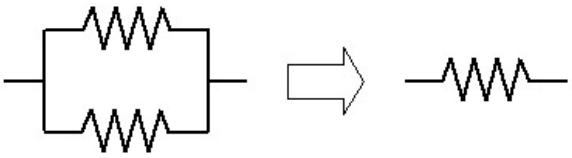

Figure 1. Parallel Resistor Reduction

Guardian LVS calculates, along with resistance, the width and length of resultant resistor using the following formulas:

$$W = \sqrt{P * Q}$$

$$L = \sqrt{\frac{P}{Q}}$$

where P and Q are calculated as

$$P = W_1 * L_1 + W_2 * L_2 + \cdots + W_n * L_n$$

$$Q = \frac{W_1}{L_1} + \frac{W_2}{L_2} + \cdots + \frac{W_n}{L_n}$$

where W_i and L_i. are width and length of the *i-th* resistor, respectively.

Guardian LVS can reduce also a group of serial resistors to a single resistor, if the **Series merge** option in **Models Settings** panel for resistors is on. All resistors in the group must have the same type and the same number of terminals (see Figure 2). All positive and negative terminals must be connected in series. As the positive and negative terminals of resistor are always swappable, the positive-to-positive, positive-to-negative, negative-to-positive, and negative-to-negative connections are admissible for the reduction. All optional (bulk) terminals of resistors must be connected to the same net.

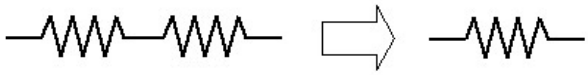

Figure 2. Serial Resistor Reduction.

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The width and length of resultant resistor are calculated as follows:

$$W = \sqrt{\frac{P}{Q}}$$

$$L = \sqrt{P * Q}$$

where P and Q are calculated as

$$P = W_1 * L_1 + W_2 * L_2 + \cdots + W_n * L_n$$

$$Q = \frac{L_1}{W_1} + \frac{L_2}{W_2} + \cdots + \frac{L_n}{W_n}$$

where W_i and L_i are width and length of the i-th resistor, respectively.

The parameters of matched resistors can be checked during netlist comparison using **Match parameters** and **Match aux parameters** options (see Figure 3). There are three combinations to check the resistor parameters:

- check only resistance values of matched resistors;
- check the length and width of matched resistors;
- check the resistance, length, and width of matched resistors.

You can change the tolerance and the default values of resistance, length, and width parameters. Initial values for default length and width and their tolerance are 1e-6m and 10%, respectively.

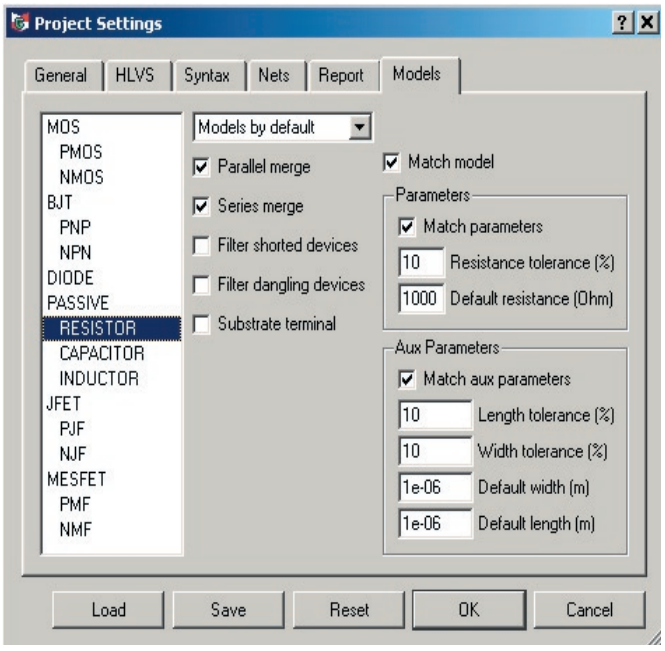

Figure 3. Resistor Parameters

If ***Guardian LVS*** finds a mismatch for at least one parameter, all parameters of matched resistor pair are reported in **Parameter Error** report like:

```
L1: R: top:X9:RH14 ..... = (#)  RX:XI2:XI3:XI0<2>:RI#32
       R=1300                    R=1300
       L=62u  W=5u               L=50u  W=5u
```

Note that **Match parameters** and **Match aux parameters** options help LVS to resolve node automorphism. When there are equal groups of devices that can't be distinguished from each other, additional information is needed for matching. Comparing device parameters helps LVS to match devices. But, if all devices within a group have the same parameters, LVS can't differentiate between group members. In this case, you can set the initial correspondence points to resolve node automorphism and reduce verification time.

Capacitor L/W Parameters

Guardian LVS can reduce a group of parallel capacitors to a single capacitor, if the **Parallel merge** option in **Models Settings** panel for capacitors is on. All capacitors in the group must have the same type, the same number of terminals. All positive, negative, and optional (bulk) terminals must be connected to the same nets (see Figure 4). Note that positive and negative terminals can be swapped, if **Swap terminals** option is on.

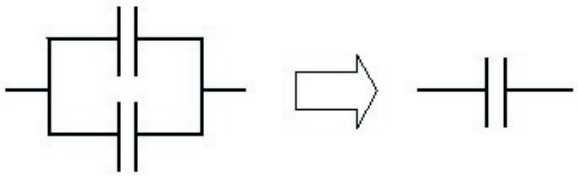

Figure 4. Parallel Capacitor Reduction

Guardian LVS calculates, along with capacitance value, the width and length of resultant capacitor using the following formulas:

$$W = \frac{P - \sqrt{P^2 - 16 * A}}{4}$$

$$L = \frac{P + \sqrt{P^2 - 16 * A}}{4}$$

where A and P are area and perimeter of resultant capacitor calculated as:

$$A = L_1 * W_1 + L_2 * W_2 + \cdots + L_n * W_n$$

$$P = 2 * (L_1 + W_1 + L_2 + W_2 + \cdots + L_n + W_n)$$

where W_i and L_i are width and length of the i-th capacitor, respectively.

Note that *L* and *W* parameters of resultant capacitor can be calculated, if $P^2 - 16 * A \geq 0$.

Guardian LVS reduces a group of serially connected capacitors to a single capacitor, if the **Series merge** option in **Models Settings** panel for capacitors is on. All capacitors in a group must have the same type, the same number of terminals.

The positive and negative terminals must alternate within series, unless **Swap terminals** option is on. All optional (bulk) terminals must be connected to the same nets (see Figure 5).

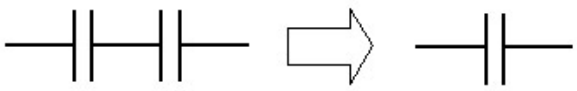

Figure 5. Serial Capacitor Reduction

There are no formulas for calculation of the width and length of capacitor obtained by serial reduction. Only the capacitance value can be calculated.

The parameters of matched capacitors (same as resistors) can be checked during netlist comparison using Match parameters and Match aux parameters options. If these options are on, the capacitance, length, and width of matched resultant capacitors, connected in parallel, are compared and reported, as in example below:

```
L0: C:($)  TN007:CI157 ..... = ($) TN007:CI157
          C=1.01507E-011              C=1.01507E-011
          L=268.478u W=30.6359u       L=268.478u W=30.6359u
```

If the length and width can't be calculated (for example, for serial capacitor reduction), the capacitance values of matched resultant capacitors and the length and width of capacitors forming the resultant capacitor are compared and reported like:

```
L0: C:($)top:C1 ............ = (@#) S3:XS2:C2
          C=1.97464E-012              C=1.97464E-012
          top:C1                      S3:XS2:C2
          L=123.038u  W=36.212u       L=103.038u  W=37.212u
          top:C3                      S3:XS2:C2
          L=103.038u  W=37.212u       L=103.038u  W=37.212u
```

Conclusion

Described methods of calculation and comparison of resistor and capacitor geometrical parameters are realized in Guardian LVS verification tool. This allows designers to execute more detailed comparison of the netlists representing the layout and the schematic of a circuit.