HIPEX-NET:
New SILVACO Full-Chip LPE Tool vs. Maverick

SILVACO is releasing its new layout parameter extractor: ***HIPEX-NET***. The new tool will replace Silvaco's ***Maverick***, which is a part of ***Guardian*** LVS/ERC. While being fully compliant with ***Maverick***, ***HIPEX-NET*** has many advantages over ***Maverick***. The comparison chart in Table 1 shows the critical features, which make ***HIPEX-NET*** much more powerful for layout verification than ***Maverick***.

HIPEX-NET is a full-chip hierarchical netlist extractor. It can handle very complex layout hierarchy, this is in stark contrast to ***Maverick*** , where ***Maverick*** must flatten the layout. As a result, ***HIPEX-NET*** works much faster and needs less memory to process big hierarchical layouts. Today ***HIPEX-NET*** successfully extracts 10 million transistor layouts on Win32 platform, which provides only 2GB of virtual memory. The 64-bit version available for SunOS can handle much larger layouts.

Unlike many other hierarchical tools on the market, ***HIPEX-NET*** doesn't require additional efforts when preparing a mask layout. The user doesn't have to define cell ports. ***HIPEX-NET*** performs best with a true hierarchical design, however it also can deal with hierarchy violations by exploding individual cells. The user has means to make ***HIPEX-NET*** identify hierarchy violations and explode appropriate cells automatically during the extraction. Since this decreases performance, the better way is to indicate cells for explosion manually before starting extraction (pre-exploding). When using ***HIPEX-NET*** within the Expert framework, it is possible to run ***HIPEX-NET*** for hierarchy checking only. Then, the user can easily pre-explode cells from the list generated during the checking.

Besides greater performance, hierarchical extraction produces results that are easier to understand. A hierarchical netlist is much more compact and readable. The new Node Probing implementation in ***Expert***, which is now based on the layout annotation database produced by ***HIPEX-NET*** rather than ***Maverick***, allows one to trace a node path through nested instances of cells. Besides nets and devices, it is now possible to highlight separate instances by their name or by clicking on them with the mouse.

Unlike ***Maverick***, ***HIPEX-NET*** properly uses the design text to name nets. As a hierarchical extractor, it allows the designer to use text labels of the three types: global, local, and port. Global text labels have the highest priority and thus name nets in the whole layout. Local text labels nets in a given cell. Port text label have the lowest priority and are intended to name user-defined cell ports only (it is not necessary but possible to predefine cell ports in ***HIPEX-NET***).

HIPEX-NET also uses the design text to perform Electric Rule Checking (ERC). ERC checks for open and short circuit nets. ***HIPEX-NET*** reports a global (local) open if two or more unconnected nets are named by the same global (local) text label. A short circuit is reported if one net is named by two or more different text labels of the same priority. In addition, ***HIPEX-NET*** can report dangles (nets that have no device connections), badly formed devices (e.g., with missing pin connections or with shorted pins), and perform an integrity check. ***HIPEX-NET*** writes in the summary file detailed information about every ERC error, including layout local coordinates, layer names, and text labels.

Feature	HIPEX	Maverick
SPICE netlist extraction	Hierarchical and flat	Flat only
Parameter extraction of transistors (MOSFET, MESFET, JFET, BJT) and design diodes, resistors, and capacitors	Yes	Yes
Integration with SILVACO layout editor, ***Expert***	Yes	Yes
Hierarchical extraction	Yes	No
Advanced processing of net names	Yes	No
Schematic backannotation	Yes	No
Compatibility with ***HIPEX*** parasitic tools	Yes	No

Table 1. HIPEX-NET vs. Maverick: features comparison chart

As part of the ***HIPEX*** family, Silvaco introduces a full-chip parasitic tool: ***HIPEX-RC.*** It divides parasitic extraction into three stages (see Figure 1). First, ***HIPEX-R*** performs parasitic resistance extraction. It produces the layout SPICE netlist annotated with parasitic resistances and the internal resistance database (RDB). ***HIPEX-R*** also creates an internal net database that stores geometrical and electrical information about all the nets, including parasitic subnets that correspond to parasitic resistor terminals. Second, the net database is used as input to ***HIPEX-C*** to extract parasitic capacitances between nets. ***HIPEX-C*** produces the SPICE netlist containing parasitic coupling capacitors and the internal capacitance database (CDB). Finally, RDB and CDB are combined into the distributed parasitic RC-network either in SPICE or DSPF format. This can be further processed by the RC-network reduction tool: ***HIPEX-CRC***.

Since both ***HIPEX-R*** and ***HIPEX-C*** produce ready-to-use SPICE netlists, they can be used separately. This way ***HIPEX-NET*** is used to create the net database (without parasitic subnet information) needed by ***HIPEX-C***.

If the layout netlist extracted by ***HIPEX-NET*** passes LVS verification, the designer can backannotate the schematic netlist with parasitic capacitances and resistances extracted by ***HIPEX-RC***.

HIPEX-NET can be used from ***Expert*** or in standalone mode. The extractor is available for Win32, SunOS 32- and 64-bit, and Linux platforms.

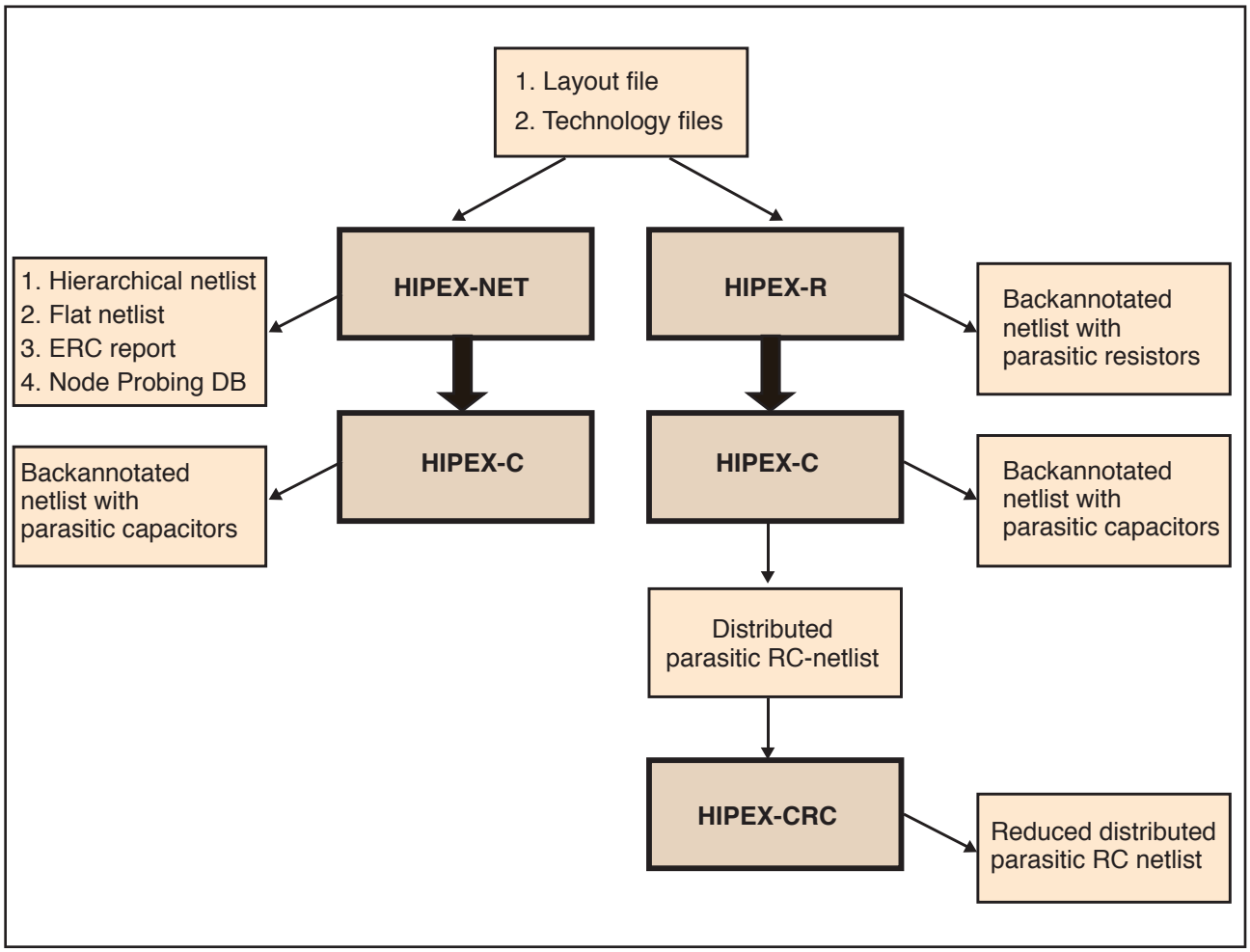

Figure 1. Hipex execution flow.