Parasitic Resistor Extraction with *HIPEX-R*

Introduction

Layout parasitic extraction (LPE) plays an important role in the post-layout verification process. Verification of the full chip layout is becoming a more common problem because the size of IC layouts continue to grow due to new IC technologies. The complexity of IC design requires consideration of the effects caused by parasitic capacitors and resistors. Parasitic devices are responsible for such effects such as time delay, voltage drop, and signal integrity violation, all of which impair chip performance.

HIPEX-R is part of the ***HIPEX*** software package for physical verification of multimillion transistor designs. It is a hierarchical full chip parasitic resistance extraction tool.

The ***HIPEX-R*** flow is depicted in Figure 1.

HIPEX-R can read either a GDSII or SLF input design.

The rules according to which ***HIPEX-R*** will extract the parasitic resistors are set in the technology file. Note that ***HIPEX-R*** also extracts the active device defined in ***HIPEX-NET*** technology file (which is also used by ***HIPEX-R***).

A set of options for customizing the extraction are defined in the option file.

Once the extraction is done, ***HIPEX-R*** generates a hierarchical and/or flat SPICE netlist, as well as a GWL/WLDS proprietary format hierarchical netlist (used by ***DistRC*** utility for RC distribution). All the information related to the extraction is output to a summary file.

HIPEX-R can also optionally generate a "stripe" database (SDB), and a resistance database (RDB), containing geometrical and electrical parasitic informations.

The SDB can be used by ***HIPEX-C*** to extract parasitic capacitors, while the RDB will be used by the ***DistRC*** utility (together with the CDB produced by ***HIPEX-C***) for RC distribution.

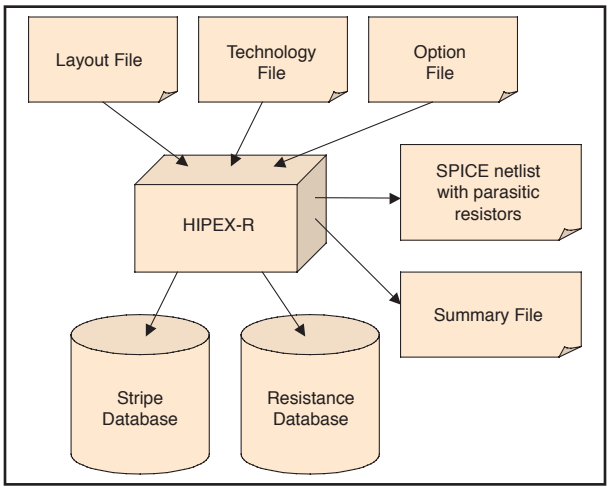

Figure 1. Hipex-R flow.

Features

HIPEX-R can extract two types of parasitic resistors: horizontal resistors and vertical (contact) resistors. It extracts these resistors on the layers specified by the user in the technology file.

The parasitic extraction is based mainly on a fragmentation algorithm that guarantees a decomposition of the parasitic layer into resistors (body and terminals) along an estimated current direction.

During the fragmentation, terminals may be created wherever there are bends (L-shapes, T-shapes, Cross-shapes) or wherever the layer to be extracted touches or overlaps another layer.

Figure 2 represents the main configurations handled by ***HIPEX-R*** fragmentation.

Once the fragmentation is done, the resistor values are calculated according to user-specified sheet and/or area

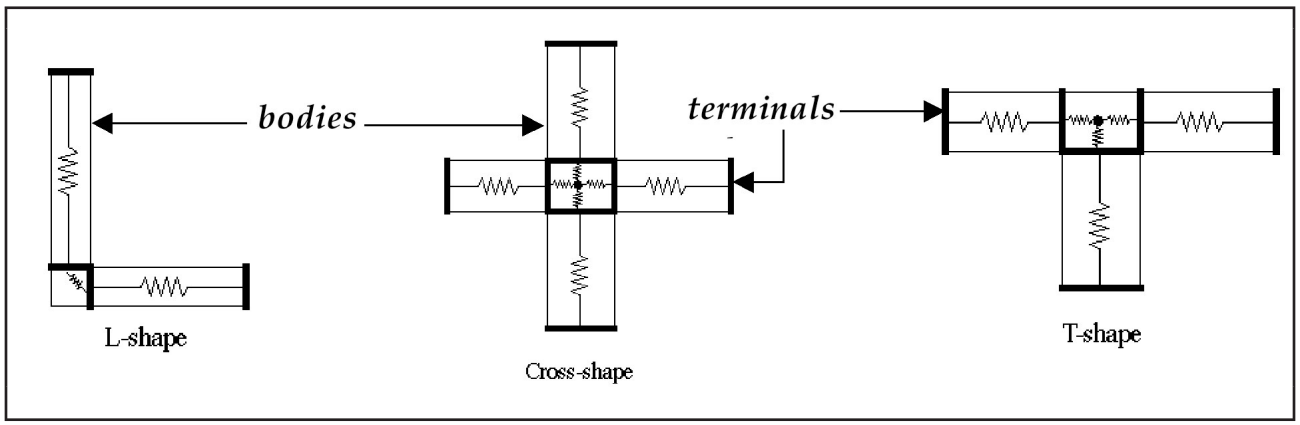

Figure 2. Hipex-R layer fragmentation configurations

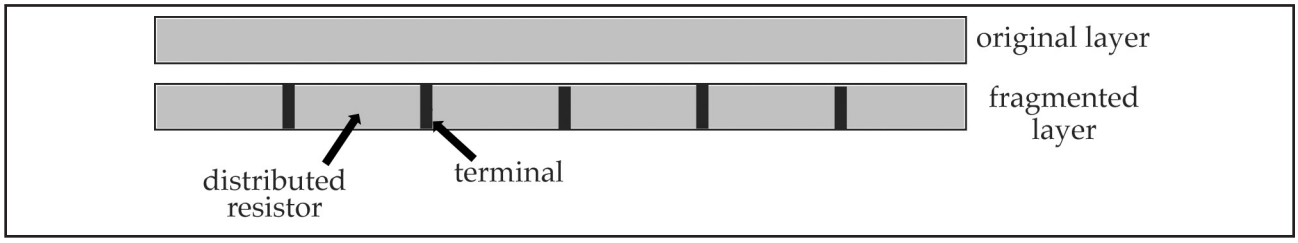

Figure 3. Long resistor fragmentation

resistivities, and the connectivity between the different resistors and the active device is then established or updated.

Finally, parasitic subnode names are assigned to the resistor terminals, and the active device terminal names are updated based on the connectivity information.

The extraction of parasitic resistors is done hierarchically, starting from the deepest substructure of the design. The hierarchical connectivity between instances of substructures in the design is updated throughout the extraction.

HIPEX-R enables you to control the output of the extraction with multiple options.

The main option are described below.

Fragmentation options

- ***HIPEX-R*** enables you to specify the maximum length of a fragmented resistor body. If a resistor body is greater than this value, it will be cut into smaller pieces of length less than or equal to this value. (see Figure 3)
- Contact oversizing and contact clustering are two other options that can be very useful for reducing the number of extracted body resistors and simplify the fragmentation, see Figure 4

Extraction options

- ***HIPEX-R*** enables you to specify a resistance threshold value. All parasitic resistors found with a resistance less than this threshold will be ignored while connectivity is preserved
- ***HIPEX-R*** extraction can be performed either on the whole design or on a specified cell
- ***HIPEX-R*** extraction can be performed on a set of selected nets. It is also possible to ignore a set of specified nets as well as dangle nets

Output options

- ***HIPEX-R*** generates the parasitic netlist in hierarchical and/or flat SPICE format, as well as in hierarchical GWL/WLDS format. Geometrical and physical information can also be outputed to the netlist, such as the coordinates of the parasitic resistors, their size and their layer
- ***HIPEX-R*** can output a layout of all parasitic resistors' geometries (body and terminals) and parasitic nodes as text elements
- Finally, ***HIPEX-R*** can be used to generate the stripe database needed by the capacitor extractor ***HIPEX-C***, and the resistance database needed by ***DistRC*** utility for RC distribution

Conclusion

An introduction to ***HIPEX-R*** features and benefits was presented in this article. Thanks to its hierarchical architecture, this full chip parasitic resistance extraction tool provides quick and efficient algorithms that are able to handle large IC designs. ***HIPEX-R*** can be used as a stand-alone product or as part of the ***HIPEX*** flow.

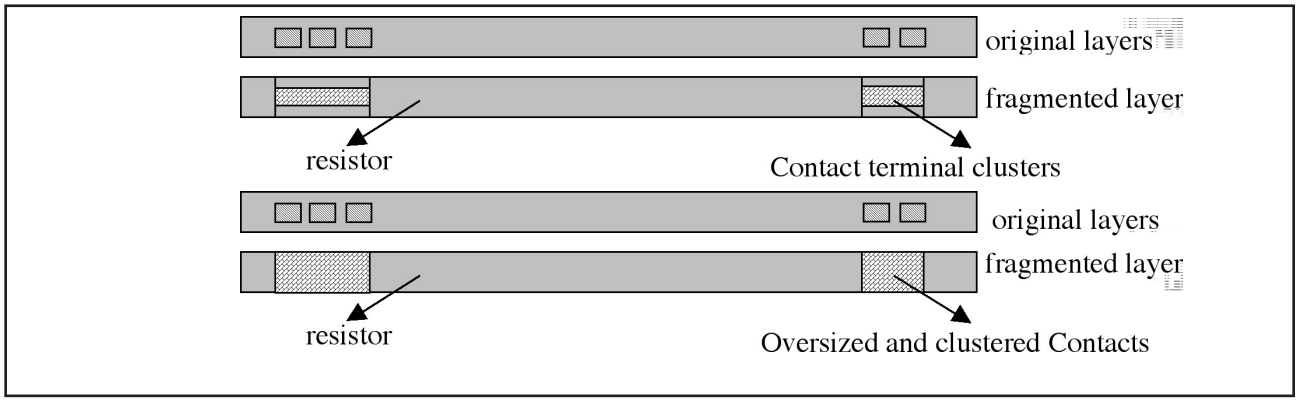

Figure 4. Contact oversizing and clustering