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Low Voltage Super Junction MOSFET Simulation and Experimentation

Timothy Henson, Joe Cao

International Rectifier, 233 Kansas St, El Segundo, CA 90245 USA, Phone +01 310 726 8842, Fax +01 310 726 8847 E-mail: thenson1@irf.com

Abstract

The application of Super Junction concepts to a low voltage power MOSFET is investigated. The body junction is modified with the addition of a high energy implant, resulting in an increased breakdown voltage. Simulations are used to quantify the relationship between dose and breakdown voltage, resulting in a predicted 35% Rds(on) reduction. This is confirmed through experiment, and a 19% reduction in Rds(on) is reported at 75 V. No change in device reliability is observed. This approach provides a simple means to reduce the on resistance of low voltage MOSFETs.

Introduction

High Voltage (600V) power semiconductors using super junctions to achieve greatly reduced on-resistance have been reported for several years[1-3]. The drift region of such devices is comprised of alternating N^- and P^- type regions of equal charge. In the blocking mode, the adjacent N^- and P^- regions deplete into each other laterally. The drift region thus comprises several N^- and P^- regions in parallel, with the N^- regions having much lower resistivity than conventional devices, and therefore presents a lower Rds. These high voltage devices are complicated to manufacture with multiple cycles of epitaxial growth, photo mask, implantation, and drive steps, or very deep trenches.

This paper presents a simple implementation of the super junction concept, utilizing a high energy Boron implant, into low voltage (50-100V) planar n-channel MOSFETS. Through the addition of a high energy implant (1-3 MeV) to form a lightly doped P^- diffusion underneath the standard p-type body diffusion, alternating N^- (EPI) and P^- regions are formed.

Device Structures and Simulations

Process and device simulations were performed to evaluate the proposed structure. An existing model for a state of the art self-aligned contact planar MOSFET with BV ~ 75V

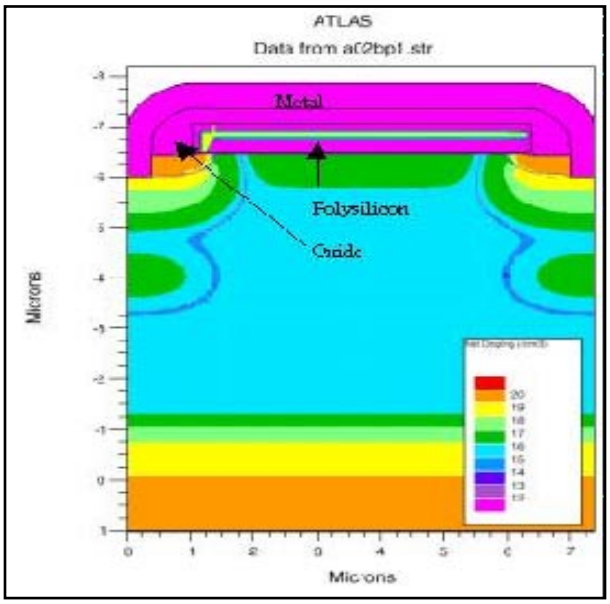

Figure 1. Simulated device with 1.5 MeV High Energy Implant.

was modified to include a high energy implant after the poly etch sequence. The simulated high energy implant is blocked from penetrating the polysilicon gate. Figure 1 shows the net doping of a device that included a 3.0E12, 1.5 MeV Boron implant.

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INSIDE

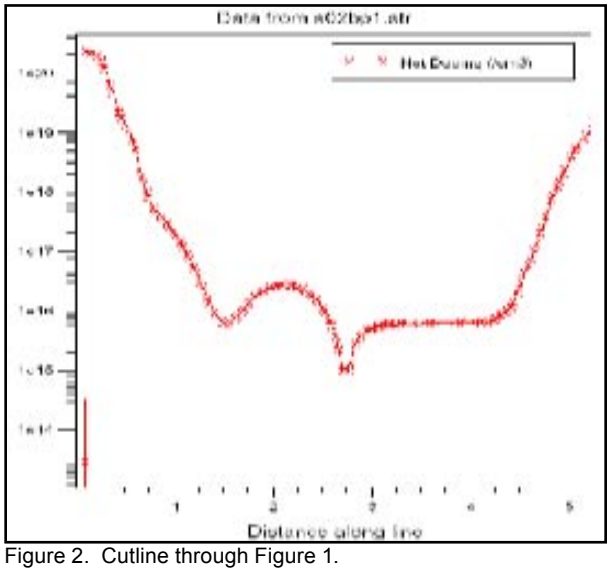

Figure 2. Cutline through Figure 1.

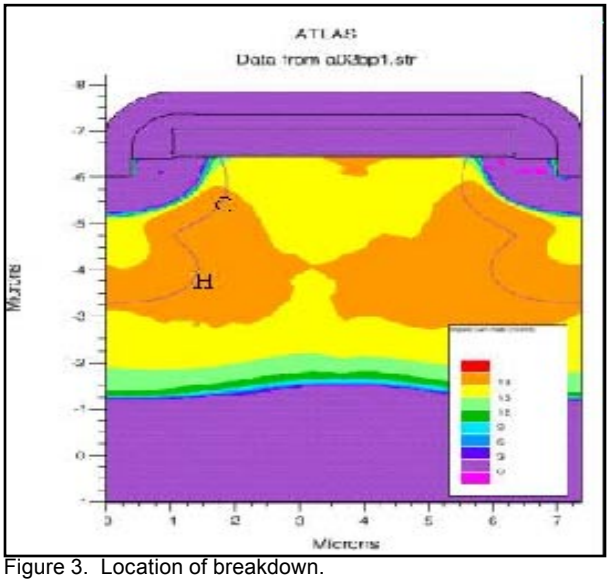

Figure 3. Location of breakdown.

The high energy implant can be seen extending beneath the p-body by about 1 um. High energy implanters are available with energies up to about 3 MeV for Boron, which gives a mean depth in silicon of 3.7 um.

In a traditional super junction, the N^- and P^- type regions are assumed to deplete in the horizontal direction, and thus the N^- and P^- concentrations are equal to achieve charge balance. Because of the limitation in depth from the high energy implanter, the P^- type regions in this case will deplete in both the horizontal and vertical directions. For this reason, the optimum P^- type doping is higher than the N^- type (j-fet and drift region) doping. This can be seen in Figure 2, where the net doping is plotted for a cutline taken through the right edge of the structure in Figure 1.

For conventional MOSFETs of this design, the location of breakdown is typically in the j-fet region at the corner of the body junction. With the addition of the high energy implant, the location of breakdown moves to the region of the deep implant. This is illustrated in Figure 3, showing a simulation of impact ionization for the device of Figure 1. 'H' indicates breakdown (dark colored region) in this simulation with the high energy implant, and 'C' indicates where a conventional device would breakdown.

The simulations indicate that, for a given implant energy, the device breakdown voltage increases as implant dose is increased up to a certain value. As the implant dose is further increased, breakdown voltage reduces. This can be seen in Figure 4, where simulated breakdown voltage is plotted for implant energies of 1.5, 2.0, and 2.5 MeV.

These simulations predict a maximum breakdown voltage increase of 32% for the 1.5 MeV implant and 45% for the 2.5 MeV implant. Higher energies create a deeper alternating N^- and P^- type column structure, and support more voltage in this region.

Deeper N^- and P^- type regions also create a longer effective j-fet, and constrict the current flow in this region, leading to increased on resistance. Based on the 6.6 um cell pitch used on the conventional device, an implant energy of 1.5 MeV is expected to provide a good tradeoff between BV and on resistance. Simulations were run to determine the optimum implant doses at 1.5 MeV for various voltages, based on different starting N^- epitaxial layers. Figure 5 shows simulated results for the on-resistance * Active Area (R*AA) figure of merit typically used to characterize power MOSFETS.

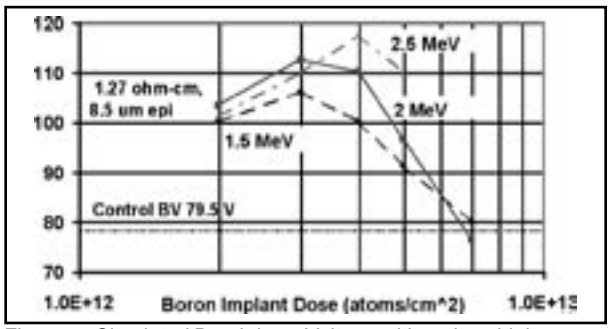

Figure 4. Simulated Breakdown Voltage with various high energy Boron implants.

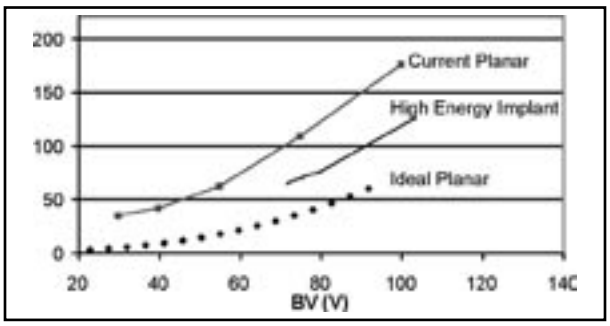

Figure 5. R*AA product for SJ MOSFET based on simulations.

The high energy implant device shows a 35% reduction in R*AA compared to the conventional MOSFET, at a breakdown voltage of 75 V. Also shown is the case of an ideal planar (1-sided) junction. It should be noted that the 'ideal planar' values do not include any contribution from channel and contact resistances that are included in the current planar devices and the high energy implant simulations.

Experimental Results

This high energy implant super junction concept was applied to a state-of-art self-aligned-contact planar MOSFET. The chosen device had a poly line width of 5 um, and a pitch of 6.6 um. The Epi thickness was 8.5 um, with a resistivity of 1.27 ohm-cm to give a nominal BV of 79.5 V. The process flow was identical to the standard FET, except that thicker (3.5 um) photoresist was used for the poly mask. This was necessary to block the high energy implant from the j-fet region. The structure at the high energy implant step is shown in Figure 6.

After the polysilicon gate has been etched, the standard channel implant is replaced by two implants. The first is the typical high dose, low energy channel implant (1.0E14, 80 KeV), and the second is the high energy low dose implant to form the deep P^- type region. Based upon the simulation results, a range of high implant energies (1.5 to 2.5 MeV) and doses (2.0E12 – 7.0E12) was performed.

The rest of the self-aligned contact sequence is left unchanged. This consists of removing the photoresist and performing the channel drive. The source is implanted and driven, as is the shallow p+ region. Then an oxide is deposited and etched back to form oxide spacers on the sides of the poly gates. Finally, the contact etch into the silicon is performed.

For comparison, a SEM of a conventional device with the junctions stained is shown in Figure 7, and a prototype device with the 1.5 MeV implant is shown in Figure 8.

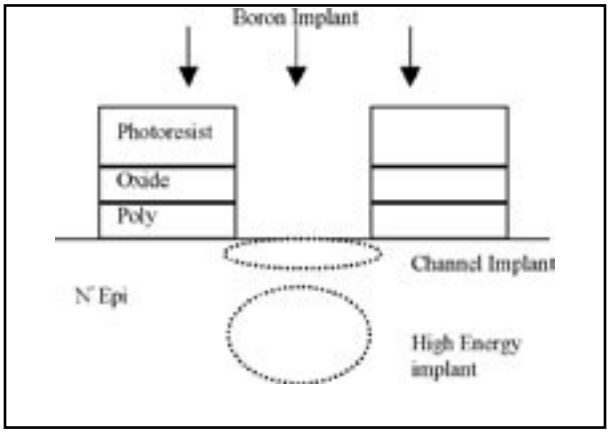

Figure 6. Schematic of structure at high energy implant.

The P^- diffusion, formed in this case by a 1.5 MeV Boron implant, can be clearly seen below the standard body junction.

The high energy implant was activated at the same time as the channel implant. No additional diffusion was desired or necessary because the implant straggle is already quite large (1840 A longitudinal, 2360 lateral at 1.5 MeV). Additional lateral diffusion would increase on resistance by narrowing the conduction (j-fet) region.

Functioning prototype devices were created and tested to compare with simulated values. Experiments follow a similar trend with dose as the simulations, showing an increase in breakdown voltage with the addition of the high energy implant, and then a reduction in maximum BV as the implant dose is increased. These results can be seen in Figure 9.

The maximum voltage predicted by simulations was not achieved, as the prototype device breakdown voltage is limited by the termination. The achieved breakdown voltage represents a 18% increase in BV, compared to the simulated 32%.

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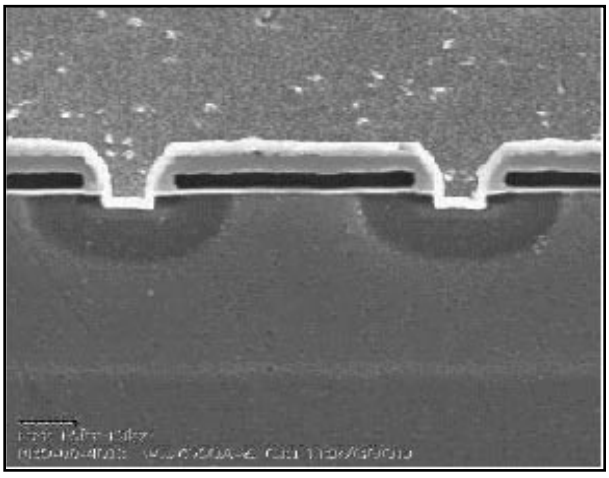
Figure 7. SEM of conventional device.

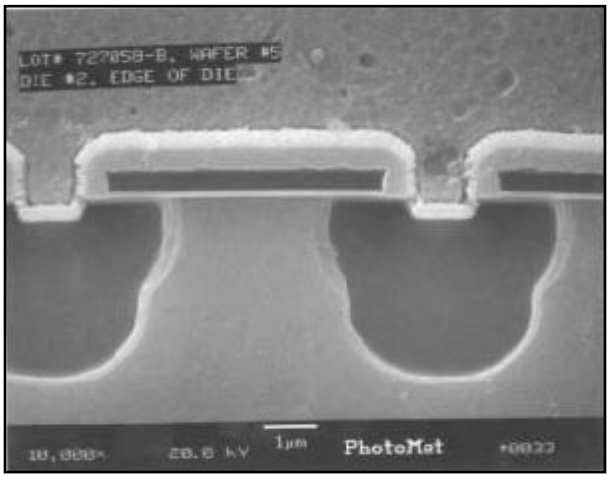

Figure 8. SEM of prototype device with 1.5 MeV Boron Implant.

Using The Statistical Sampling Feature in Silvaco's BCA Monte Carlo Implant Simulator

1.0 Introduction

Silvaco's Binary Collision Approximation (BCA) Monte-Carlo Implantation simulator closely replicates the physics of implantation by individually tracking implanted ions and their resulting interstitial and vacancy damage as the ions collide and interact with atoms in the substrate. The simulator then tracks subsequent ions, gradually building up the implanted ion concentration profile, until the required number of ions is reached.

All implanted ions do not come to rest at the same depth in the substrate due to different interaction with the substrate atoms. An implanted ion that collides head on with a substrate atom at the surface is more likely to come to rest closer to the surface than an implanted ion that channeled between atoms for some distance before colliding head on with an atom.

There is a statistical probability that some implanted ions travel relatively long distances between substrate atoms without encountering a collision event. This is especially true in an ordered structure such as a silicon crystal. On rare occasions, the eventual collision of the travelling ion results in another trajectory that allows a relatively long flight path before another collision. The few implanted ions that travel very deep into the substrate are usually the result of several rare events. Despite their relative rarity, however, the vast amount of implanted ions ensure that even rare events affect the overall implanted profile and must be taken into account.

The graph of a low-energy arsenic implant (Figure 1) illustrates how rare events affect the implantated profile. The few straggling ions that penetrated deepest into the substrate represent these events. If the number of simulated ions were equal to the number of ions actually implanted, these statistical aberrations would accurately reflect reality. Time constraints typically limit the number of simulated ions, however, so each are weighted accordingly. This has a minimal effect on accuracy apart from these rare events, which are considered statistical aberrations at the "tail end" of the implant. If more ions are implanted than simulated, the concentration in the tail of the implant would be smoother in reality than in the simulation. To correct for this, a new algorithm has been implemented in ATHENA. The algorithm is invoked by the "sampling" parameter in the "implant" statement.

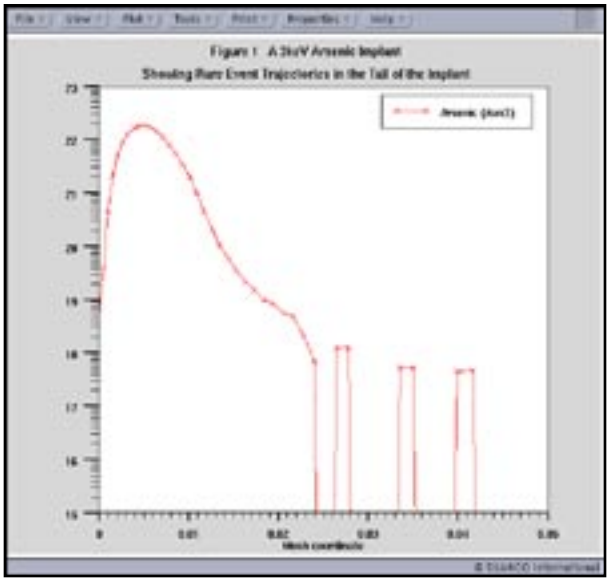

Figure 1. A typical Monte-Carlo simulation of a 3 keV Arsenic implant showing rate event ion trajectories in the tail of the concentration profile.

2.0 Implementation of the Rare Event Correction Algorithm

ATHENA reduces calculation time and improves statistical quality of simulated profiles by means of a three-dimensional rare event algorithm. An implantation profile often differs significantly in concentration value across implantation depth. Low concentrations in the profile are due to the low probability of implanted species (rare events) to reach that point in space. A valid statistics profile is comprised of a number of simulated cascades that are relative to the desired level of accuracy. Depending on device size, implant distributions below a certain threshold concentration value may exhibit significant statistical noise, even in real experiments.

The algorithm uses trajectory splitting to achieve an increased occurrence of rare events by generating several independent sub-trajectories from more common events. The original idea, [1], was first developed into a refined simulation technique by Villién-Altamirano et al., [2]. Their version of this approach is called "restart." The basic idea is to identify subspaces from which it is more likely to reach the rare event's target subspace. Each time these subspaces are reached, current event sequences are split into a number of replicas, all continuing forward from a state of splitting. In this way the number of rare events increase, depending on the number of restart thresholds defined and the amount of replicas generated.

The trajectory-splitting algorithm naturally fits into the problem of Monte Carlo simulation of stopping and ranges, such as ion implantation. A similar method was first used in the work of Phillips and Price, [3], to simulate hot electron transport. The first rare event algorithm that applied to the transport phenomena simulation of ions in matter was used by Yang et al., [4]. Later, Beardmore et al., [5], significantly refined the rare event algorithm. A brief, but comprehensive review of trajectory splitting methods used in modeling of ion implantation is given in [6].

The increased speed of the rare event trajectory splitting technique is due to changes in the statistical behavior that provoke rare events to occur more frequently. ***ATHENA's*** rare event algorithm achieves this by identifying likely subspaces from which to observe a given collision event, and then making replicas of the cascade sequences that reach those subspaces. Figure 2 illustrates the trajectory splitting and the restart of replica events as a new threshold is reached. When applying splitting to collision cascades, or other specific system, the two main parameters to determine are: first, when to split and, second, how many sub-trajectories to create when splitting.

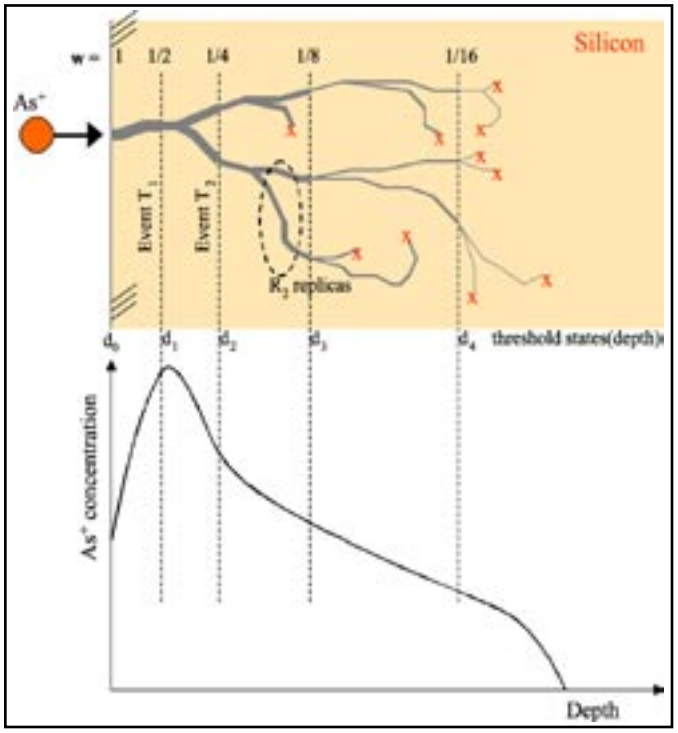

Figure 2. Restarting collision events by splitting at 'm' thresholds.

Different criteria are used to obtain the threshold states when splitting must occur. For example, Bohmayr et al., [7], use a trajectory split method based upon checking the concentration of local dopant molecules at certain points. Beardmore, et al's. rare event algorithm, [5], uses the integrated dose as a criterion for deciding when to split. ***ATHENA*** uses the same criterion to determine the splitting depths. Dose integration is carried out along the radius vectors of ions' co-ordinates, thus, roughly taking into consideration the three-dimensionality of the ion distribution.

Due to the discrete nature of collision cascades, the number of sub-trajectories created at each split depth should be an integer greater or equal to two. Let T i i represent the event at each threshold state (the event of an ion passing through a split depth). The probability of an ion in state T i-1 i-1 to reach T i i state is pi = P(T i i |T i-1 i-1) 1) . Then the recommended number of replications at each threshold (a split depth) is Ri=1/ pi. This relation links the number of replications at each split and the criterion necessary to identify the threshold states (split depths). If Ri=2, then the number of ions passing through split depth, d i i , will be twice smaller than the number of particles passing through split depth d i i . ATHENA's criterion to determine the split depths is the integrated dose along the radius vectors of stopped particles. For example:, split depths d i i , d 2 2 , d 3 3 , etc. will be at integrated doses 0.5ϕ , 0.75ϕ , 0.875ϕ , etc. where ϕ is the total retained implant dose.

In ***ATHENA***, trajectory splitting is turned on with the sampling command in the implant statement. In theory, sampling estimators are unbiased and consistent, as theoretical expectation is obtained from the whole ensemble of sample paths, including very unlikely ones. In practice, the estimate is obtained as the average of finite number of samples. Overbiasing can occur if the only goal is to increase the probability of the event that requires further analysis. Overbiasing usually results in the underestimation of the evaluated probability (dopant concentration, in case of ion implantation). In fact, it has been reported in [8] that when the splitting

parameters are not consistent with the system's large deviations behavior, the probability in question may be severely underestimated. This situation is almost present in ion implant simulators when treating multi-layered targets and two-dimensional layouts. Therefore, splitting should be used with caution. In conclusion:

- Variance reduction is not guaranteed by an increased occurrence probability of the event pending analysis.
- Trajectory splitting should be used carefully. Complex implantation geometry can lead to considerable system behavior deviation, thus overbiasing and underestimating the relevant statistics.

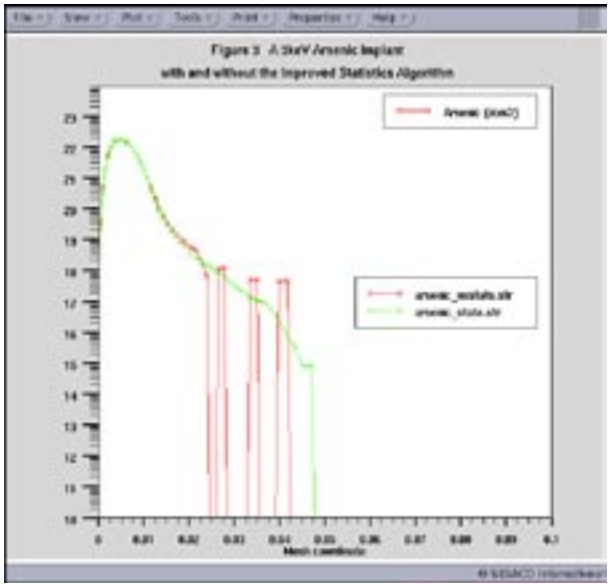

Figure 3. A 3keV Arsenic Implant at 7 degrees from vertical with and without the new statistical algorithm activated.

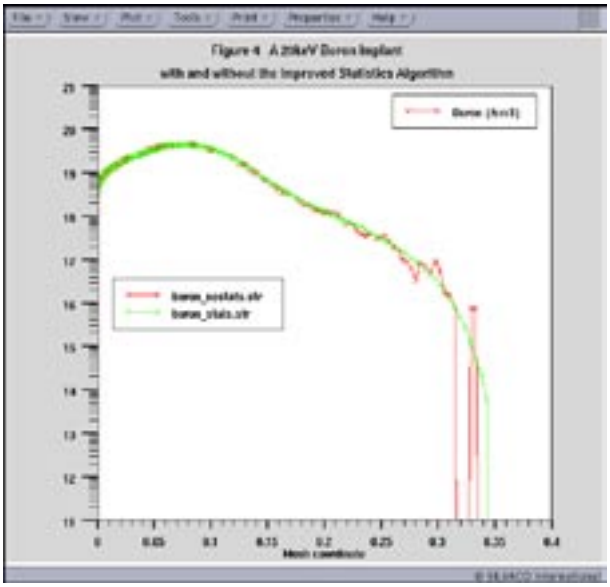

Figure 4. A 20keV Boron Implant at 7 degrees from vertical with and without the new statistical algorithm activated.

3.0 Results and Examples

Typical results showing the improved statistics encountered when using the "sampling" parameter on the Monte-Carlo implant statement are shown in figures 3 and 4. Both figures show typical implant curves with and without the "sampling" parameter activated. The improvements in smoothness at the tail of the implant profiles are clear. All simulations used the same number of ion trajectories. These improvements, therefore, are solely the result of improved statistics using the new algorithm.

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Parasitic Extraction Today: A Comparison Between Classical Full Chip Extraction and Field Solver Extraction

Introduction

With current technologies, parasitic effects must be taken into account in the first phase of IC design development. So, Layout Parasitic Extraction (LPE) is today a very important step before circuit simulation and tape out.

This article will present two different ways to extract parasitics from an IC design: first using a full chip extraction tool ***HIPEX-RC*** based on geometrical information, then using a field solver based extraction tool ***CLEVER***.

The ***HIPEX-RC*** and ***CLEVER*** core features will be detailed in the first part. We will then use these two different tools to characterize inverters and see the consequences on parasitics extraction accuracy.

The goal of this article is not to give exhaustive information about the software but to highlight the differences in regards to capacitance extraction.

LPE Based on Geometrical Information: *HIPEX-RC*

HIPEX is based on a geometrical engine to detect and extract parasitic capacitance and resistance. It is able to extract three groups of capacitance described below :

- *The Overlap Capacitance:* It is detected when two different layers overlap. The Capacitance between the two plates is extracted

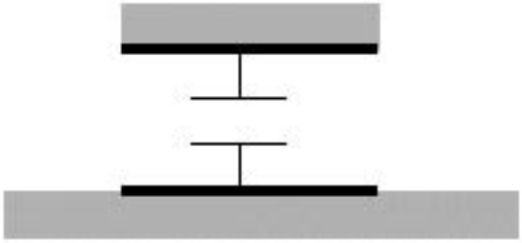

Figure 1. Overlap Capacitance.

- *The Lateral Capacitance:* It is detected when two identical layers are in the same level. The capacitance between the 2 edges is extracted

Figure 2. Lateral Capacitance.

- *The Fringe Capacitance:* It is detected when two different layers overlap (like Overlap Capacitance). The Capacitance between the edge of first layer and the plate is extracted

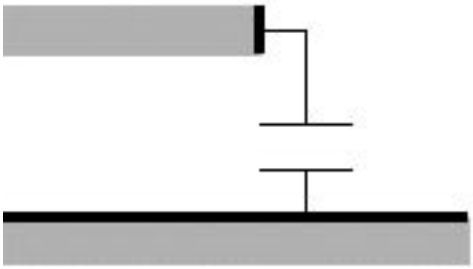

Figure 3. Fringe Capacitance

We can note that two events lead to a capacitance extraction in ***HIPEX-RC***:

- Overlap of different layers (overlap and fringe capacitance in Figure 1 and 3)
- Face to face of two identical layers (lateral capacitance in Figure 2)

The capacitances are extracted only if the two layers involved are inside a vicinity zone. It means that if the distance between the two layers is outside the vicinity zone, the capacitance will not be extracted.

Once a capacitance is detected the geometrical engine will take into account the environment as it may influence the value extracted.

See Figure 4 with an example of an overlap capacitance defined between the two black layers. The perturbations involved by the shading layers are represented in gray.

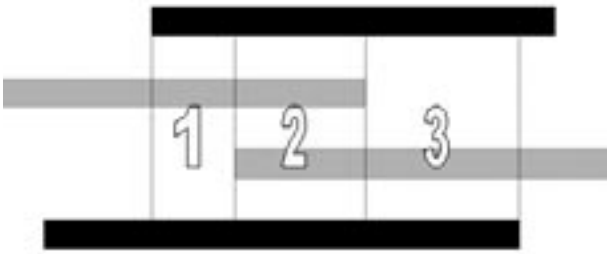

Figure 4. Overlap capacitance: 3 different zones

HIPEX-RC detects three different zones (zone 1,2 and detects three different zones (zone 1,2 and 3 from Figure 4) where different geometrical parameters will be extracted.

Indeed, ***HIPEX-RC*** returns all the geometrical parameters from the structure: area overlap, perimeter, distance between 2 layers... Then three different strategies can be used:

- Let ***HIPEX-RC*** apply its built-in formula
- Create a user-defined formula as a function of these geometrical parameters
- Create a Table look-up model

With this method, ***HIPEX-RC*** is able to treat large full chips with a minimum of CPU time.

LPE Based on Field Solver: *CLEVER*

CLEVER is designed to model interconnect parasitics by simulating the back end processing steps of custom cells in three dimensions.

A 3D-process simulator is used to reproduce the topography realistically (Figure 5).

The process steps are driven from existing masks in standard GDSII data format from the current design. The 3D grid re-meshing required for each of the steps is generated totally automatically and requires no user input (Figure 6).

Finally a 3D-field solver is used to calculate capacitances and resistances (Figure 7).

This approach is well known to be the most accurate when compared to measurements [2] as there is no more capacitance detection based on pattern. So they all will be extracted with their real environment and perturbation.

But this way of working based on high computing method leads to longer simulation and restricted layout size.

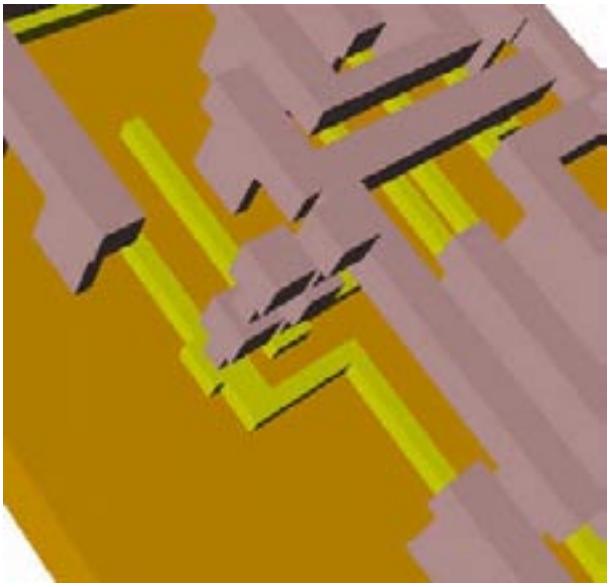

Figure 5. 3D structure.

CASE STUDY: A Simple Inverter

Significant difference on capacitance extraction may be noticed on simple design between results coming from ***HIPEX-RC*** and ***CLEVER***. The comparison will be based on two measured targets:

- The delay from the inverter (propagation time between IN and OUT)
- The capacitances between the nodes IN, OUT and Ground

First consider the following inverter (Figure 8).

Using the extracted parasitic netlist back annotated onto the netlist allows a SPICE simulator to measure the delay between IN and OUT. Similar results are obtained Table 1).

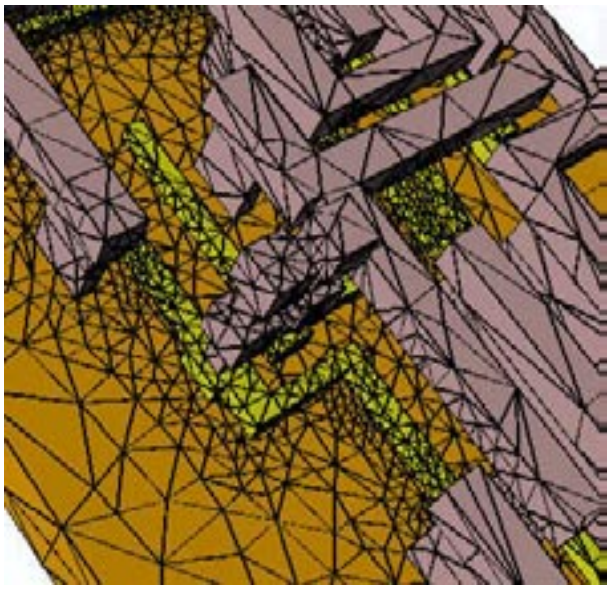

Figure 6. 3D structure Mesh.

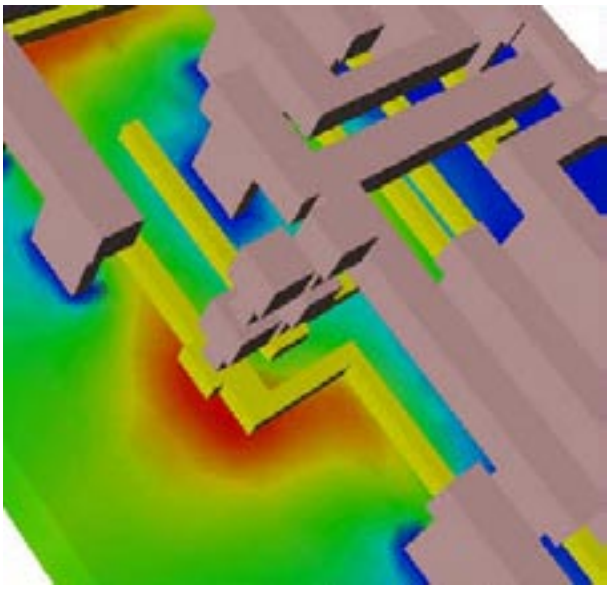

Figure 7. Potential calculated from Laplace's equation.

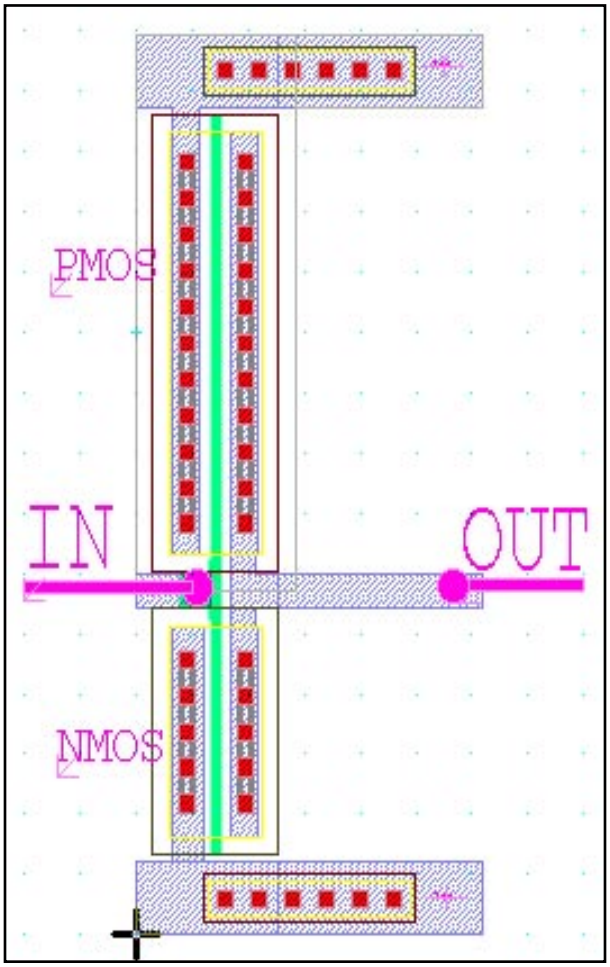

Figure 8. Inverter_1.

	HIPEX	CLEVER
Delay in/out (ns)	44	45

Table 1: Simulation result with inverter_1.

Consider now the following design with another inverter. Input and output signals are now interlaced. See Figure 9 and 10 for the plan and 3D view.

The simulated delay with parasitics are now shown in Table 2. ***CLEVER*** gives different results as compared to ***HIPEX-RC.***

	HIPEX	CLEVER
Delay in/out (ns)	52	59
Cout_gnd (FF)	3.2	1.5
Cin_gnd (FF)	7.0	6.5
Cin_out (FF)	0.06	3.5

Table 2. Simulation/extraction result with inverter_1.

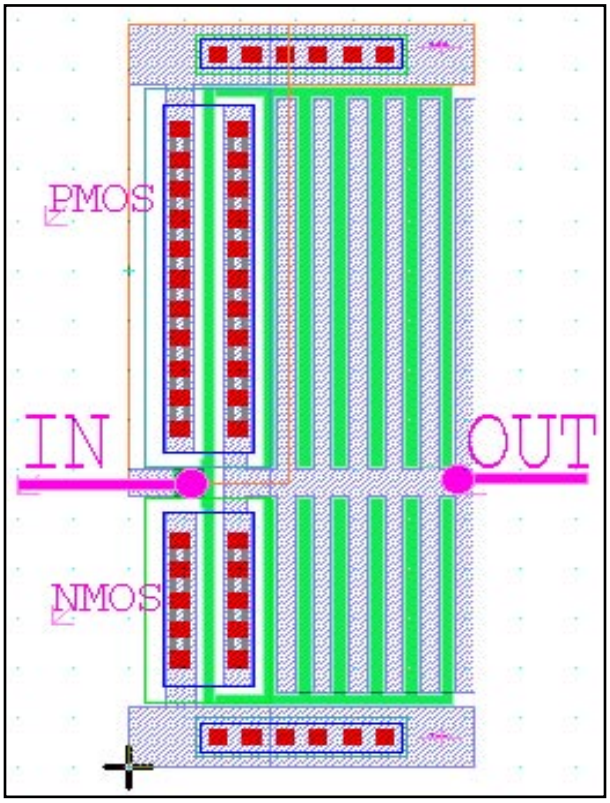

Figure 9. Inverter_2 with interlaced input and output.

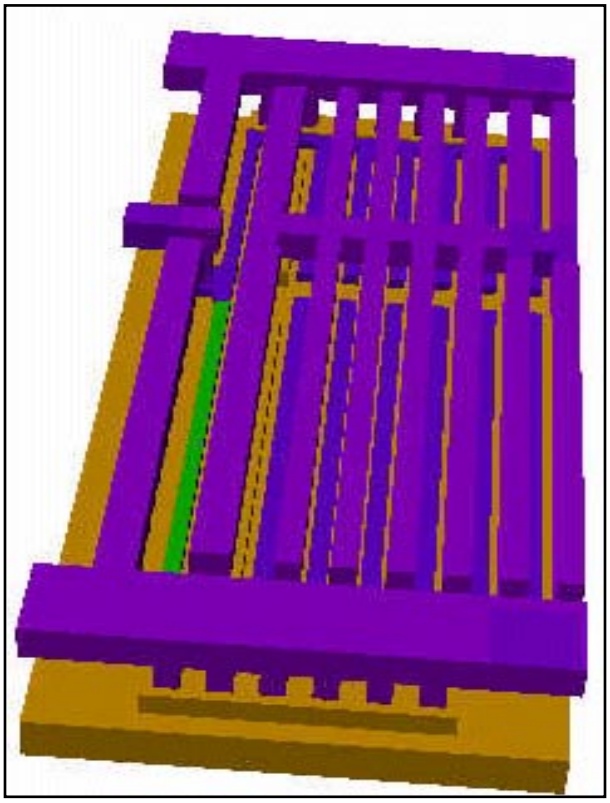
Figure 10. 3D View of the inverter_2.

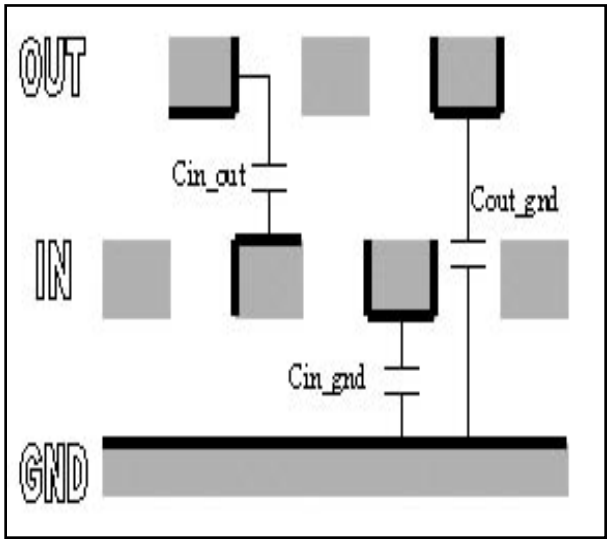

Figure 11. IN and OUT interlaced (inverter_2).

If we refer to Table 2 we can give two explanations. They will be based on the vertical cut view below which shows more in detail the input and output signals interlaced (Figure 11).

First, the Cout_gnd capacitance is higher with the ***HIPEX-RC*** extraction than with the ***CLEVER*** one. As previously explained the field solver extraction takes into account all the perturbation generated by other conductors. In this situation, the IN signal acts as a perturbation between the OUT and GND conductors. ***HIPEX-RC*** is not able to detect it because there is no overlap between the OUT and IN signals. ***HIPEX-RC*** analyses the capacitance between OUT and GND as if the layout looks like the one shown in Figure 12.

As a result the Cout_gnd capacitance is overestimated by ***HIPEX-RC*** mainly due the two fringe capacitances.

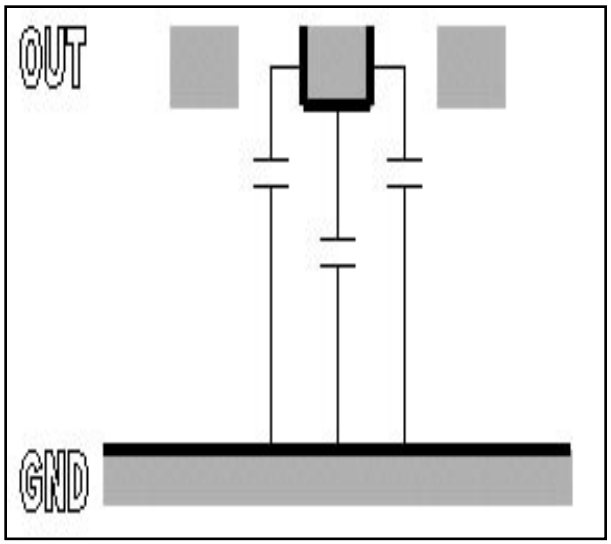

Figure 12. GND and OUT seen by HIPEX-RC.

However it doesn't explain why the parasitic netlist extracted by ***HIPEX-RC*** gives a delay smaller as compared to ***CLEVER***. Another phenomena with a higher influence than the previous one will clarify the situation.

We can note an important difference between the Cin_out capacitance extracted from ***HIPEX-RC*** and ***CLEVER***. In the area represented in Figure 11, there is no overlap between IN and OUT signals and there are on different level (IN is in Poly and OUT in Metal1). If we refer to what was written about capacitance detection with ***HIPEX-RC***, nothing will be detected in this area. This explains why the capacitance between IN and OUT is so low (a small overlap is present in another part not represented in the cut view from the Figure 11). This underestimation leads to a delay slightly shorter with ***HIPEX-RC***.

Conclusion

From an accuracy point of view, only a field solver can give good results independently of the layout used. But another criterion must be taken into account: the extraction time. On a structure similar to the previous one repeated thirty-one times to obtain a ring oscillator, the extraction time can vary from one minute with ***HIPEX-RC*** to thirty minutes with a field solver like ***CLEVER***.

This article, based on a concrete example, shows that parasitic extraction can be done in several ways. Each method should be used according to the size of the layout, the accuracy level expected and the inputs we have.

However the perspective is to mix these two methods instead of choosing between them.

References

[1] Silvaco,"HIPEX-Hierarchical Layout Parameter and Parasitic Extractor", Simulation Standard, March 2003, http://www.silvaco.com/applications/archive/2003/mar2003/mar03_a1/mar03_a1.html.

[2] B. FROMENT, et al., "New interconnect characterization method for multilevel metal CMOS processes", ITTC may 1999. 12. GND and OUT seen by HIPEX-RC.

Calendar of Events

May

1	
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11	
12	IPRM - Santa Barbara, CA
13	IPRM - Santa Barbara, CA
14	IPRM - Santa Barbara, CA
15	IPRM - Santa Barbara, CA
16	IPRM - Santa Barbara, CA
17	
18	
19	GaAs MANTECH Scottsdale, AZ
20	GaAs MANTECH Scottsdale, AZ
21	GaAs MANTECH Scottsdale, AZ
22	GaAs MANTECH Scottsdale, AZ
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June

1	
2	DAC - Anahiem, CA IITC - San Francisco, CA
3	DAC - Anahiem, CA IITC - San Francisco, CA CLEO - Baltimore, MD
4	DAC - Anahiem, CA IITC - San Francisco, CA CLEO - Baltimore, MD
5	DAC - Anahiem, CA CLEO - Baltimore, MD
6	DAC - Anahiem, CA
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10	VLSI Symposium - Japan
11	VLSI Symposium - Japan
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19	WOLTE-5 - France
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Bulletin Board

Silvaco Gets Royal Treatment in Cambridge

Silvaco hosted His Royal Highness The Duke of York for the dedication of Silvaco's Cambridge Technology Center. Located in the heart of the UK technology corridor close to several prestigious universities, this 28,000-sq.ft R&D facility accommodates the existing Silvaco UK development team with room for an additional one hundred software and electrical engineering professionals.

(Left to right) HRH the Duke of York, Felix Rayner, MD of Silvaco UK, Ivan Pesic, Founder and CEO of Silvaco International, and Mrs Katherine Pesic

This site was selected to tap the highly educated physicists, electrical engineers, mathematicians, and software developers from this university area. The center will be used to advance the R&D muscle of Silvaco in the areas of TCAD, circuit simulation, and custom IC CAD.

If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

William French Ph.D., Applications and Support Manager

Q: Can *ATLAS* simulate an SEU event in 2D? To simulate a single event upset (SEU) is inherently a 3D problem because the alpha particle may strike the chip at any arbitrary angle to the chip surface. Silvaco's 3D device simulator Device3D incorporates sophisticated algorithms to model this process accurately. However, it is possible to do this simulation in 2D with *ATLAS* but it should be remembered that this is only an approximation.

A: One method within ***ATLAS*** to simulate a particle strike in 2D involves the use of the ***C-Interpreter*** capability of ***ATLAS***. This feature allows the user to write a simple C-coded ascii file that describes the generation rate of carriers (per cc per sec) as a function of location x (microns), location y (microns) and time t (secs). The ***C-Interpreter*** file is specified on the BEAM statement very simply as

```
BEAM F.RADIATE=RADIATE.LIB
```

where the file RADIATE.LIB contains the C-code.

To illustrate this with a simple example the MOSFET structure of Figure 1 was first generated. An alpha particle strike through the drain region, at 90 degrees to the surface, was modelled with the following C-interpreter model:

```
int radiate(double x,double y,double
t,double *rat)
   {
       double GEN;
       GEN = 1e20;
       if ((x>2.3) && (x<2.35)) {
          if ( (t >= 20e-12) && (t<=40e-12) )
{
              *rat = GEN;
       }
           }
           else {
           *rat = 0;
           }
       return(0);
       /* 0 - ok */
}
```

This defines that the strike occurs between t=20 ps and t=40 ps and the generation rate is a simple delta function between 0 and GEN cm-3 s-1. The strike is limited between x=2.3um and 2.35um and travels from the top of the structure to the bottom.

The ***ATLAS*** syntax to define the transient is quite simpleand in this example is :

```
SOLVE B1=1 TFINAL=1E-6 DT=1E-12
```

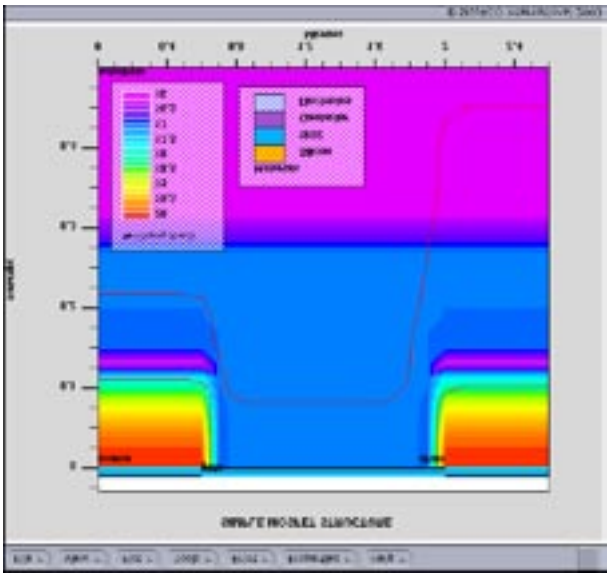

Figure 1. Simple 2D MOSFET structure for the alpha particle strike simulation. The drain bias is 3.3V so the depletion regions extend into the bulk as shown.

It should be noted that the GEN parameter in the C-code is multiplied by the value of the B1 parameter on the SOLVE statement.

Figure 2 shows the resultant drain current versus time plot of this strike for B1=1, 1e2 and 1e5. The gate is initially off and the drain voltage is at 3.3V. The familiar SEU current pulse profiles are obtained.

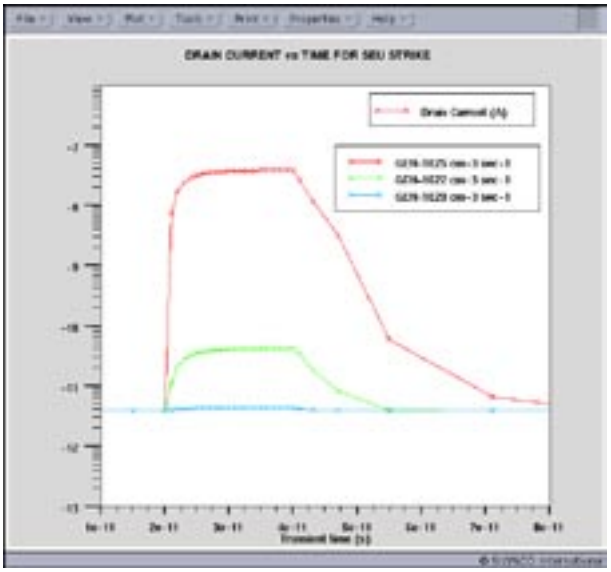

Figure 2. Simulated drain curent versus time for 3 separate particle strikes. The generation rate (or particle energy) was varied as shown.

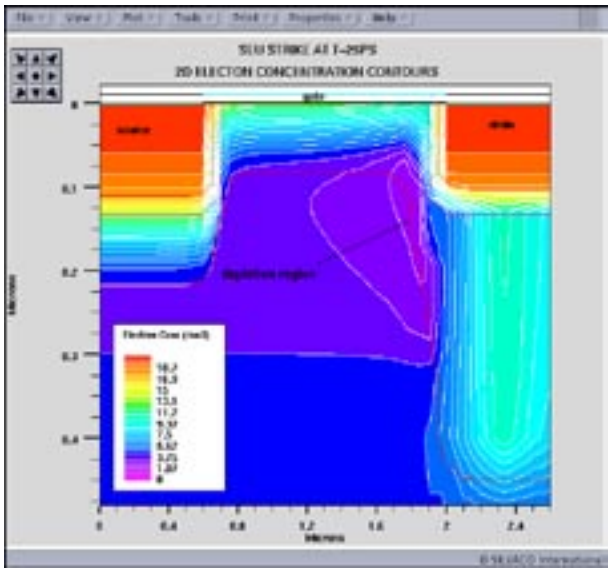

Figure 3. 2D Contours of electron concentration during the particle strike.

Figure 3 shows a plot of the electron concentration at time t=25 ps. The generated electrons are observed below the drain contact. As the generation occurs within the shown depletion region, the carriers are swept very quickly to the source and drain.

References

1. *ATLAS User's Manual.*

Call for Questions

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e-mail: support@silvaco.com

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...continued from page 3

To compare on resistance, the curve for the conventional device from Figure 4 was used to determine the R*AA value at the achieved breakdown voltage of 94 V. This was compared with measured values for the prototype devices. The results can be seen in Table 1, indicating a 19% reduction in on resistance compared to conventional planar devices.

Device	BV (V)	R*AA (mohm-mm^2)	R*AA at 94 V	R*AA Improvement
Current Planar	79.5	101	136	
3e12.1.5 MeV	93.9	111	111	19%

Table 1. Comparison of Prototype Device

All other prototype device parametric values were comparable to conventional devices of the same voltage. The fact that drain to source leakage was not increased indicates that the low dose, high energy implant did not introduce significant damage, or that this damage was annealed out during processing.

These prototypes were subjected to the standard set of reliability tests, including High Temperature Gate Bias at 20Vgs / 175 C, and High Temperature Reverse Bias at 70Vds / 175 C. No failures were observed.

Conclusion

Simulations and experimental results for a new planar MOSFET device containing an extended p-body formed through high energy ion implantation have been presented. Simulations suggest a reduction in R*AA of 35%. Prototype devices exhibit a 19% reduction in on-resistance per unit area. Further improvement is expected

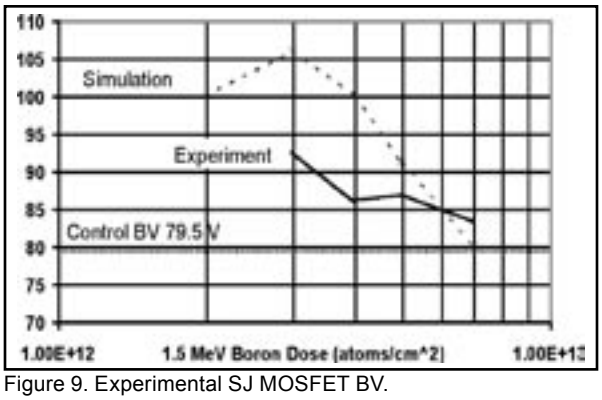

Figure 9. Experimental SJ MOSFET BV.

through improved termination design and process. An optimization of this device would combine a substantial gain in performance with minimal processing changes from conventional devices.

Acknowledgements

The authors would like to thank Kyle Spring, Jonathan Stout, Vijay Viswanathan and Phil Parsonage for technical discussions and process assistance.

References

[1] X. Chen, U. S. Patent 5216275, 1993.

[2] P. M. Shenoy, A. Bhalla, and G. M. Dolny, "Analysis of the Effect of Charge Imbalance on the Static and Dynamic Characteristics of the Super Junction MOSFET", *Proc. Of the ISPSD*, pp.99-102, May, 1999.

[3] J. Tihanyi, U. S. Patent 5438215, 1995.

SILVACO INTERNATIONAL

USA Headquarters:

Silvaco International
4701 Patrick Henry Drive, Bldg. 2
Santa Clara, CA 95054 USA

Phone: 408-567-1000
Fax: 408-496-6080

sales@silvaco.com
www.silvaco.com

Contacts:

Silvaco Japan
jpsales@silvaco.com

Silvaco Korea
krsales@silvaco.com

Silvaco Taiwan
twsales@silvaco.com

Silvaco Singapore
sgsales@silvaco.com

Silvaco UK
uksales@silvaco.com

Silvaco France
frsales@silvaco.com

Silvaco Germany
desales@silvaco.com

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