

# Simulation Standard

Connecting TCAD To Tapeout

A Journal for Process and Device Engineers

## Low Voltage Super Junction MOSFET Simulation and Experimentation

Timothy Henson, Joe Cao

International Rectifier, 233 Kansas St, El Segundo, CA 90245 USA, Phone +01 310 726 8842, Fax +01 310 726 8847 E-mail: thenson1@irf.com

### Abstract

The application of Super Junction concepts to a low voltage power MOSFET is investigated. The body junction is modified with the addition of a high energy implant, resulting in an increased breakdown voltage. Simulations are used to quantify the relationship between dose and breakdown voltage, resulting in a predicted 35%  $R_{ds(on)}$  reduction. This is confirmed through experiment, and a 19% reduction in  $R_{ds(on)}$  is reported at 75 V. No change in device reliability is observed. This approach provides a simple means to reduce the on resistance of low voltage MOSFETs.

### Introduction

High Voltage (600V) power semiconductors using super junctions to achieve greatly reduced on-resistance have been reported for several years<sup>[1-3]</sup>. The drift region of such devices is comprised of alternating N<sup>-</sup> and P<sup>-</sup> type regions of equal charge. In the blocking mode, the adjacent N<sup>-</sup> and P<sup>-</sup> regions deplete into each other laterally. The drift region thus comprises several N<sup>-</sup> and P<sup>-</sup> regions in parallel, with the N<sup>-</sup> regions having much lower resistivity than conventional devices, and therefore presents a lower  $R_{ds}$ . These high voltage devices are complicated to manufacture with multiple cycles of epitaxial growth, photo mask, implantation, and drive steps, or very deep trenches.

This paper presents a simple implementation of the super junction concept, utilizing a high energy Boron implant, into low voltage (50-100V) planar n-channel MOSFETS. Through the addition of a high energy implant (1-3 MeV) to form a lightly doped P<sup>-</sup> diffusion underneath the standard p-type body diffusion, alternating N<sup>-</sup> (EPI) and P<sup>-</sup> regions are formed.

### Device Structures and Simulations

Process and device simulations were performed to evaluate the proposed structure. An existing model for a state of the art self-aligned contact planar MOSFET with  $BV \sim 75V$

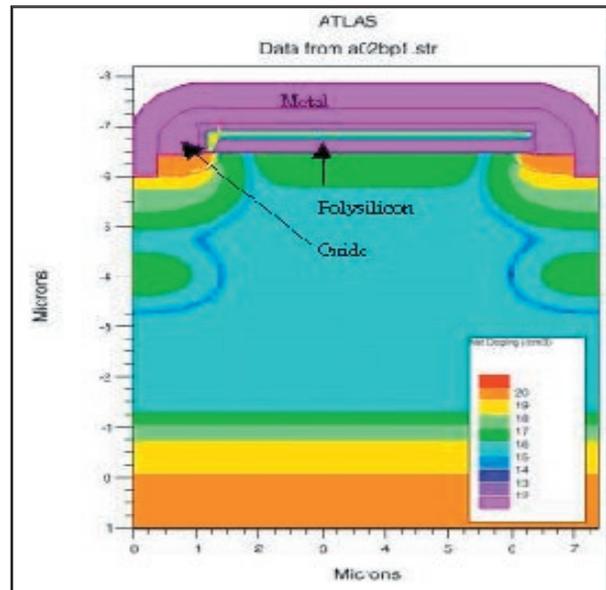


Figure 1. Simulated device with 1.5 MeV High Energy Implant.

was modified to include a high energy implant after the poly etch sequence. The simulated high energy implant is blocked from penetrating the polysilicon gate. Figure 1 shows the net doping of a device that included a  $3.0E12$ , 1.5 MeV Boron implant.

Continued on page 2 ...

### INSIDE

Using The Statistical Sampling Feature in Silvaco's BCA Monte Carlo Implant Simulator .....	4
Parasitic Extraction Today .....	7
Calendar of Events .....	11
Hints, Tips, and Solutions .....	12

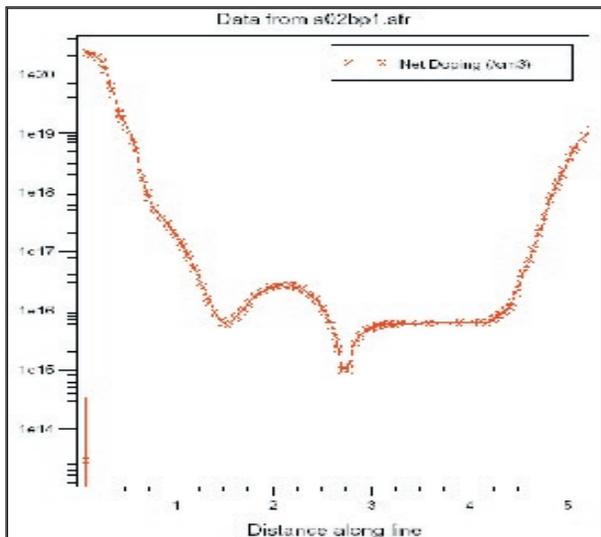


Figure 2. Cutline through Figure 1.

The high energy implant can be seen extending beneath the p-body by about 1 um. High energy implanters are available with energies up to about 3 MeV for Boron, which gives a mean depth in silicon of 3.7 um.

In a traditional super junction, the N<sup>-</sup> and P<sup>-</sup> type regions are assumed to deplete in the horizontal direction, and thus the N<sup>-</sup> and P<sup>-</sup> concentrations are equal to achieve charge balance. Because of the limitation in depth from the high energy implanter, the P<sup>-</sup> type regions in this case will deplete in both the horizontal and vertical directions. For this reason, the optimum P<sup>-</sup> type doping is higher than the N<sup>-</sup> type (j-fet and drift region) doping. This can be seen in Figure 2, where the net doping is plotted for a cutline taken through the right edge of the structure in Figure 1.

For conventional MOSFETs of this design, the location of breakdown is typically in the j-fet region at the corner of the body junction. With the addition of the high energy implant, the location of breakdown moves to the region of the deep implant. This is illustrated in Figure 3, showing a simulation of impact ionization for the device of Figure 1. 'H' indicates breakdown (dark colored region) in this simulation with the high energy implant, and 'C' indicates where a conventional device would breakdown.

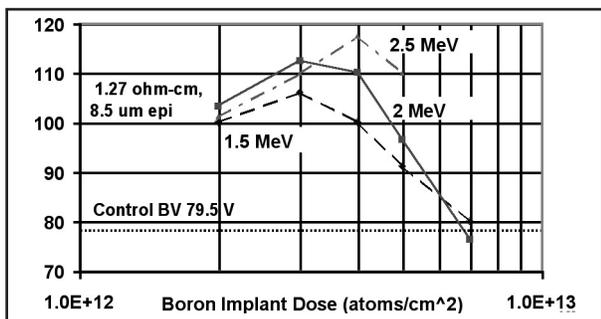


Figure 4. Simulated Breakdown Voltage with various high energy Boron implants.

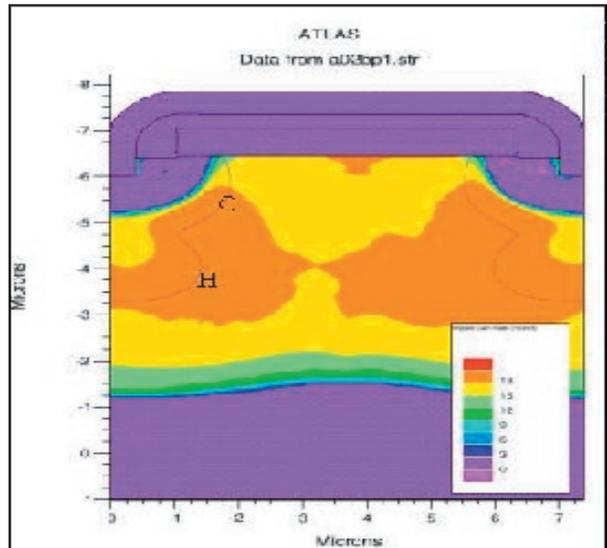


Figure 3. Location of breakdown.

The simulations indicate that, for a given implant energy, the device breakdown voltage increases as implant dose is increased up to a certain value. As the implant dose is further increased, breakdown voltage reduces. This can be seen in Figure 4, where simulated breakdown voltage is plotted for implant energies of 1.5, 2.0, and 2.5 MeV.

These simulations predict a maximum breakdown voltage increase of 32% for the 1.5 MeV implant and 45% for the 2.5 MeV implant. Higher energies create a deeper alternating N<sup>-</sup> and P<sup>-</sup> type column structure, and support more voltage in this region.

Deeper N<sup>-</sup> and P<sup>-</sup> type regions also create a longer effective j-fet, and constrict the current flow in this region, leading to increased on resistance. Based on the 6.6 um cell pitch used on the conventional device, an implant energy of 1.5 MeV is expected to provide a good tradeoff between BV and on resistance. Simulations were run to determine the optimum implant doses at 1.5 MeV for various voltages, based on different starting N<sup>-</sup> epitaxial layers. Figure 5 shows simulated results for the on-resistance \* Active Area (R\*AA) figure of merit typically used to characterize power MOSFETs.

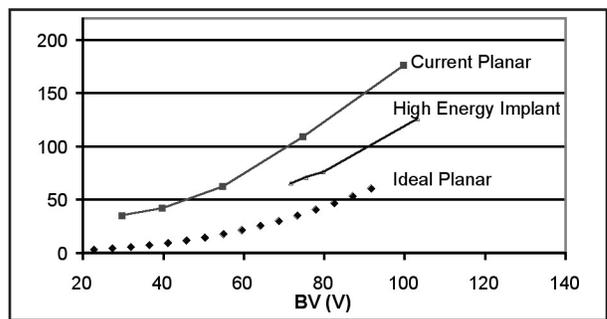


Figure 5. R\*AA product for SJ MOSFET based on simulations.

The high energy implant device shows a 35% reduction in  $R^2AA$  compared to the conventional MOSFET, at a breakdown voltage of 75 V. Also shown is the case of an ideal planar (1-sided) junction. It should be noted that the 'ideal planar' values do not include any contribution from channel and contact resistances that are included in the current planar devices and the high energy implant simulations.

## Experimental Results

This high energy implant super junction concept was applied to a state-of-art self-aligned-contact planar MOSFET. The chosen device had a poly line width of 5  $\mu\text{m}$ , and a pitch of 6.6  $\mu\text{m}$ . The Epi thickness was 8.5  $\mu\text{m}$ , with a resistivity of 1.27  $\text{ohm-cm}$  to give a nominal BV of 79.5 V. The process flow was identical to the standard FET, except that thicker (3.5  $\mu\text{m}$ ) photoresist was used for the poly mask. This was necessary to block the high energy implant from the j-fet region. The structure at the high energy implant step is shown in Figure 6.

After the polysilicon gate has been etched, the standard channel implant is replaced by two implants. The first is the typical high dose, low energy channel implant (1.0E14, 80 KeV), and the second is the high energy low dose implant to form the deep P type region. Based upon the simulation results, a range of high implant energies (1.5 to 2.5 MeV) and doses (2.0E12 – 7.0E12) was performed.

The rest of the self-aligned contact sequence is left unchanged. This consists of removing the photoresist and performing the channel drive. The source is implanted and driven, as is the shallow p+ region. Then an oxide is deposited and etched back to form oxide spacers on the sides of the poly gates. Finally, the contact etch into the silicon is performed.

For comparison, a SEM of a conventional device with the junctions stained is shown in Figure 7, and a prototype device with the 1.5 MeV implant is shown in Figure 8.

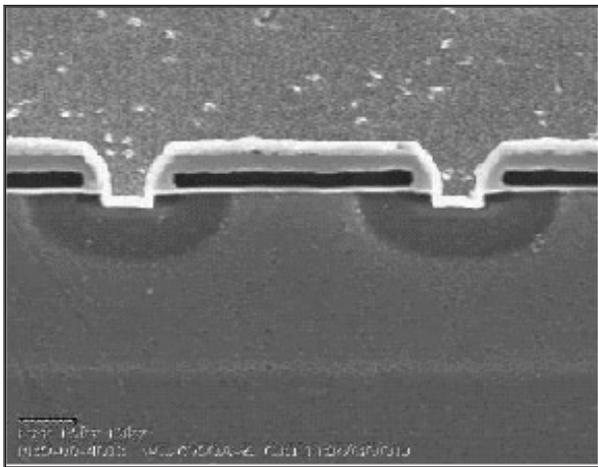


Figure 7. SEM of conventional device.

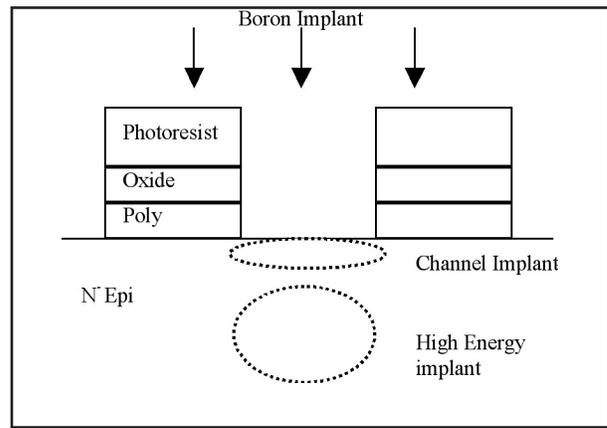


Figure 6. Schematic of structure at high energy implant.

The P diffusion, formed in this case by a 1.5 MeV Boron implant, can be clearly seen below the standard body junction.

The high energy implant was activated at the same time as the channel implant. No additional diffusion was desired or necessary because the implant straggle is already quite large (1840  $\text{\AA}$  longitudinal, 2360 lateral at 1.5 MeV). Additional lateral diffusion would increase on resistance by narrowing the conduction (j-fet) region.

Functioning prototype devices were created and tested to compare with simulated values. Experiments follow a similar trend with dose as the simulations, showing an increase in breakdown voltage with the addition of the high energy implant, and then a reduction in maximum BV as the implant dose is increased. These results can be seen in Figure 9.

The maximum voltage predicted by simulations was not achieved, as the prototype device breakdown voltage is limited by the termination. The achieved breakdown voltage represents a 18% increase in BV, compared to the simulated 32%.

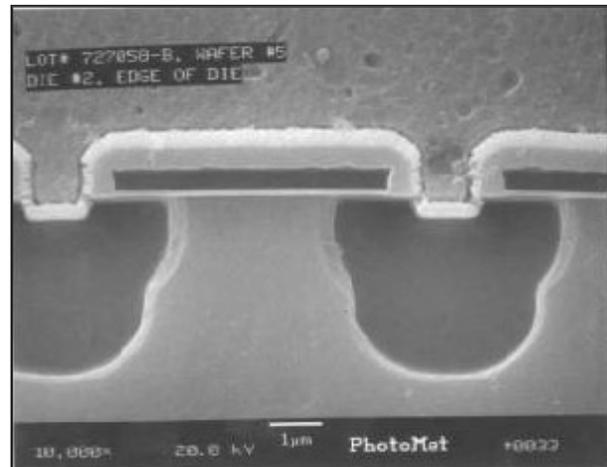


Figure 8. SEM of prototype device with 1.5 MeV Boron Implant.

To compare on resistance, the curve for the conventional device from Figure 4 was used to determine the R\*AA value at the achieved breakdown voltage of 94 V. This was compared with measured values for the prototype devices. The results can be seen in Table 1, indicating a 19% reduction in on resistance compared to conventional planar devices.

Device	BV (V)	R*AA (mohm-mm <sup>2</sup> )	R*AA at 94 V	R*AA Improvement
Current Planar	79.5	101	136	
3e12.1.5 MeV	93.9	111	111	19%

Table 1. Comparison of Prototype Device

All other prototype device parametric values were comparable to conventional devices of the same voltage. The fact that drain to source leakage was not increased indicates that the low dose, high energy implant did not introduce significant damage, or that this damage was annealed out during processing.

These prototypes were subjected to the standard set of reliability tests, including High Temperature Gate Bias at 20Vgs / 175 C, and High Temperature Reverse Bias at 70Vds / 175 C. No failures were observed.

## Conclusion

Simulations and experimental results for a new planar MOSFET device containing an extended p-body formed through high energy ion implantation have been presented. Simulations suggest a reduction in R\*AA of 35%. Prototype devices exhibit a 19% reduction in on-resistance per unit area. Further improvement is expected through improved termination design and process. An optimization of this device would combine a substantial gain in performance with minimal processing changes from conventional devices.

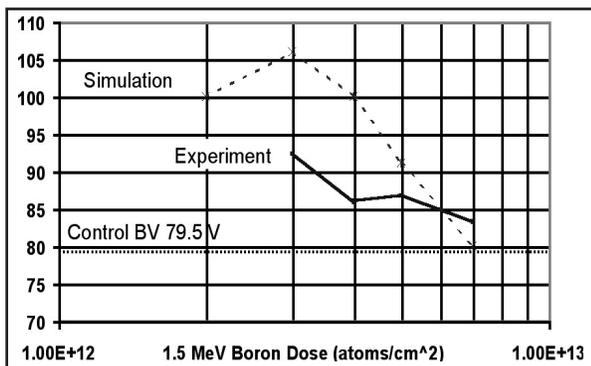


Figure 9. Experimental SJ MOSFET BV.

## Acknowledgements

The authors would like to thank Kyle Spring, Jonathan Stout, Vijay Viswanathan and Phil Parsonage for technical discussions and process assistance.

## References

- [1] X. Chen, U. S. Patent 5216275, 1993.
- [2] P. M. Shenoy, A. Bhalla, and G. M. Dolny, "Analysis of the Effect of Charge Imbalance on the Static and Dynamic Characteristics of the Super Junction MOSFET", *Proc. Of the ISPSD*, pp.99-102, May, 1999.
- [3] J. Tihanyi, U. S. Patent 5438215, 1995.