Complex Parallel-Series Reduction

1. Introduction

Silvaco's ***Guardian LVS*** tool compares two circuits that are defined by their netlists. The comparison is based strictly on the topological structure of these circuits. Topologically equivalent netlists are considered different, even if they are functionally equivalent. There are several techniques available for designing the same functionality by means of topologically different netlists. While it is impossible for the LVS tool to "know" about all these techniques, many are supported.

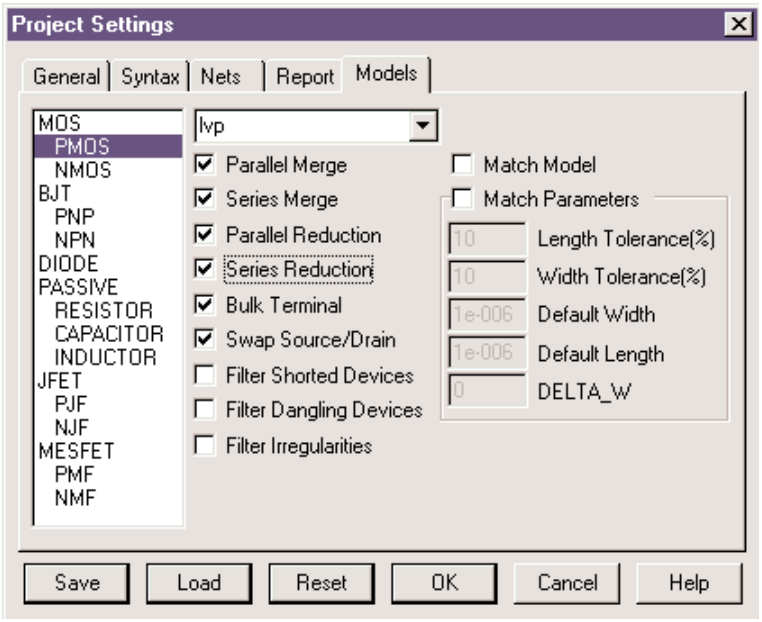

Figure 1. Model Settings Panel.

2. Reduction Varieties

A general method of ignoring strict topological equivalence during the layout design phase is the disregarding of the order of series-connected transistors in the reduction phase. **Series Reduction** is a process of reducing series-connected, same-type transistors that feature different gate terminals. In order for LVS to properly handle this process, a special "pseudo-node" device is introduced into the netlist graph. This pseudo-node represents the series of transistors as a single node. The resulting logical configuration is called a **cluster**. Users choose to recognize or disregard series transistor order by checking the box next to "Series Reduction" in the Model Settings Panel (Figure 1). The option is set independently for each device type and model.

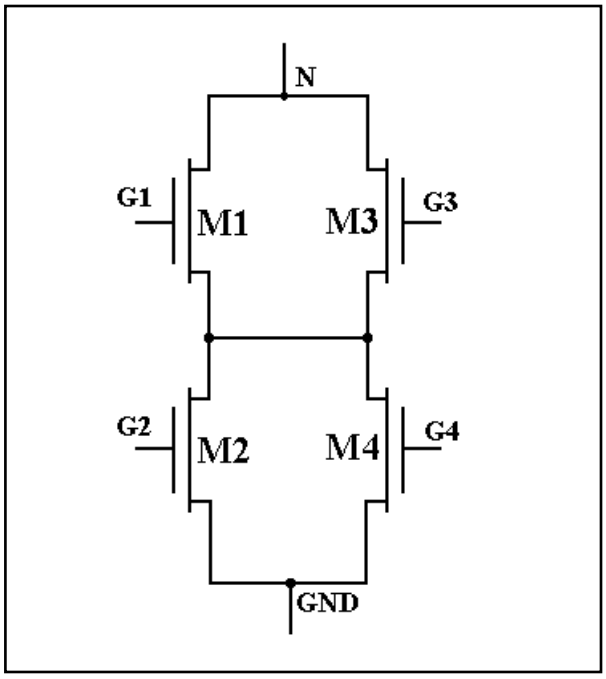

Figure 2. Series-parallel network of MOSFET transistors.

Another reduction process in the Guardian LVS tool is called **parallel reduction.** Parallel reduction is used to reduce parallel sets of transistors for later use in a separate series reduction. Parallel reduction also replaces sets of clusters that are connected in parallel and constructed previously from "pseudo-nodes." The logical configuration obtained as a result of parallel reduction is also called a cluster. Users choose to recognize or disregard parallel transistor order by checking the box next to "Parallel Reduction" in the Model Settings Panel (Figure 1). The option is set independently for each device type and model.

Since the LVS tool handles sets of parallel transistors without reducing to single "pseudo-node," parallel reduction must be activated in tandem with series reduction. In addition, the series reduction feature is also used to reduce either a series of parallel clusters or a series of both transistors, as well as parallel clusters that are connected in series form to a single cluster.

3. Simple Abstraction Model for Reduction

The section describes a simple reduction-stage abstraction model that helps to illustrate some problems that arise during the process. Figure 2 is an illustration of a

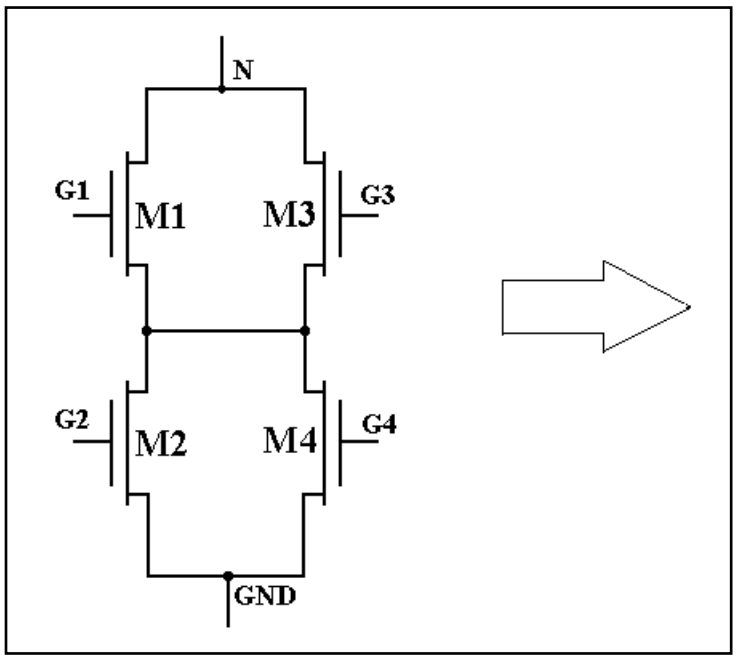

Figure 3. Reduction for series-parallel network using simple abstraction model.

series-parallel network of MOSFET transistors. Transistors **M1** and **M3** and gates **G1** and **G3** are connected in parallel, as are transistors **M2** and **M4** and gates **G2** and **G4**. Transistor pairs **M1-M3** and **M2-M4** are connected in series. There is no way for series reduction to transform this schematic if parallel reduction is not previously executed.

Note: Gates **G1** and **G3** nets should not be identical. Identical gates result in a "transistor parallel merging" pattern. The transistors are merged if the box next to the "Parallel Merge" option of Guardian LVS's Model Settings Panel (see Figure 1) is checked. Necessary merging is automatic if the Series Reduction and Parallel Reduction options are turned on, regardless of the state of the Series Merge or Parallel Merge settings.

How are parallel and series reduction performed? A relatively simple abstraction model for handling different reduction cases is illustrated by Figure 3.

After a combination of parallel and series reductions, the original network is replaced by single cluster with interchangeable **G1**, **G2**, **G3** and **G4** gate terminals. Pseudo-nodes in Figure 3 are indistinguishable from other pseudo-nodes obtained from the network shown in Figure 4, because Figure 4 is also reduced to a single cluster of interchangeable **G1**, **G2**, **G3** and **G4** gate terminals:

It is necessary to improve the abstraction model to distinguish the two previous cases, but to do so is complicated. It is possible that in both netlists in some place we have the configuration from previous figure. Let's assume that net **G1** in Figure 3 is connected to a network with local characteristic **A**. Net **G2** is connected to the network with characteristic **B**, **G3** to network **C**, and **G4** to network **D**. Let's assume also that net **G1** in Figure 4 is connected to the network with characteristic **A**, **G2** to **C, G3** to **B,** and **G4** to **D**. There is no difference between these configurations because in this abstraction model, **G2** and **G3** are not interchangeable.

4. Guardian LVS Abstraction Model for Reduction

The ***Guardian LVS*** matching engine abstraction model accurately reflects conditions of gate terminal interchangeability, and to solve problems like the one found in section 3. For the previous example it is possible to interchange **G1** and **G2**, **G3** and **G4**, as well as pairs **G1-G2** and **G3-G4**. An idea for an abstraction model that met our requirements is illustrated in Figure 5.

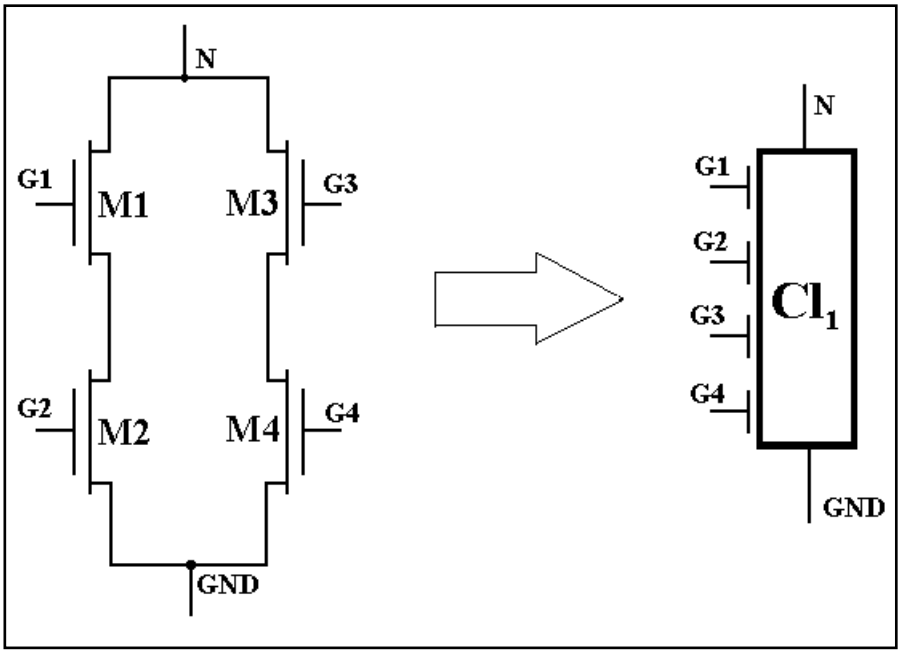

Figure 4. Reduction for parallel-series network using simple abstraction model.

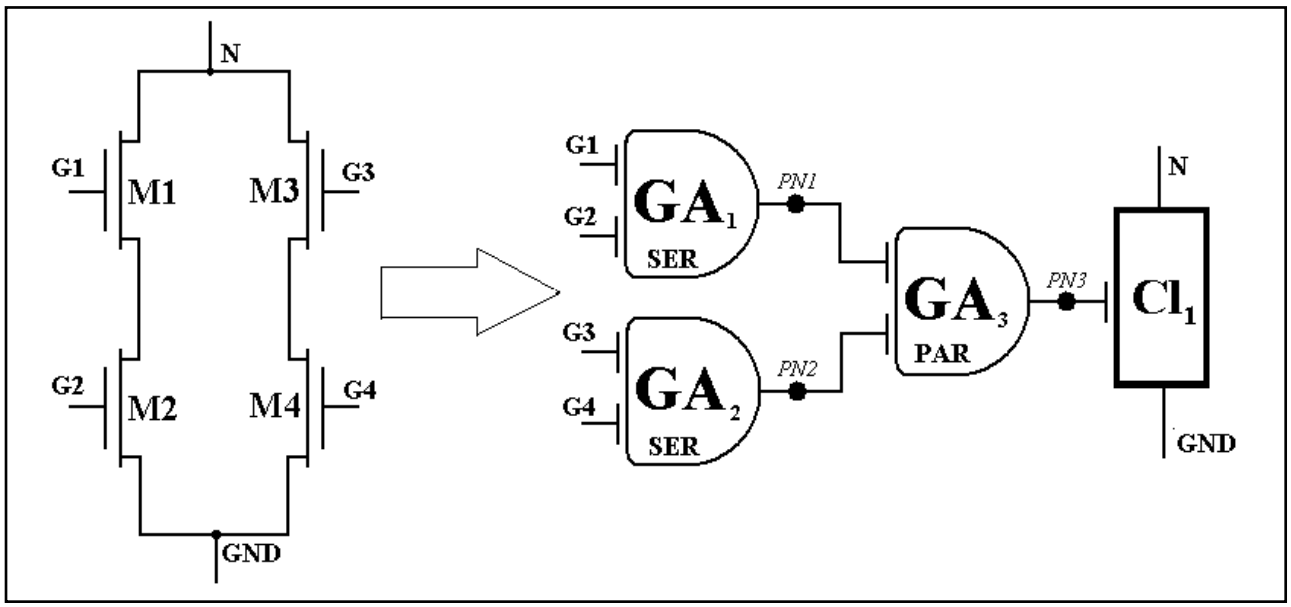

Figure 5. Reduction for parallel-series network realized in Guardian LVS tool.

In this model, several "pseudo-devices" and "pseudo-net" nodes represent the original network. Pseudo-nets are represented as **PN1**, **PN2** and **PN3**. Pseudo-devices are shown as "gate-arrays" **GA1**, **GA2**, **GA3** and cluster **CL1**. Each gate-array represents single interchangeability: **GA1** provides interchangeability of **G1** and **G2**, **GA2** makes **G3** and **G4** interchangeable, and **GA3** makes the pairs **G1-G2** and **G3-G4** interchangeable as well. If the matching engine finds an error in pseudo-node **GA1**, **GA2**, **GA3**, **PN1**, **PN2**, **PN3**, or **CL1**, it is reported to the user in transistor cluster **M1-M4**.

Reduction process for network of Figure 2 can be illustrated in Figure 6.

In Figure 6, cluster **CL1** is the result of a series reduction of "pseudo-devices" that was executed after the parallel reduction of transistor pairs **M1**, **M3** and **M2**, **M4.**

Conclusion

Guardian LVS from Silvaco features several options for both parallel and series transistor reduction. These reductions improve interchangeability and help to reduce many of the problems associated with transistor reduction.

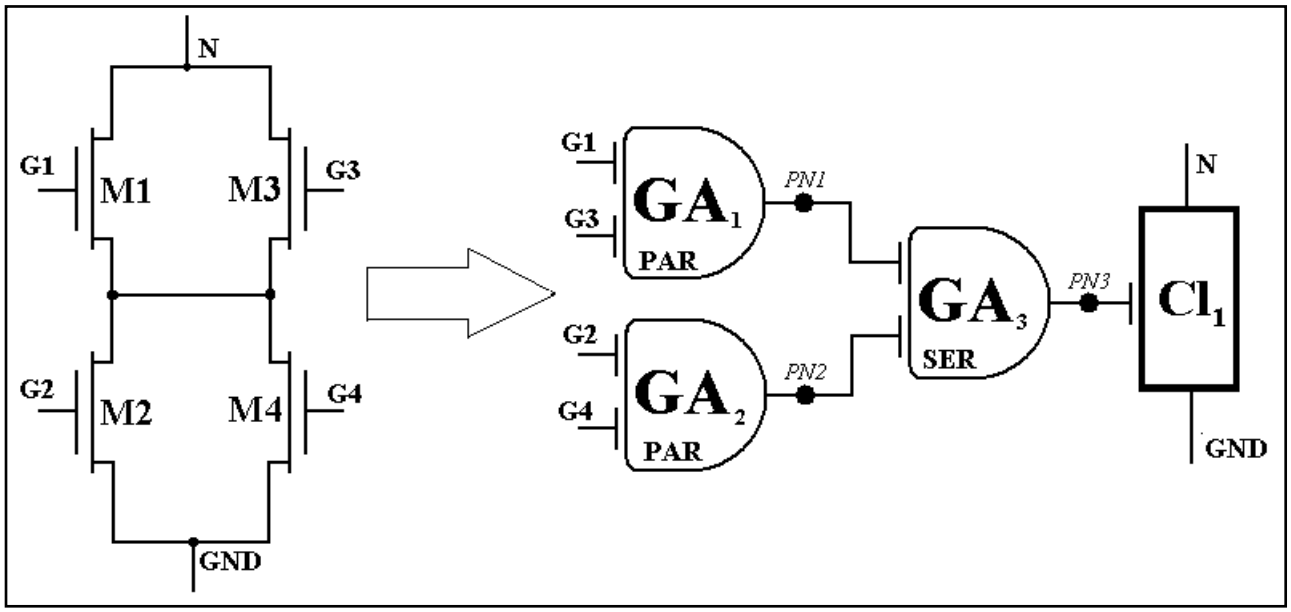

Figure 6. Reduction for series-parallel network realized in Guardian LVS tool.