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HIPEX – Hierarchical Layout Parameter and Parasitic Extractor

Overview

Layout parameter extraction (LPE) and parasitic extraction play important roles in the post-layout verification process. Verification of full chip layout becomes progressively more difficult as the complexity of IC layouts increase, and as new IC technologies are made available. Complex IC design requires the careful consideration of the effects of parasitic capacitors and parasitic resistors or circuit performance. Parasitic devices that are responsible for such effects as time delay, voltage drop, and signal integrity violation, may lead to low chip performance. An accurate estimation of parasitic devices is often a crucial problem in the IC design process.

Silvaco's ***HIPEX*** software suite for multimillion-transistor IC design hierarchical layout parameter and parasitic extraction helps to solve these problems. It consists of several parts that perform fast and accurate netlist and parasitic extraction for full chip design.

The components of the ***HIPEX*** family are:

- ***HIPEX-NET*** – hierarchical netlist extraction and ERC verification tool;
- ***HIPEX-C*** – parasitic capacitance extractor;
- ***HIPEX-R*** – parasitic resistance extractor;
- ***HIPEX-RC*** – parasitic RC network distribution tool;
- ***HIPEX-CRC*** – tool for merge and reduction of parasitic network.
- ***HIPEX Automation Tools***

HIPEX-NET, the hierarchical netlist extractor, makes use of a GDSII or CIF layout file and a user-defined technology file. HIPEX-NET uses back-annotated net names from the schematic netlist to retain the names from the original list. In addition, ***HIPEX-NET*** produces the stripe and hdb databases that are used for further parasitic capacitor and resistor extraction. During parameter extraction, ***HIPEX-NET*** also performs electrical rule checks (ERC).

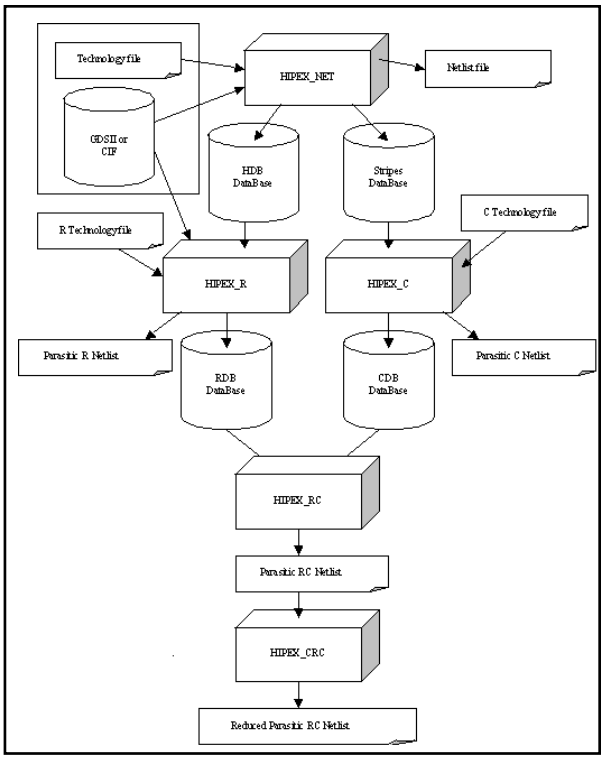

Figure 1. The flow of data in ***HIPEX.***

HIPEX-R and ***HIPEX-C*** extract parasitic resistors and capacitors. Parasitic resistors and capacitors are extracted for whole chips or for selected nets and layers. The ***HIPEX-R*** and ***HIPEX-C*** codes make use of user-defined technology files for generating the parasitic elements.

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The ***HIPEX-RC*** code merges the outputs of these two codes into a distributed RC network. The parasitic netlist is optionally output in either SPICE or DSPF format.

HIPEX-CRC is used to merge and reduce the parasitic network for further simulation by SPICE tools. The merge and reduction dramatically decreases simulation time.

HIPEX Automation Tools convert third party technology files into ***HIPEX*** technology files and execute LPE flow.

The features of ***HIPEX*** are:

- Full chip extraction
- Selected net extraction
- Hierarchical / flat extraction
- Different parasitic extraction models for trade off accuracy versus run time;
- Powerful scripting capabilities
- Integration with industry standards (GDSII, CIF, SPICE, DSPF,…)
- Hierarchical back-annotation
- Efficient network reduction
- Multiprocessing

The flow diagram shown in Figure 1 illustrates how data is managed in ***HIPEX***.

HIPEX-NET – Netlist Extractor

HIPEX-NET features:

- Hierarchical and flattened netlist extraction. Hierarchical netlist extraction reduces processing time and memory usage
- Supported design with cell abutments and overlapping cells without requiring cell pin definition or assigned names
- It is technology-independent, flexible, and driven by a user-technology file. DRACULA / CALIBRE technology files are easily converted to ***HIPEX*** format
- ERC checks extracted netlists for opens, shorts, and dangling nodes
- Hierarchical back-annotation

HIPEX-NET input includes the layout file, technology file, and option file. The layout file is in either GDSII format or CIF format.

The technology file includes device recognition commands, Boolean operations for layer derivation, connectivity commands, text attachment commands, and node generation commands.

The Option file contains files handling options (such as input-output file names and working directories), text handling options (such as net and instance names prefix and separators), and global and local text settings. The file also includes hierarchy manipulation options. Hierarchy manipulation options are set to check hierarchy violations in cells and to explode these cells. The Option file contains ERC options as well. These options control the processing of shorts, opens, and dangles.

HIPEX-NET can output either hierarchical or flattened SPICE netlists. It supports MOSFET, BJT, DIODE, CAPACITOR, and RESISTOR models. Since ***HIPEX-NET*** is the first stage of parasitic capacitor and parasitic resistor extraction, it optionally outputs two databases with geometric and electric node information: a stripe database for ***HIPEX-C*** and a HDB database for ***HIPEX-R***. It is possible to dump selected nets to either a GDSII or CIF file for layout debugging. All ***HIPEX-NET*** messages on extraction and ERC process are output to a summary file.

HIPEX-C – Parasitic Capacitors Extractor

HIPEX-C features:

- Coupling and junction parasitic capacitor extraction for full chip or selected nets
- Overlap, Lateral and Fringe Operators that include 3D effects
- Extraction of various geometrical parameters for user defined capacitor models
- Different parasitic extraction models for a trade-off in accuracy versus run time
- Driven by a user defined technology file
- SPICE capacitor netlist is output

HIPEX-C is a powerful tool for parasitic capacitor extraction. It optionally uses different built-in or user-defined capacitor models. ***HIPEX-C*** extracts three kinds of capacitors:

- OVERLAP
- LATERAL
- FRINGE

An overlap capacitor is formed between nets by overlapping areas of polygons from different layers. A lateral capacitor is formed between parallel edges of two adjacent polygons of the same layer. A fringe capacitor is formed between a polygon edge and a polygon surface of a different layer that lies either above or below this edge.

There are different modes for each kind of capacitor extraction that adjust accuracy and execution time:

- BASIC
- MEDIUM
- HIGH

BASIC is the simplest and fastest mode, using very simple built-in capacitor models. MEDIUM mode permits more complicated built-in capacitor models or user-defined models. In this case several geometrical parameters are extracted and are available for use in a user-defined capacitor model. HIGH mode uses built-in

or user-defined models. The number of extracted geometrical parameters in HIGH mode is greater than in MEDIUM mode.

HIPEX-C input includes a strip database, a technology file, and an setup file.

During layout parameter extraction, ***HIPEX-NET*** divides the input layout to several parallel stripes. Each stripe includes information about the geometrical and electric nodes. This uses very little memory and makes multiprocessing possible.

The technology file contains ***HIPEX-NET*** to ***HIPEX-C*** layer mapping, extraction operators for overlap, fringe, and lateral capacitors, Boolean operations for layer derivation, and layer manipulation operators.

The setup file includes file handling options, such as input-output file names and working directories, as well as output options.

HIPEX-C outputs either standard or detailed SPICE netlists. Spice netlists define parasitic capacitors between nets. Each capacitor value is the sum of the overlap, lateral and fringe capacitors. A detailed spice netlist contains a detailed list of parasitic capacitors between nets. Each overlap, lateral or fringe capacitor is reported to this file separately.

HIPEX-C also outputs a parasitic capacitor database. This binary database contains information about all parasitic capacitors, including related geometrical information. It is used (by ***HIPEX-RC)*** to build a distributed RC net.

HIPEX-R – Parasitic Resistor Extractor

HIPEX-R has the following features:

- Hierarchical Parasitic Resistance Extraction
- Parasitic Resistance for both conducting and contact layers
- Back-annotation of original spice netlist with parasitic network
- Contact over-sizing and clustering
- Models for T, Cross, L, and Bend shapes
- Distributed resistance for long tracks
- Add or Remove Device regions from body resistors (e.g. GATE/POLY)
- Node Filtering

HIPEX-R input includes the layout file, hdb database, technology file, and setup files.

HIPEX-R collects geometrical and electrical node information in two different ways.

The first is by performing LPE in the same manner as ***HIPEX-NET***. In this case ***HIPEX-R*** reads the layout file, which is in either GDSII format or CIF format. The second way is to use the hdb database, which is exclusive to ***HIPEX-NET***.

The technology file contains the device recognition commands, Boolean operations for layer derivation, parasitic conducting layer definitions, parasitic contacts definitions, connectivity definitions, and parasitic node generation commands.

The setup file includes file handling options such as input-output file names and working directories. The file also includes extraction options such as resistor threshold and whether or not to ignore dangles and nodes.

HIPEX-R outputs a hierarchical SPICE netlist with parasitic resistors and subnet names, along with a parasitic resistor database. This binary database is used to build a distributed RC net by HIPEX-RC and contains information on all parasitic resistors, including geometrical information. Statistical information about the extracted parasitic resistors in each cell of the hierarchy is output to the summary file.

Parasitic capacitor and parasitic resistor databases are used by HIPEX-RC code for building distributed parasitic RC nets.

HIPEX-RC - parasitic Network Distribution Tool

HIPEX-RC features:

- Accurate distribution of capacitors over a resistor using spatial coordinates
- PI model support
- Generation of SPICE netlist
- Generation of DSPF netlist

HIPEX-RC uses the ***HIPEX-C*** parasitic database, ***HIPEX-R*** parasitic database, and setup files as input.

HIPEX-RC outputs the distributed RC network in DSPF file format for input into other timing calculation tools.

HIPEX-CRC - Network Reduction Tool

HIPEX-RC features:

- RC circuit handling with loops
- Network reduction in linear time
- The same accuracy as SPICE tools

HIPEX-RC uses the netlist in SPICE/DSPF/SPEF formats and a setup file as input. ***HIPEX-RC*** optionally converts netlists from DSPF to SPEF format.

Conclusion

The ***HIPEX*** tool provides advanced full chip layout parameter and parasitic extraction for IC design using DeepSubMicron process technology. ***HIPEX*** supports GDSII/CIF layout format for input files and SPICE format for extracted netlists.

Distributed parasitic RC networks are output to DSPF or SPEF files suitable for other delay/timing verification tools.