Simulation Standard

Connecting TCAD To Tapeout

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HIPEX-Net: Interface From Expert

1. Introduction

HIPEX-Net is a hierarchical layout extractor. It can create both hierarchical and flat SPICE formatted netlists of the extracted layout. ***HIPEX-Net*** also performs ERC (Electric Rule Checking) on the extracted netlist. This checks for connectivity errors in a chip design such as opens, shorts, and dangling nodes.

HIPEX-Net is a sophisticated script-driven tool. To invoke the extraction, the user must provide a number of input script files in LISA: Language for Interfacing Silvaco Applications. These are option file, layer mapping files, and technology file. ***HIPEX-Net*** technology is defined by a list of various ***LISA*** statements that build derived layers, connectivity, and devices. However, the input generation is easy when running ***HIPEX-Net*** from ***Expert***.

Expert automatically creates all the input files needed by ***HIPEX-Net***. You use the ***Expert*** GUI to define technology and the extractor settings rather than writing ***LISA*** scripts manually. You can also use Dracula technology converter ***Expert*** provides.

HIPEX-Net introduces in ***Expert*** hierarchical Node Probing feature.

2. *HIPEX-Net* Options Dialog Box

The user controls the extractor run-time settings in the ***HIPEX-Net*** Options dialog box. It is composed of Layout, Node names, ERC/Pins, Explosion, Ports, Output, and Netlist Technology Definition pages.

2.1. Layout Settings

Here you choose which cell is to be extracted. You can specify any cell in the layout hierarchy as a top level. The **Flatten Layout** option makes ***HIPEX-Net*** flatten the layout before extracting the netlist. This allows you to process safely layouts with hierarchy violations (devices built partly in one cell and partly in another) at the cost of performance. The **Rebuild Derived** Layers checkbox should be checked if there have been any changes in the layers related to device/connectivity definition. The **Annotate Layout** checkbox makes the Node Probing feature available after ***HIPEX-Net*** completes the netlist

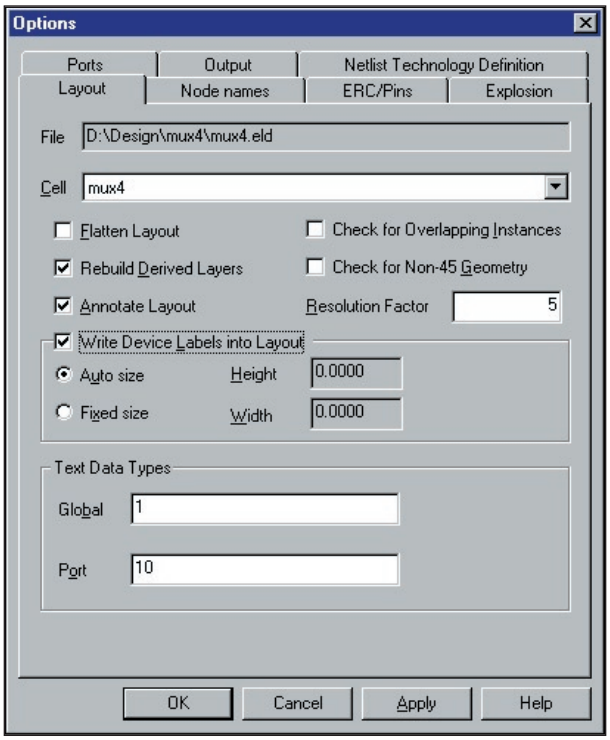

Figure 1. Layout page of the Options dialog.

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INSIDE

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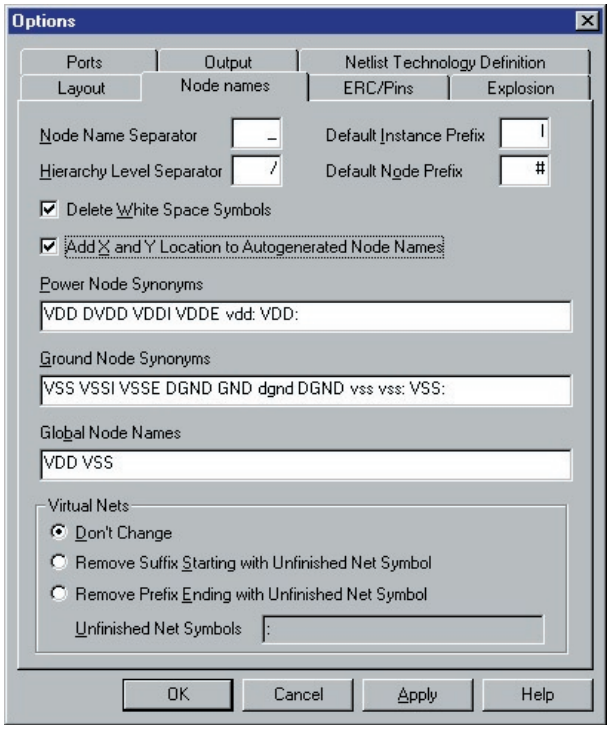

Figure 2. Node Names Options Page.

extraction. Checking this box can decrease ***HIPEX-Net*** performance, but the benefit is that you can search by name or point by mouse nets, devices, and instances to highlight and traverse them directly in the layout editor window.

The two **Check for "..."** options check the layout for multiple identical placements of instances and for non-45 angle geometry. The **Resolution Factor** text box defines the minimum distance that separates two distinct points of the layout.

Using the **Write Device Labels into Layout** group of options, you set up text labels that ***HIPEX-Net*** can add to devices found in the layout. The text is the SPICE statement of the device.

The **Text Data Types** group box contains the two text fields, **Global** and **Port**, for setting the global and port text datatypes. ***HIPEX-Net*** considers text with any other datatype as local text. Local text are labels for a node in a cell, while global text are labels for nodes for the entire layout (e.g., VSS and VDD). Port text are intended to label ports only.

2.2. Node Names Settings

HIPEX-Net extracts text from the layout and uses it to: (1) assign names to nodes in the output netlist and (2) check for opens and shorts in the layout. ***HIPEX-Net*** follows a set of rules when processing layout text for node names. For example, global text always takes precedence over local text. You can fine tune node naming in the Node Names page of the Options dialog (see Figure 2).

Here you define the separator and prefix characters ***HIPEX-Net*** uses in node names. If ***HIPEX-Net*** cannot find text anywhere in the hierarchy for a node, it creates a name for the node automatically based on the serial number. You can make ***HIPEX-Net*** add the X, Y layout local coordinates to autogenerated names by checking the appropriate box.

The two text boxes, **Power Node Synonyms** and **Ground Node Synonyms**, allow you to define the synonym names to the power and ground node. ***HIPEX-Net*** substitutes all the listed names by the first one. The Global Node Names text box lists labels you want to make global in spite of their actual datatype in the layout.

The **Virtual Nets group** box provides options to make ***HIPEX-Net*** consider separated virtual (unfinished) nets as the same net.

2.3. ERC/Pins Settings

HIPEX-Net uses extracted text from the layout to check continuity and reports possible shorts and opens. If ***HIPEX-Net*** finds open or shorted nodes, it flags them by writing error messages to the summary file. ***HIPEX-Net*** can also report dangle nodes that are not attached to any devices.

You control various ERC options in the ERC/Pins page of the Options dialog shown in Figure 3.

Here you choose whether ***HIPEX-Net*** reports in the summary file all the dangles it encounters. Using the

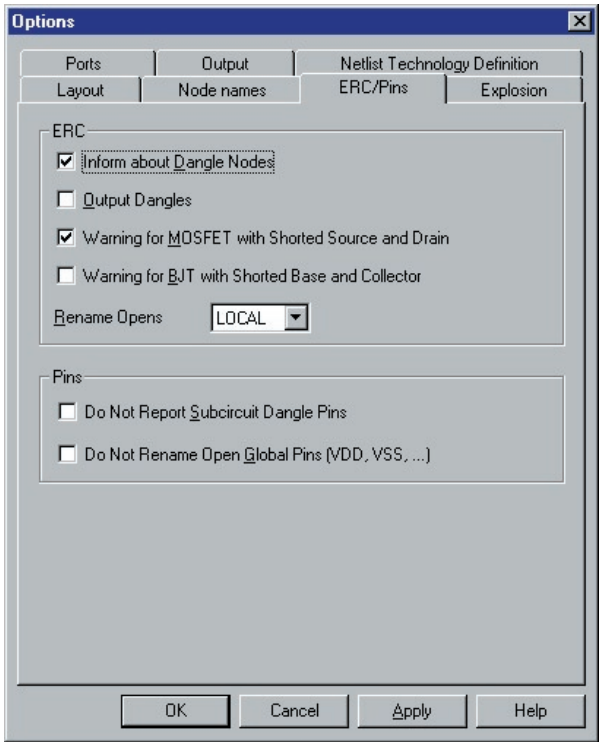

Figure 3. ERC/Pins Options Page.

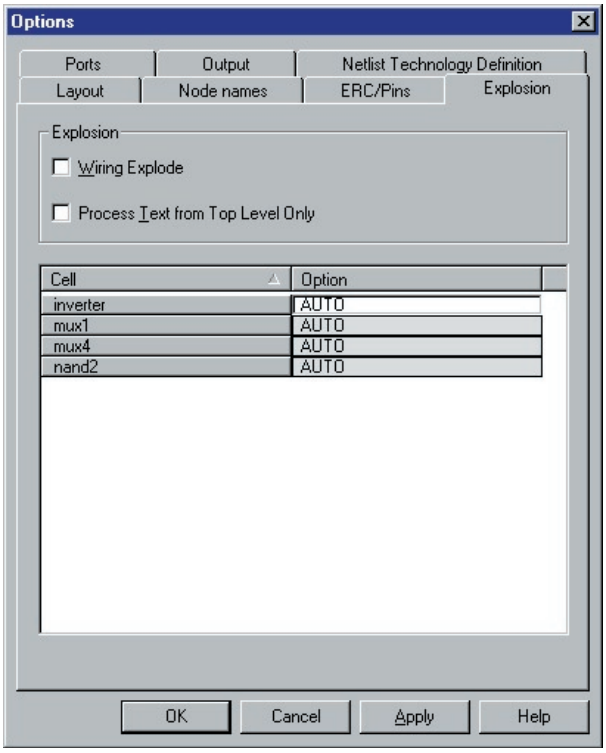

Figure 4. Explosion Options Page.

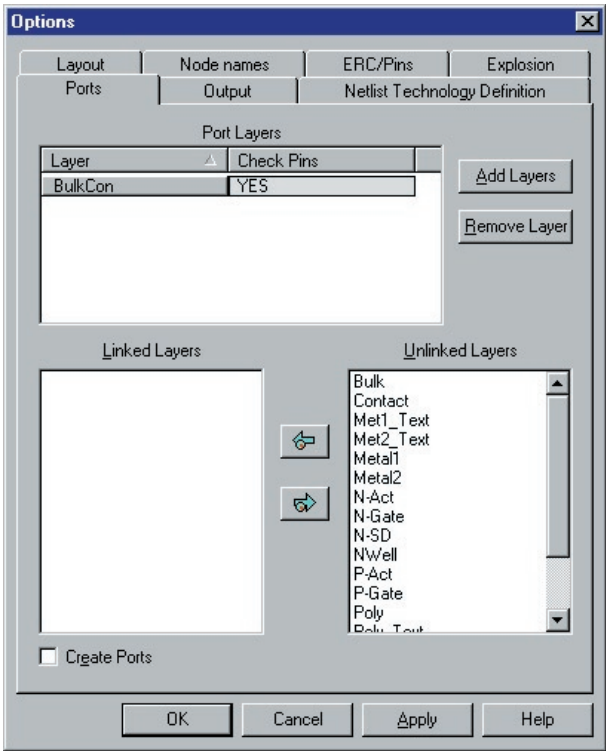

Figure 5. Ports Options Page.

Output Dangles checkbox, you can dump flat layout of the dangle nodes into the separate GDSII file. The two **Warning for "..."** checkboxes make ***HIPEX-Net*** write in the summary file the warning messages about improperly connected MOSFETs and BJTs. The **Rename Opens** drop-down list determines whether ***HIPEX-Net*** assigns different names to the nodes having the same local (in a given cell) or global (in the entire layout) text label.

The **Pins** options determine whether ***HIPEX-Net*** ignores dangle pins of subcircuits and renames open global pins.

2.4. Explosion Settings

In the Explosion page of the Options dialog, you can define various operations on design hierarchy, such as cell explosions and ignoring particular cells during the extraction. Figure 4 shows the Explosion page.

Here you can explode all the instances of cells containing only wiring, raising their content up one level before the cell is processed. The other checkbox forces ***HIPEX-Net***- to ignore all text at lower levels of the hierarchy except the top one.

The table in the bottom of the Explosion page allows you to define operations on individual cells. The allowable operations are: EXPLODE, FLATTEN, SMASH, and IGNORE. The AUTO option means do nothing.

2.5. Ports Settings

One of the benefits using ***HIPEX-Net*** is that it doesn't force you to declare the cell pins or assign names to cell pins. ***HIPEX-Net*** creates pins automatically when it finds any hierarchical connection (that is, between cells from

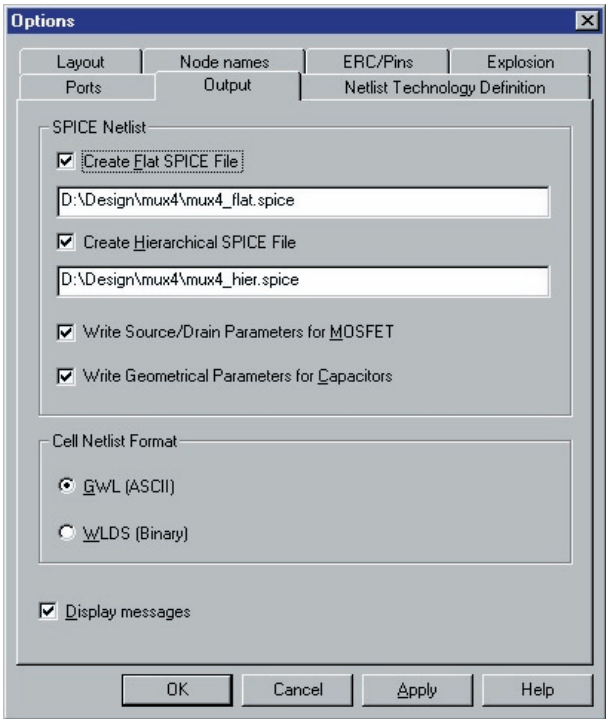

Figure 6. Output Options Page.

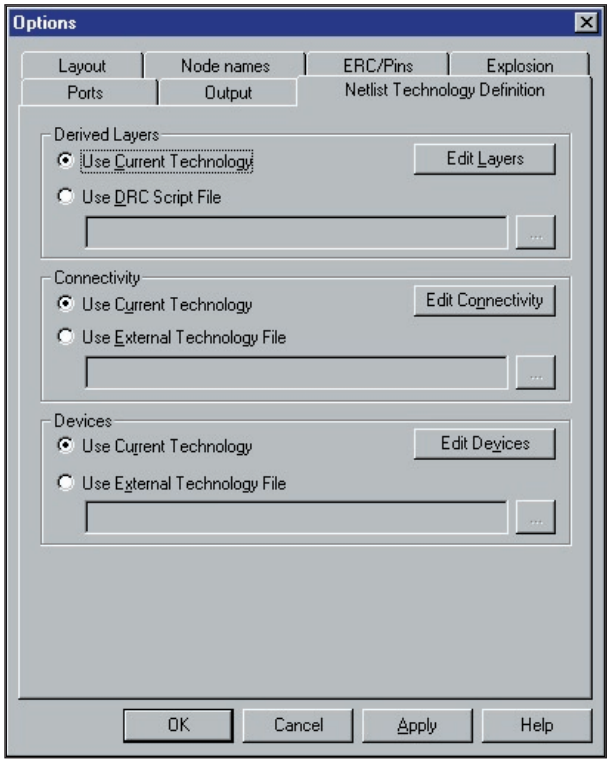

Figure 7. Netlist Technology Definition Page.

different hierarchy levels). Nevertheless, ***HIPEX-Net*** allows you to predefine names and locations of cell pins. These predefined pins are called ports. There are a couple of advantages using ports. One advantage is you can define pins for the top cell in the layout. The other advantage is you can verify hierarchical connections (i.e., pins) by ports. If you do so, ***HIPEX-Net*** creates pins only in those locations where both pin and port are present.

You define ports in the Ports page of the Options dialog box (see Figure 5).

Use a special port layer in your layout (you can also use several port layers if needed). Give your ports names using port datatype text. Then, set this layer as port layer using the **Add Layers** button. Once you define port layer(s), you can link/unlink conductor layers to the selected port layer. Then, the port-linked conductor layers can be verified for hierarchical connections that go through them. You can force HIPEX-NET to create subcircuit pins in the port locations, even if there are no actual hierarchical connections, by checking the **Create Ports** box.

2.6. Output Settings

In the Output page of the Options dialog, you define filenames of the output SPICE netlists and control SPICE device parameters to be written to those netlists. Figure 6 shows the Output page.

The two **Write "..."** allow you to output additional SPICE parameters for MOSFETs and capacitors.

3. Netlist Technology Definition

The Netlist Technology Definition page of the Options dialog allows you to define technology information needed by ***HIPEX-Net***. ***Expert*** saves the user technology definitions in the project file (.eld file). Then, the layout editor converts the technology data to the ***HIPEX-Net*** technology file once you run the extractor.

HIPEX-Net deals with three types of technology information (see Figure 7): Layer Derivation Statements **(Derived Layers),** Connectivity Statements **(Connectivity),** and Device Definitions **(Devices).** You can modify these types of technology parameters separately.

For technology definition, you can use GUI controls and dialogs accessible from the page above. The alternative way is to load technology data from external ***Expert*** technology files (.tcn files). You can create .tcn files in any text editor manually or use the **Setup>>Technology>> Import Technology"..."** menu command to convert Dracula rule files.