

Hints, Tips and Solutions

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Q. My simulation fails because *SmartSpice* cannot find a binned model, what does this mean ?

Normally when a MOS model is extracted for a range of devices it is scaleable over the range of device geometries i.e. it is a continuous varying function over the required operating region for all device geometries. Sometimes there is too much variation in the output characteristics to be covered by one continuous model parameter set e.g. "straight" and "dog-bone" layout designs which contain very different electric field patterns. The total operating region is therefore broken up into sub-sections and a model produced for each of these subsets of device geometry. This is a binned model where each region is a different set of model card values for a smaller range of device properties like width, length and temperature. In this way a group of model card parameter sets can be used to cover a wide variation in say gate width and length variations not possible from a single scaleable model. In the simple case these bins are ranges of Width and Length transistor geometries that say what model card parameter set should be used. The only problem with this approach is a discontinuity at the boundary of one model set to another and can be thought of as trying to approximate a curve with a set of straight lines. Your error is because the device geometry is not covered by any of the specified ranges in the model library. Typically the binned model will have a model name of say nch.1, nch.2, nch.3 etc. and you device geometry is not allowed for in the say Lmin to Lmax range of any of these binned model sections.

New options functionality in *SmartSpice*

There are a number of .OPTIONS & variables in *SmartSpice* to allow the user to tailor the simulation environment to his needs. This becomes a bit confussing when there are so many options and they are inter-dependant and their influence on the circuit understood. To help the customer we have included a new variable in *SmartSpice* setoption

Since there are a number of option settings in *SmartSpice* that are not independent of each other we have created a new .OPTION optionset=<val> to simplify things. *SmartSpice* with the cell characterization values:

| Optionset=<val> | Option used | Value |
|-----------------|---------------|-------|
| 3 | accurate | 1 |
| | cnode(cshunt) | 1e-12 |
| | ITL1 | 5000 |
| | ITL2 | 5000 |
| 4 | accurate | 1 |
| | cnode(cshunt) | 1e-12 |
| | conv | 1 |
| | accept | TRUE |
| | ITL2 | 5000 |

Optionset=3

This is recommended for transient analysis. This set of options helps to fix "Time step too small" problem (cnode=1.0E-12). Option ITL1=5000 allows more regular Newton iterations for the OP calculation. If the regular Newton iterations fail, *SmartSpice* automatically goes to the advanced stepping algorithm and uses 5000 iterations to find the OP. This set of options can be used if the transistor/diode models behave properly and the I/V curves are smooth.

Optionset=4

This is recommended for transient analysis to cover failure during .OP calculation due to slow convergence (ITL2=5000), helps to fix "Time step too small" during transient analysis (cnode=1.0E-12) and automatically accepts the solution during the advanced stepping in the OP calculation (ACCEPT). It also improves the I/V characteristics of the transistors and diodes when these curves are more irregular and uses DCGMIN parameter stepping (CONV=1) to fix internal device conductance's. This set of options is recommended for all cell characterization to cover convergence failures.

Q.How to detect bad models and solve the model problem ?

The construction of the device model is the fundamental building block on which the rest of the functionality is based. If the model card construction is poor then you can use the "gnode" option with a high value to get convergence but this just swamps the device with conductance masking the underlying problems and in some case just simulating a completely different circuit to the one intended. To detect a bad model you can include in the model card "PARAMCHK=1" this will highlight bad basic parameter values and the combination of parameters that lead to some equations of the model being outside or near their range limits. Another way is to include in the main input deck ".OPTIONS EXPERT". This allows a lot of errors to be reported and for every time point iteration so it is best to use this with a very limited simulation time to avoid too many repeated messages for each time point iteration. For the case where you have BSIM3v3 models ".OPTIONS EXPERT=779" is best giving more detail for this particular model and possible conflicts in the different aspects of the model to make sure it is overall consistent in specification. The input decks should also contain the setting ".OPTIONS CONV=1" which helps dc convergence by going straight to a more sophisticated stepping algorithm and giving more detail and suggestions should this stage fail to find an operating point.

Call for Questions

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