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A CAD Framework for Co-Design and Analysis of CMOS-SET Hybrid Integrated Circuits

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Abstract

This paper introduces a CAD framework for co-simulation of hybrid circuits containing CMOS and SET (Single Electron Transistor) devices. An improved analytical model for SET is also formulated and shown to be applicable in both digital and analog domains. Particularly, the extension of the recent MIB model for single/multi gate symmetric/asymmetric device for a wide range of drain to source voltage and temperature is addressed. Circuit level co-simulations are successfully performed by implementing the SET analytical model in Analog Hardware Description Language (AHDL) of a professional circuit simulator ***SmartSpice***. Validation at device and circuit level is carried out by Monte-Carlo simulations. Some novel functionality hybrid CMOS-SET circuit characteristics: (i) SET neuron (ii) Multiple valued logic circuit and (iii) a new Negative Differential Resistance (NDR) circuit, are also predicted by the proposed SET model and analyzed using the new hybrid simulator.

I. Introduction

Although scaling of CMOS technology has been predicted to continue for another decade, novel technological solutions are required to overcome many limitations of the CMOS [1]. Several *nanotechnologies* are rapidly evolving, but at this point it seems unlikely that any of them can completely replace CMOS [2]. However, co-design of CMOS and some suitable nanotechnology seems more plausible [3]. In fact, in the near future, it seems highly probable that CMOS technology will need to share its present domination on modern ICs with fundamentally new nanotechnologies such as Single Electron Transistors (SET) that use a few electrons [4]. It appears that

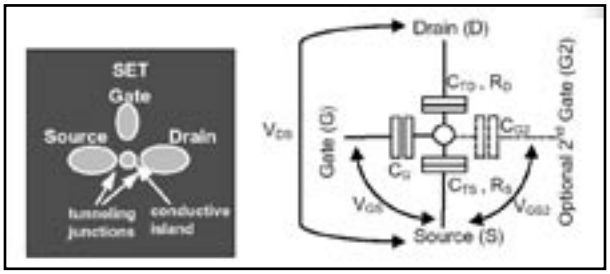

Figure 1. Schematic of a SET. Here CG is the gate capacitance, C_{G2} is the optional second gate capacitance, C_{TD} and C_{TS} are the drain and source tunnel junction capacitances, respectively, and R_D and R_S are drain and source tunnel junction resistances, respectively.

CMOS and SETs are rather complementary: SET is the *campaigner of low-power consumption* [5,6] and of new functionality while CMOS has advantages like high-speed driving and voltage gain, which can compensate exactly for SET's intrinsic drawbacks. Therefore, although a complete replacement of CMOS by SETs is highly unlikely in the near future, it is also true that combining SET and CMOS can bring out new functionalities [7-8], which are un-mirrored in pure CMOS technology.

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INSIDE

It is well known that Computer Aided Design (CAD) and simulation of electron devices and circuits (using tools like SPICE) are one of the key factors contributing to the success of the CMOS technology. Therefore, a successful implementation of SET as a candidate for hybrid CMOS-nano VLSI also demands accurate modeling and simulation of CMOS-SET devices and circuits. Hence, a suitable simulation framework for exploration of hybrid CMOS-SET circuit architectures is highly desirable. In this paper we introduce a new CAD framework for co-simulation of hybrid CMOS-SET circuits. An improved analytical model for SET is also formulated and shown to be applicable in both digital and analog domains. The SET model is validated using Monte Carlo simulations, which are typically used as a benchmark for accurate SET- device and circuit level simulations. Some novel functionality CMOS-SET circuit architectures are analyzed using the new hybrid simulator.

A schematic of a SET, which consists of a tiny conductive island, two high resistive (>26kΩ) tunnel junctions, and an opaque gate is shown in Figure 1. It is worth noting that the operation of the SET devices is based on the *Coulomb Blockade* phenomenon [9], which is quite unique compared to the principle of operation of MOS transistors. By exploiting this particular Coulomb Blockade phenomenon, several *niche* applications of SET devices have been demonstrated in logic circuits (inverter, logic gates etc.)[5,6,10], analog circuits (neuron cell, negative differential circuit [8,11]) and in mixed signal circuits (quantizer [7]) regime.

II. Set Simulation: An Overview

Monte Carlo (MC) simulation method is the most popular approach that is employed to simulate single electron devices and circuits. Some of the widely used single-electron MC simulators are SIMON [9], MOSES [12] and KOSEC [13]. Some efforts have also been made to simulate single electron device and circuit characteristics by Master Equation Method (e.g.: SETTRANS [14]). It should be noted that:

1) These methods calculate single electron device and circuit characteristics based on "Orthodox Theory" [9] (i.e., manipulating electron energy with the help of complex Fermi-Dirac distribution and Fermi's golden rule) instead of using any analytical model of SET.

2) These simulators are developed in order to simulate generalized single electron devices (where the charging energy of the island is determined not only by the drain, source and gate capacitances associated with it but also other capacitances associated with other islands in the same circuit) and it is quite impossible to find an analytical model for single electron devices. [Note: SET (where the charging energy of the island is determined solely by the drain, source and gate capacitances associated with it) is a special case of generalized Single Electron Devices].

III. Chalanges of Set-CMOS Co-Simulation

Some previous works have addressed [15] the hybrid SET-CMOS simulation based on background MC or Master equation simulation of SET devices combined with conventional analytical model based on SPICE simulation for MOSFETs. However, the major disadvantage of these approaches is time-consuming computation (especially for the calculation of transient response, current sources and resistances), and concrete limitations for more complex circuits.

It should also be noted that simulation of SET devices are not as straightforward as CMOS devices. Some architecture, which is commonly used in CMOS technology, may be 'forbidden' in SET circuits. One such example is shown in Figure 2. The architecture in Figure 2(a) is commonly used in CMOS (e.g. Differential Amplifier) however a similar SET prototype [Figure 2(b)] may create instability in the circuit (and convergence problems in simulation) as the periodic I_{DS}-V_{GS} characteristics of a SET offer several possible values of V_{GS} is for a certain value of IBIAS [Figure 2(c)]. We'll see in §VIII.III how we can exploit such an apparent limitation to provide NDR characteristics in a hybrid CMOS-SET IC.

Apart from MC and Master Equation method, "Macro Modeling" technique [16] has also been employed in order to simulate SET devices and circuits. Although this technique is SPICE compatible and useful for co-simulation with MOS, its non-physical (or, empirical) nature makes it an inconvenient tool for practical SETCMOS hybrid IC design. Therefore, a successful implementation of SET as a candidate for post-CMOS VLSI demands an accurate analytical SET model instead of Monte Carlo (MC) simulation, Master Equation Method or macro modeling.

Recently, analytical models MIB [5,17] and Uchida et al.[18] have been reported, which appear to be extremely exciting for practical IC design. These models are physically based, and are easily used in conventional SPICE for the co-simulation with CMOS devices.

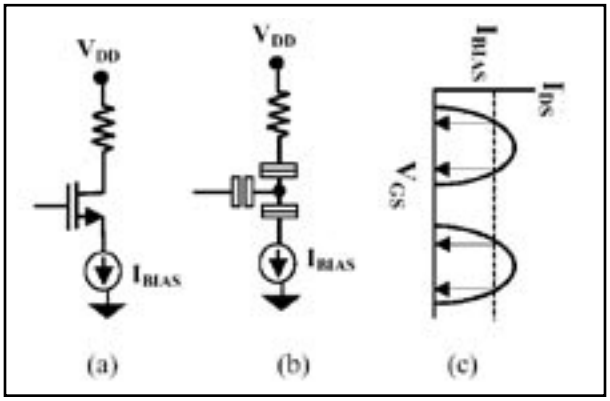

Figure 2. (a) A current bias MOSFET with a floating gate (b) corresponding SET prototype (c) Different possible value of the gate voltage for in (b) for a fixed current bias.

The model reported by Uchida et al.[18] is adequately accurate for high temperatures, however it is only applicable to the *single* gate resistively *symmetric* device and it cannot explain the background charge effect, which is significant for SET operations. On the other hand MIB, which is applicable to single/multiple-gate symmetric/asymmetric devices, can explain the crucial background charge effect. However it is not as accurate as [18] for high temperatures due to its semi-empirical modeling of the temperature effect. One point to note is that, both of these models are developed under the basic assumption of $|V_{DS}| \leq e/C_{\Sigma}$ (where e is the elementary charge and C_{Σ} is the total capacitance of the SET island with respect to ground), which is quite practical for digital circuits (as the SET loses its Coulomb Blockade region and hence the digital switching property when $|V_{DS}| > e/C_{\Sigma}$). However, for the analog application of SET [8], one needs a model which is applicable to any value of V_{DS}. This is due to the fact that:

(i) In a current biased SET (which is a common building block of analog SET circuits) the $|V_{DS}|$ could be more than e/C_{Σ} .

(ii) In CMOS-SET hybrid architecture MOSFET biases may impose $|V_{DS}|>e/C_{\Sigma}$ to operate the SET.

In this work, we have modified the MIB model in order to extend its validity over |VDS| > e/CS specifically for analog circuit operation. Moreover, we have modeled the temperature (T) effect physically so that MIB can predict the device behavior accurately at higher temperatures. In order to exploit the proposed model for SET-CMOS hybrid IC design, MIB has been implemented by the Verilog-A interface (which is one type of Analog Hardware Description Language) in the professional circuit simulator ***SmartSpice*** [19]. Using ***SmartSpice*** different simulations have been performed in SET device and circuit level for different benchmark circuits and good agreement with MC simulation has been observed.

IV. Analytical Models for Set: MIB

SET analytical model MIB, which is founded on the "orthodox theory of single electron tunneling" [9] (i.e., charge is discrete but energy is continuous, tunnel junction resistance is more than the quantum resistance ~ 26KΩ etc.), is based on a practical assumption that the interconnect capacitance associated with the gate, source and drain terminals is much larger than the device capacitances, this ensures the total capacitance of the island with respect to ground is equal to the summation of gate and source/drain tunnel capacitances i.e.,

$$C_{\Sigma} = C_G + C_{G2} + C_{TD} + C_{TS} \quad (1)$$

In this way the SET characteristics are independent of the capacitances of neighboring devices and are only dependent upon the nodal voltages of source, gate and drain terminals.

In this work, the following improvements are made over the earlier version [5] of MIB:

- MIB is extended for $|V_{DS}| \leq 1.5e/C_{\Sigma}$ for *resistively symmetric device and* $|V_{DS}| \leq 1.2e/C_{\Sigma}$ *for resistively asymmetric device*, which is essential for analog applications of SET. It is found that for $|V_{DS}| > 1.5e/C_{\Sigma}$, variation of I_{DS} with V_{GS} becomes too small to exploit in any circuit application
- The temperature effect is modeled physically which enables the temperature range of MIB to be extended
- Another key result, the Subthreshold Slope can be estimated analytically

The algorithm for the calculation of drain current in MIB model (Figure 3) can be briefly discussed as follows:

Based on the external bias voltages (V_{DS}, V_{GS}, V_{GS2}) the initial (before any electron tunneling has occurred) island potential (V_{island}) can be calculated as:

$$V_{island} = (C_{TS}/C_{\Sigma})V_{DS} + (C_G/C_{\Sigma})V_{GS} + (C_{G2}/C_{\Sigma})V_{GS2} - ne/C_{\Sigma} \quad (2)$$

where n is a real number representing the background charge. Now, according to the "orthodox theory", when the potential difference between island-and-source or drain-and-island becomes larger than V_{Σ} *[= e/(2C$_{\Sigma}$)]*, one electron tunnels-in or tunnels-out from the source to island or island to drain and as a result V_{island} decreases (for tunnel-in) or increases (for tunnel-out) by an amount of $2V_{\Sigma}$. However, if the potential difference between island-and source or drain-and-island becomes less than VS no electron tunneling happens and the device enters into the Coulomb Blockade region. The first pair of *'while'* statements in the MIB algorithm (Figure 3) is used to modify the initial island potential (V_{island}) in order to capture the periodic Coulomb Blockade oscillation characteristics of SET. Based on this modified value of V_{island}, the drain current (I_{DS}) is formulated as

$$I_{DS} = I_D I_S/(I_D+I_S) \quad (3)$$

Here I_S and I_D are the electron-tunneling *current* from source-to-island and island-to-drain respectively which can be expressed as

$$I_S = \frac{V_{island} - V_{\Sigma}}{R_S} \frac{1}{1 - exp\left[-\frac{V_{island} - V_{\Sigma}}{V_T}\right]} \quad (4)$$

$$I_D = \frac{V_{DS} - V_{island} + V_{\Sigma}}{R_D} \frac{1}{1 - exp\left[-\frac{V_{DS} - V_{island} + V_{\Sigma}}{V_T}\right]} \quad (5)$$

where V_T (= $k_B T/e$, k_B is the Boltzmann's constant) is the thermal voltage. It should be noted that the expressions of I_S and I_D are purely based on the "orthodox theory" of single tunneling and completely different from the older version of MIB (where the temperature effect was modeled empirically). In order to include the $|V_{DS}| > e/C_{\Sigma}$ effect, in this work, we have added an extra component to the main component of the drain current as shown in Figure 3.

It is worth noting that all the model parameters of MIB are physical: (i) drain and source tunnelling capacitances (C_{TD} and C_{TS}), (ii) first and second gate capacitances (C_{G1} and C_{G2}), (iii) drain and source tunnel junction resistances (R_D and R_S), and the background charge (n).

V. Implementation of MIB in Verilog-A

Verilog-A [19] is a "high level hardware description language" of analog systems by which one can mix ***SmartSpice*** device models (such as BSIM [19], EKV [19] etc.) and Verilog-A modules in the same netlist. In this work, we have implemented the MIB model for SET devices in Verilog-A language and then simulated them with the ***SmartSpice*** simulation kernel as shown in Figure 4. In this way, we can use the MIB analytical model to co-simulate the SET device with any other solid-state device (MOS, BJT etc.) instead of using the time consuming MC technique [9,12,15]).

In the present work one can use various levels of complexity of MIB which are listed as:

LEVEL1: $T = 0$, $|V_{DS}| \le e/C_\Sigma$ (for hand calculation)

LEVEL2: $T < e^2/(20k_BC_\Sigma)$; $|V_{DS}| \le e/C_\Sigma$ (for digital operation)

LEVEL3: $T < e^2/(20k_BC_\Sigma)$; $|V_{DS}| \le 1.5e/C_\Sigma$ for symmetric and $|V_{DS}| \le 1.2e/C_\Sigma$ for asymmetric SET. (analog purpose)

It should be noted that the SET module is implemented with default values of model parameters (gate capacitances, tunnel junction capacitances and resistances, and back ground charge),which can be changed easily through the MODEL CARD in the SPICE netlist.

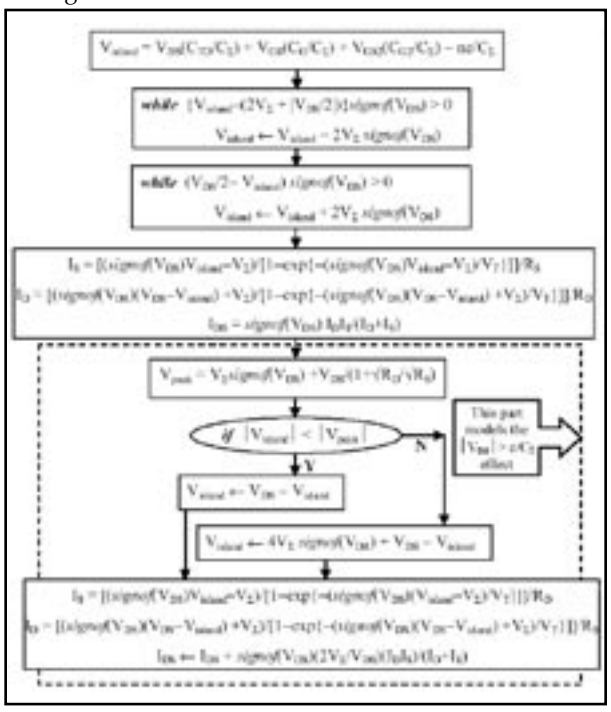

Figure 3. Flowchart for the MIB analytical Model.

VI. MIB Model Verification

The proposed model (embedded in SMARTSPICE) has been verified against the simulated data from the widely accepted Monte Carlo simulator SIMON [9]. Figure 5(a) reveals the validity of our model for a wide range (even more than e/C_Σ) of values of V_{DS}, which is important for SET analog operation. Figure 5(b) demonstrates the accuracy of our model for an asymmetric SET. It should be noted that by introducing asymmetry one could reduce the static power dissipation in SET logic while keeping the dynamic power dissipation and propagation delay almost constant [5]. However the importance of resistively asymmetric current biased SET in analog applications has not yet been demonstrated. Figure 5(c) exhibits the validity of the MIB model for a wide range of temperatures up to $T = e^2/(20k_BC_\Sigma)$, Note: According to Kirihara et al.[20] maximum temperature for stable SET logic operation is $e^2/(40k_BC_\Sigma)$. From our new model the subthreshold slope (S) of the SET is found to be $S = dV_{GS}/d\log_{10}I_{DS} \approx (C_\Sigma k_B T)/(0.434eC_G)$.

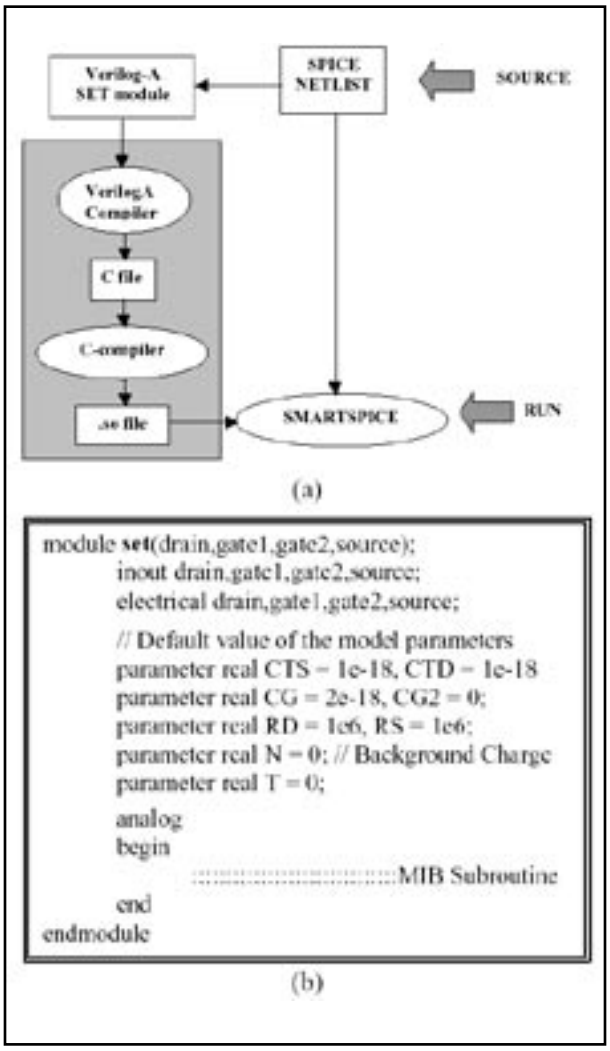

Figure 4. (a) Working principle of Verilog-A in SMARTSPICE (b) partial architecture of Verilog-A SET module.

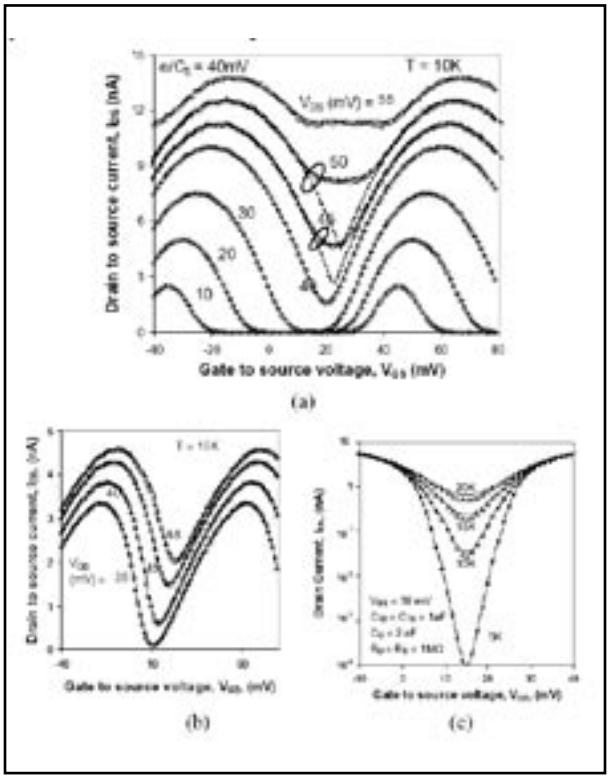

Figure 5: Verification of MIB model for (a) symmetric SET device with $C_G = 2aF$, $C_{TD} = C_{TS} = 1aF$ and $R_D = R_S = 1M\Omega$. Here symbols denote Monte Carlo simulation (SIMON) and solid line represents MIB LEVEL3 and dotted line represents MIB LEVEL2 (without $|V_{DS}|>e/C_\Sigma$ correction). (b) asymmetric device with $C_G = 2aF$, $C_{TD} = 1.5\,aF$, $C_{TS} = 0.5aF$ and $R_D = 1M\Omega$ and $R_S = 5M\Omega$ (c) effect of temperature on the device characteristics.

VII. Pure Set Logic Circuit Simulation

Static and transient responses of a SET inverter cell are successfully predicted [Figure 6] by ***SmartSpice*** simulation. Comparison and good agreement with MC simulation reveals the accuracy of our SPICE simulation in both static and dynamic regimes as given in Figure 6(a) & (b). One should note that a SET inverter is different from a typical CMOS inverter in the following respects:

(i) In a SET inverter the two transistors are completely identical to each other (in contrast with a CMOS inverter where we have one p-MOS and one n-MOS).

(ii) Unlike the CMOS counterpart, the SET inverter does not offer a constant voltage level when the output is in logic high or low.

(iii) The gain of a SET inverter is quite low compared to a CMOS inverter and it is determined by C_G/C_T ratio.

(iv) In contrast to the CMOS inverter, power dissipation in SET logic is dominated by static power dissipation.

A detailed analysis of the SET inverter along with the effect of background charge, device asymmetry and temperature on the inverter characteristics could be found in [5].

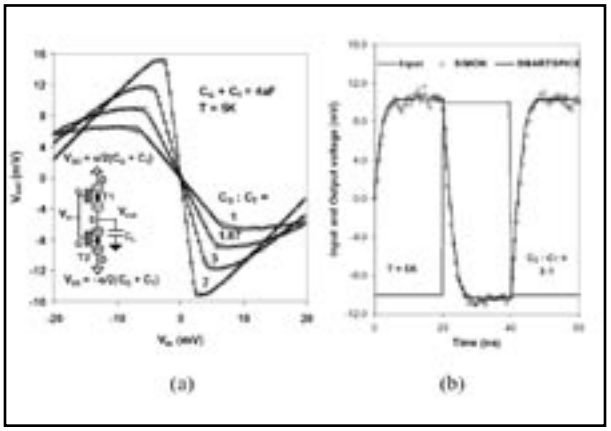

Figure 6. SET-inverter (a) static and (b) transient characteristics for different values of C_G/C_T (solid line = ***SmartSpice*** and symbol = SIMON). T1 and T2 are identical with $R_D = R_S = 1M\Omega$, $C_T = C_{TD} = C_{TS}$ and load capacitance $CL = 1fF$. The oscillations in the MC simulation in (b) are due to the noise in the random number generator.

VIII. Hybrid CMOS-Set IC Simulation

As mentioned previously, a complete substitution of CMOS by single-electronics is highly improbable in the near future, therefore we have to combine SET and CMOS in order to bring out new functionalities. For these reason it is extremely important to develop a simulator, which is able to co-simulate SET devices with CMOS. In the following sections we will discuss three examples of CMOS-SET hybrid IC.

VIII.I. Set Casacade Neurone

Since a powerful signal processor demands a large neural network, therefore, due to the power dissipation and size of the neural chip it is difficult to design an efficient neural network by CMOS technology. However, one can exploit the ultra low power dissipation of SET devices and their nano feature size in order to realize a compact neural device.

The basic building block of a neuron is given in Figure 7. The most challenging part of this neuron cell is to design the activation function block, which is generally expressed by a sigmoidal function as given below

$$f(x) = (1-e^{-ax})/(1+e^{-ax}) \qquad (1)$$

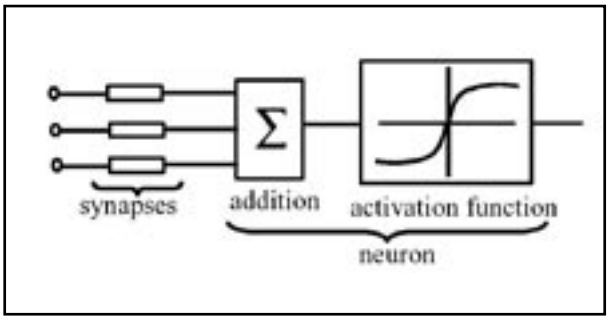

Figure 7. Functional block diagram of a neuron.

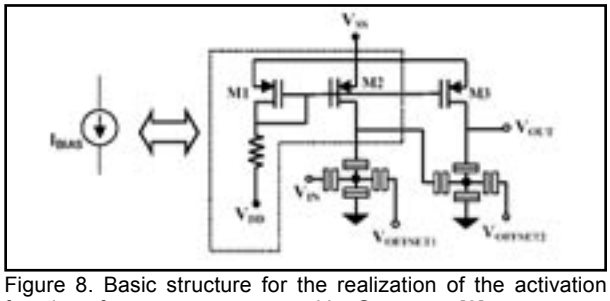

Figure 8. Basic structure for the realization of the activation function of a neuron as proposed by Goossens [8].

As proposed by M. Goossens [8], the activation function of a basic neuron cell can be implemented by two cascaded current biased SET as presented in Figure 8.

According to Goosens [8], for the proper operation of the circuit, the drain and source tunnel capacitances of the SETs have to be equal ($C_{TD} = C_{TS}$) and the gate capacitances have to be twice that ($C_G = C_{G2} = 2C_{TD}$). One point to note is that in order to drive a nA current through the SET one has to bias the MOS transistors in the subthreshold (weak inversion) region.

Using ***SmartSpice***, the static characteristics of the neuron cell [8], have been simulated accurately and good agreement with MC simulation [Figure 9] is shown, this demonstrates the reliability of our physical analytical model. Note: In this figure, MIB model without $|V_{DS}| > e/C_{\Sigma}$ correction is represented by a dotted line. In the the figure the exhibited inaccuracy with MC simulation for a certain range of input voltage, demonstrates the requirement of a SET model to be valid over $1/2V_{DS}1/2 = e/C_{\Sigma}$ for analog circuit applications.

VIII.II. Multiple Vauled Logic

Multiple-valued logics (MVLs) have potential advantages over binary logics with respect to the number of elements per function and operating speed. Most MVL circuits, fabricated with MOS and bipolar devices, have limited success partially because the devices are inherently single-threshold or single-peak, and are not fully suited for MVL. Inokawa et al.[7] have recently proposed a hybrid SET-CMOS MVL circuit for practical applications (e.g., quantizer for digital communication system). Figure 10(a) shows the schematic of the hybrid MVL circuit [7]. The MOSFET with the fixed bias V_{GG} is used to suppress the variation of drain to source voltage of the SET. The simulated V_{in}-V_{out} characteristics of this circuit are demonstrated in Figure 10(b) which shows good resemblance with the measured data as presented in [7].

It is impossible to achieve such characteristics by using a pure conventional SET circuit because the voltage gain of SET circuits is very small.

VIII.III. Hybrid NDR Circuit

A Negative Differential Resistance (NDR) is a resourceful element with a wide variety of circuit applications such as: oscillators, amplifiers, logic cell and memory. Figure 11(a)

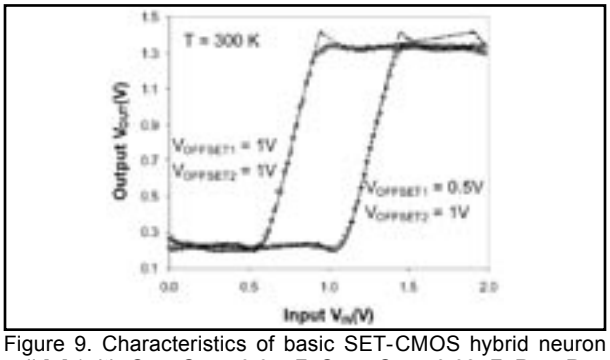

Figure 9. Characteristics of basic SET-CMOS hybrid neuron cell [5] (with $C_G = C_{G2} = 0.04aF$, $C_{TD} = C_{TS} = 0.02aF$, $R_D = R_S = 1M\Omega$) as predicted by SIMON (symbol) and ***SmartSpice*** (solid & dotted line). Note: I_{bias} is taken to be ideal current source of 50nA for SIMON simulation and for ***SmartSpice*** simulation the MOS current source is designed in such a way that it can drive the same bias current through the SET.

demonstrates an alternative CMOS-SET architecture of NDR device [21], which is composed of two cross-connected SETs (S1 and S2) and one MOS current mirror. The I-V characteristics of this NDR circuit and the effect of bias current on the circuit behavior are demonstrated in Figure 11(b). The CMOS current source and the first SET (S1) creates a feedback loop that helps to decrease the gate-to-source voltage (V_{GS}) of second SET (S2) for a certain range of increasing input voltage (V_{IN}), and that follows a decrease in the drain current (or the input current, I_{IN}) of S2, which creates the NDR effect. It is found this NDR architecture appears more versatile than the previously reported structure [11] in terms of dynamic range of NDR region, current controllability and drivability, and offers a very effective solution for real implementation of the NDR functionality.

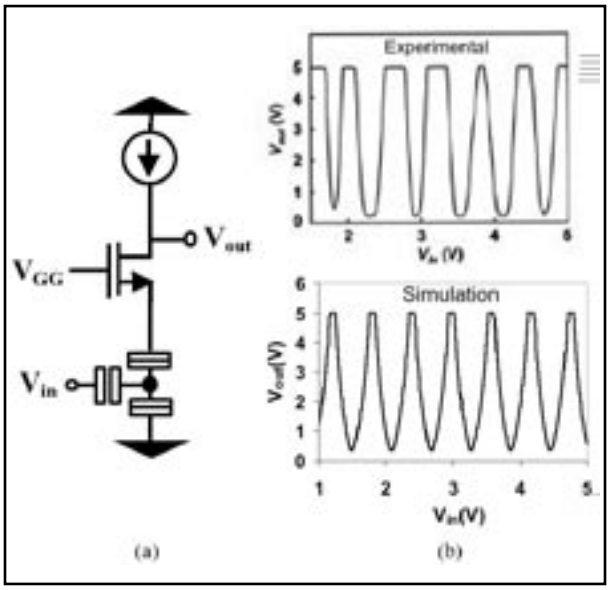

Figure10. (a) A schematic of the universal literal gate comprising a SET and a MOSFET [7]. (b) Comparison between measured and simulated V_{in} –V_{out} characteristics of the universal literal gate at T = 27K. The SET device parameters are C_G = *0.27aF*, $C_{TD} = C_{TS}$ = *2.7aF*, $R_D = R_S$ = *200kΩ* and MOS device parameters are W = 12μm, L = 14μm, t_{ox} = *90nm*. V_{GG} is set to 1.08V and V_{out} is hard-limited at 5V.

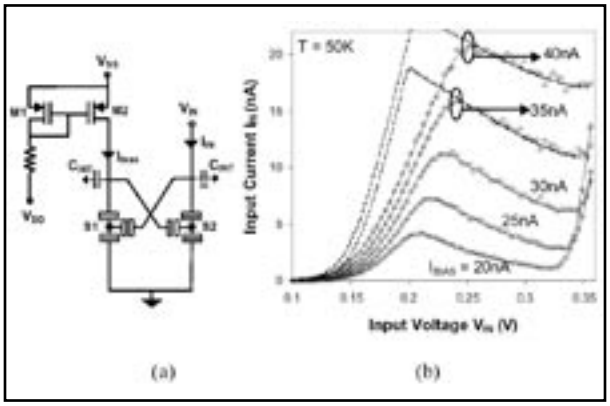

Figure 11. (a) Schematic of CMOS-SET hybrid NDR circuit, where, the interconnect capacitance CINT is much bigger than the SET device capacitances (b) NDR characteristics as simulated by SMARTSPICE (solid line: MIB LEVEL3 and dotted line: MIB LEVEL2) and by MC simulation (by replacing the CMOS current mirror by ideal current source, denoted by symbols) for the SET device parameters C_G = *0.2 aF,* C_{TD} =C_{TS} = *0.15aF,* R_D = R_S = *1MΩ* for S1 and C_G = C_{TD} = C_{TS} =*0.15aF,* R_D = R_S = *1MΩ* for S2. In order to drive *nA* current through the SET one has to bias the MOS transistors of the current source in the weak inversion or in moderate-inversion region.

It should be noted that similar circuit architecture [22] (cross coupled MOS devices) is also used for oscillator design (in order to provide negative differential resistance) in CMOS technology. In contrast with such cross-connected CMOS architecture, the proposed SET circuit requires an adapted current bias [see I_{BIAS} in Figure 11(a)] to provide NDR behavior.

IX. Conclusion

A CAD framework is presented for the design and analysis of CMOS-SET hybrid circuits. An improved analytical model for SET is also formulated and shown to be applicable in both digital and analog domains. Particularly, the extension of the recent MIB model for single/multi gate symmetric/asymmetric device for a wide range of drain to source voltage and temperature is addressed. The proposed model is implemented in the professional circuit simulator ***SmartSpice*** by its Verilog-A interface for the cosimulation with CMOS devices. The model has been validated in both device and circuit level and compared with Monte Carlo simulations. It is worth noting that the proposed MIB model is particularly adapted for both digital and analog hybrid CMOSSET applications. The need and interest of CMOS-SET hybrid IC simulation has been demonstrated for three IC architecture that demonstrate new functionality compared with pure CMOS: (i) SET neuron, (ii) Multiple Valued Logic circuit (iii) new Hybrid NDR circuit.

References:

[1] The International Technology Roadmap for Semiconductors (ITRS), 2002 Edition.

[2] J. A. Hutchby, et al., "Extending the road beyond CMOS," IEEE Circuits and Devices Magazine, Volume: 18 Issue: 2, pp: 28 –41, March 2002.

[3] M. M. Ziegler and M. R. Stan, "A case for CMOS/nano co-design," Proc. ICCAD, 2002, pp. 348-352.

[4] A.M. Ionescu, M. Declercq, S. Mahapatra, K. Banerjee, J. Gautier, "Few electron devices: towards hybrid CMOS-SET integrated circuits", DAC 2002, pp. 88-93.

[5] S. Mahapatra, A.M. Ionescu, K. Banerjee, M.J.Declerq, "Modelling and analysis of power dissipation in single electron logic", Technical Digest of IEDM 2002.

[6] K. Uchida, J. Koga, R. Ohba, A. Toriumi, "Programmable single-electron transistor logic for low-power intelligent Si LSI", ISSCC 2002, Vol. 2, pp. 162-453.

[7] H. Inokawa, A. Fujiwara, Y. Takahashi, "A multiple-valued logic with merged single-electron and MOS transistors" IEDM 2001, pp. 147 -150.

[8] M. Goossens, "Analog neural networks in single-electron tunneling technology", Delft University Press, Nederlands.

[9] C. Wasshuber, "Computational Electronics", Springer Verlag, New York.

[10] Y. Ono and Y Takahashi, " Single electron pass transistor logic and its application to a binary adder", Symposium on VLSI Circuits 2001, pp. 63-66.

[11] C. P. Heij, D. C. Dixon, P. Hadley and J. E. Mooij, "Negative differential resistance due to single-electron switching", Applied Phys. Lett., Vol. 74, No. 7, pp. 1042-1044, 1999.

[12] R. H. Chen, A. N. Korotkov, and K. K. Likharev, "A new logic family based on single-electron transistors", Device Research Conference, pp. 44-45, 1995.

[13] KOSEC(KOrea Single Electron Circuit simulator) is developed in Nanoelectronics Laboratory, Korea University, Seoul, Korea.

[14] http://hana.physics.sunysb.edu/set/software

[15] M. Fujishima, S. Amakawa and K. Hoh, "Circuit simulators aiming at single-electron integration", Jpn. J. Appl. Phys., Vol. 37, pp. 1478-1482, 1998.

[16] Y. S. Yu, S. W. Hwang, and D. Ahn, "Macromodeling of single electron transistors for efficient circuit simulation", IEEE Trans. Electron Devices, Vol. 46, No. 8, pp 1667-1671, 1999.

[17] S. Mahapatra, A.M. Ionescu, K. Banerjee, "A quasi-analytical SET model for few electron circuit simulation", IEEE Electron Dev. Lett., Vol. 23, No. 6, pp. 366 –368, 2002.

[18] K. Uchida, K. Matsuzawa, J. Koga, R. Ohba, S. Takagi, and A. Toriumi, "Analytical single-electron transistor (SET) model for design and analysis of realistic SET circuits", Jpn. J. Appl. Phys., Vol. 39, Part 1, No. 4B, pp. 2321-2324, 2000.

[19] *SmartSpiceUser Manua*l, SILVACO Inc., www.silvaco.com

[20] M. Kirihara, N. Kuwamura, K. Taniguchi and C. Hamaguchi: Ext. Abst. 1994 Int. Conf. Solid State Devices and Materials (Business Center for Academic Socities Japan, Tokyo, 1994), pp. 328.

[21] Ongoing research in authors' group.

[22] A. Hajimiri, T. H. Lee, "The design of low noise oscillators", Kluwer academic publishers, 1999, Boston, USA.

Behavioral Modeling and Simulation in the *Scholar* Schematic Environment

Introduction

This article focusses on the use of Silvaco International's schematic capture and editing tool ***Scholar*** combined with Verilog A. Verilog A is a standard language used for behavioral level modeling. Verilog A combined with ***Scholar*** forms a powerful tool capable of running both schematics with Verilog A modules and mixed Verilog A and physical model simulations. Verilog A may also be used in an environment for compact model development but primarily it is used to reduce schematics of significant amounts of transistors into efficient maintainable and changeable blocks which can be instantiated on any level of a design.

Silvaco's ***Scholar*** is the entry point for the ***Analog Express*** design environment. The ***Scholar*** schematic is netlisted for ***SmartSpice*** and tightly integrated for running simulations concurrent with the schematic. ***Scholar*** handles behavioral simulations in two ways:

- Use of analog behavioral SPICE element (A device)
- Verilog-A

The analog behavioral element (A device) is a two-port device capable of describing a voltage across or current through the pins of the device. These currents and voltages may be logical expressions or user-defined functions. Listed below is an example of an A device which is defined here as a temperature dependent linear resistor connected between nodes A and D:

```
TEMP = 100
.PARAM RNOM = 10
+ TNOM = 25
+ TC1 = 0.02 TC2 = 0.03
+ DT = 'TEMP - TNOM'
AR A D I = (V(A) - V(D)) / (RNOM * (1. + TC1
  * DT + TC2 * DT^2)
```

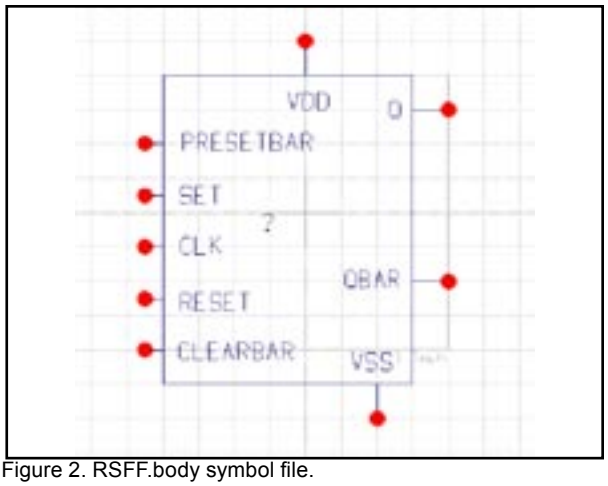

Figure 2. RSFF.body symbol file.

Figure 1. RSFF.va file containing ***Verilog-A*** module.

The current through this device is a function based on the temperature coefficients and voltage difference across the terminals of the device. This is an adequate behavioral modeling for simple devices. However, more complex devices need a language suited for producing behavioral models capable of reducing hundreds to thousands of transistors to single or multiple behavioral blocks. In this case, the Verilog-A language built into ***SmartSpice*** provides a powerful solution to achieve accuracy and gain speed.

Advantages of the Schematic Driven Environment

- ***Verilog-A*** modules may be used inside a multilevel design hierarchy by instantiating Child Verilog.va files inside a Parent Verilog.va module
- Schematic environment provides capture of mixed ***Verilog-A*** and physics –based models for simulation
- Schematic symbols may be mapped to analog primitives -- SPICE devices, model cards or subcircuits that can be instantiated from a ***Verilog-A*** module
- In the ***Scholar***+***Verilog-A*** environment, top-down approach design methodology is easily utilized which produces requirements for deriving the individual circuit blocks

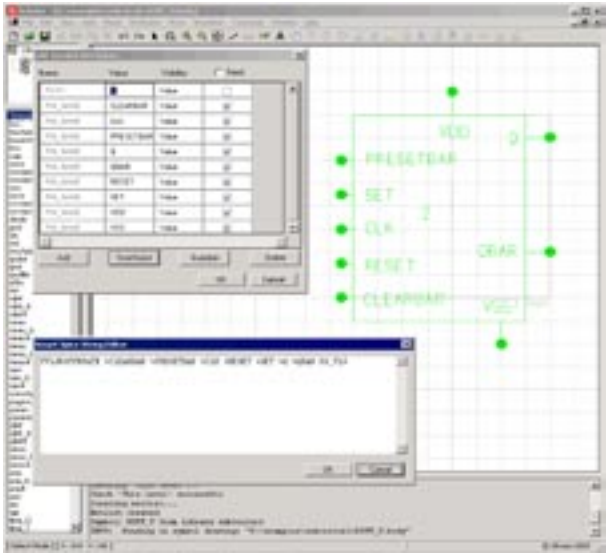

Figure 3. Defining SmartSpice string for the RSFF.body symbol.

How to Implement *Verilog-A* in *Scholar*

To use the environment for schematic, simulation, ***Verilog-A***, and postprocessing, the following licenses are required:

- ***Scholar***
- ***SmartSpice***
- ***Verilog-A***
- ***SmartView***

The following example is for an RSFF simulation using ***Verilog-A***:

1. Create a *.va file. This is file containing the ***Verilog-A*** module(s). In this case, a RSFF.va file is created with the RSFF module definition. (Figure 1)
2. Create a symbol in Scholar to reference the RSFF.va file from the first step. (Figure 2)
3. Define the ***SmartSpice*** string for the symbol. (Figure 3) This string is defined as follows
   - Reference designator YVLGRSFF@PATH which defines each instance as type YVLG (***Verilog-A*** device).

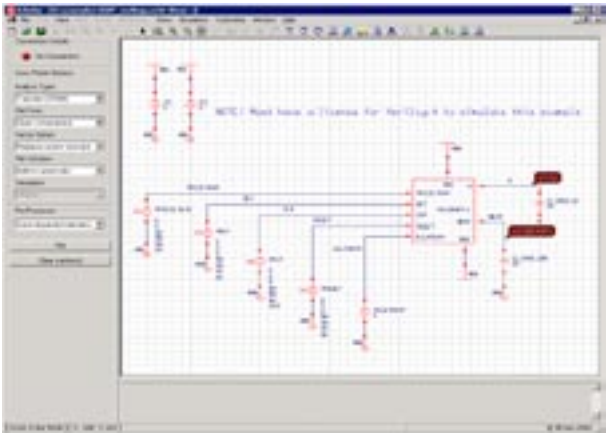

Figure 5. Create schematic to simulate the module.

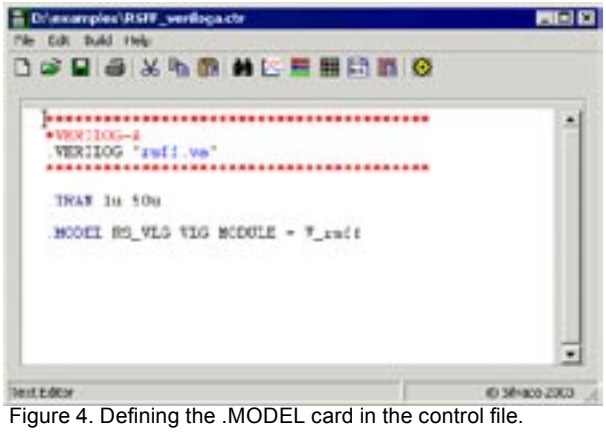

Figure 4. Defining the .MODEL card in the control file.

   - The pins are defined in the order which they should netlist, each pin name beginning with the % character in the string
   - Finally, the model name for the device, RS_VLG
4. Define the model card for the Verilog-A module in the control file (*.ctr). In this example, the model RS_VLG is linked to the V_rsff module in the RSFF.va file (Figure 4)
5. Create the schematic and instantiate the Verilog-A symbol created in step (2) (Figure 5)
6. Simulate the schematic and view the results (Figure 6)

Conclusion

The ***Scholar*** schematic editor is a tool capable of driving simulations for both physics-based device models and behavioral level modeling using ***Verilog-A***. Top-down design saves time and drives the design of individual circuit-level blocks. With the scholar interface, symbols may be readily changed in and out, swapping the transistor level designs and the ***Verilog-A*** behavioral designs, providing designers with the means to reduce simulation time for portions of the design and overlay results on the same plots.

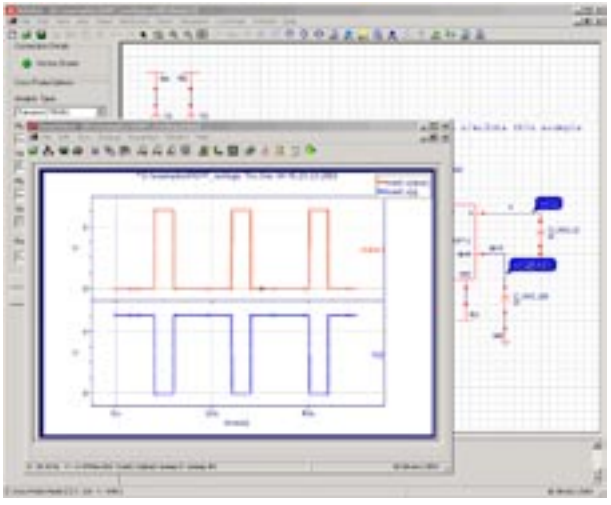

Figure 6. Simulation of RSFF Verilog-A module and results.

SmartView –
Integration Aspects and Key Atrributes

Introduction

This simulation standard will discuss Silvaco International's post processing application ***SmartView*** and will highlight features that identifying it as an important tool to the design engineer. In particular, the integration of ***SmartView*** with ***SmartSpice*** will be discussed in addition to its key attributes within the ***SmartView*** interface.

Integration Issues

The integration of ***SmartView*** into Silvaco International's circuit simulator ***SmartSpice***, permits the direct transfer of data between applications. This capability eliminates the need to write data to a file as an intermediate stage and will thus significantly reduce computation time. This integration of applications will also allow data transfer from a shared server farm directly to ***SmartView*** running on the user's on work station.

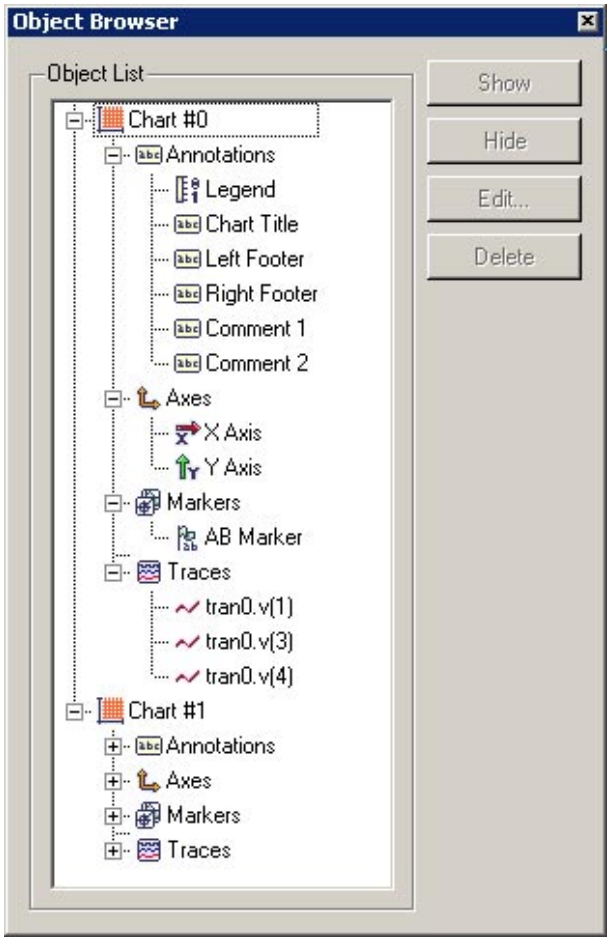

Figure 2 Example of an Object Browser in ***SmartView***

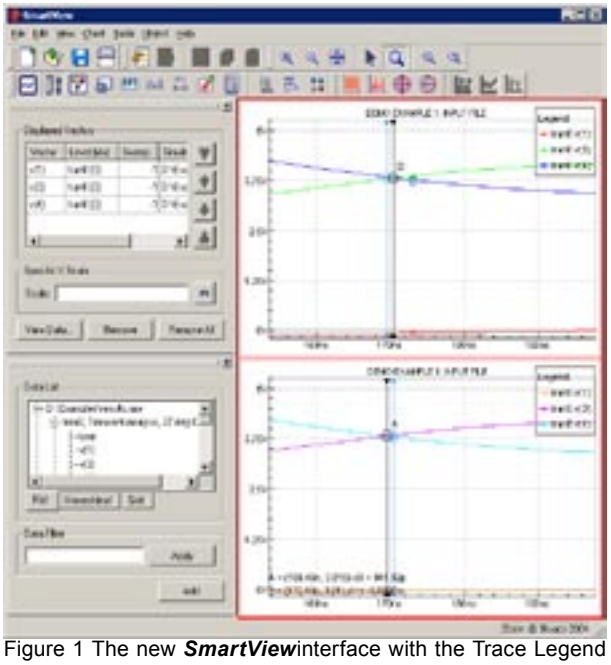

Figure 1 The new ***SmartView***interface with the Trace Legend and Data Browser docked in the main window.

SmartView interface key attributes

The ***SmartView*** interface supports context sensitive menus for all user editable chart objects and an example is shown in figure 1. With the simple double click every visible chart object can be edited. The interface also includes customisable features on all supported platforms. ***SmartView*** has many key attributes and an exhaustive list is not possible within this simulation standard. However, some key attributes has been highlighted which should improve the user's understanding of the application. Some of ***SmartView 's*** key attributes are as follows:

- Drag and Drop of traces from the data browser window to a chart, between charts and into text fields. Making it easier to select and use traces in measurements and the calculator.
- Every reversible user interaction events (i.e. create, select, edit, delete and move object events) can be undone and then redone.
- Object Browser for the quick location of hidden and off screen objects.(See Figure 2)
- All charts of the same type use the identical screen dimensions. With the Align in X and Align in Y feature these charts can be aligned on the same data values. (See Figure 3)

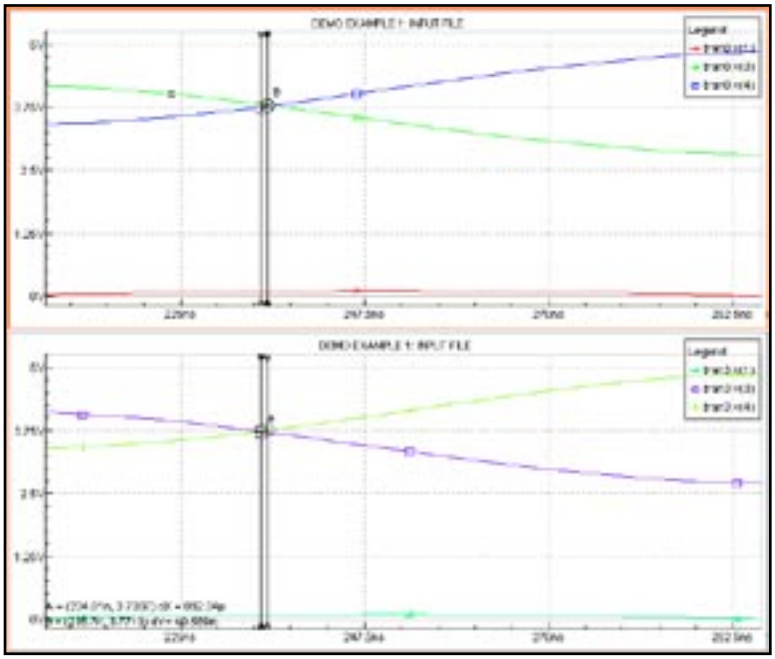

Figure 3 Example of alignment using "Align in X"

- Every editable object inside a chart has a context menu, allowing the user to edit, move, and delete the object
- User interaction with chart has two mode of operation. A zoom mode for the manipulation of the visible data area and an interactive mode for the manipulation of the objects in the charts.
- Single point Data Markers can be placed on Smith, Polar and Histogram Charts for easier annotation of traces. (See Figure 4)
- The user interface remembers the placement of all dialogs and toolbars between sessions and restores them on restarting the application.
- Automatic chart layout of charts into predefined layout modes (Vertical, Horizontal, Tile, Page and Palette Modes)
- Marching waveforms from the simulator are supported in the interactive and Batch modes of the ***SmartSpice*** simulator.
- The Histogram chart has user definable bin widths using the histogram tool to bin the data prior to adding it to the display.
- Single value measurements (Y value, Average, Root Mean Square, Derivative, Min and Max values) for all traces in a chart can be measured simultaneously in the Single Measurement dialog.
- Management of all application defaults is handled by a single dialog utilizing a property tree style layout as seen in Internet Explored or Netscape Navigator.
- Display Dialog is separated into two windows Data Viewer and Trace Legend. The Data Viewer is used to select and add data to the chart, the Trace Legend is responsible for removing trace from the chart and their position in the Chart Legend.
- Deleted data can be deleted from the data Cache as soon as it is deleted or by the Clear Cache action

Conclusion

This simulation standard has discussed the post processor ***SmartView*** and has identified some of its key attributes. By utilising these key attributes, the user's productivity and efficiency can be improved in addition to the reduction of computation time delvered through ***SmartView 's*** inherent integration into the ***SmartSpice*** framework.

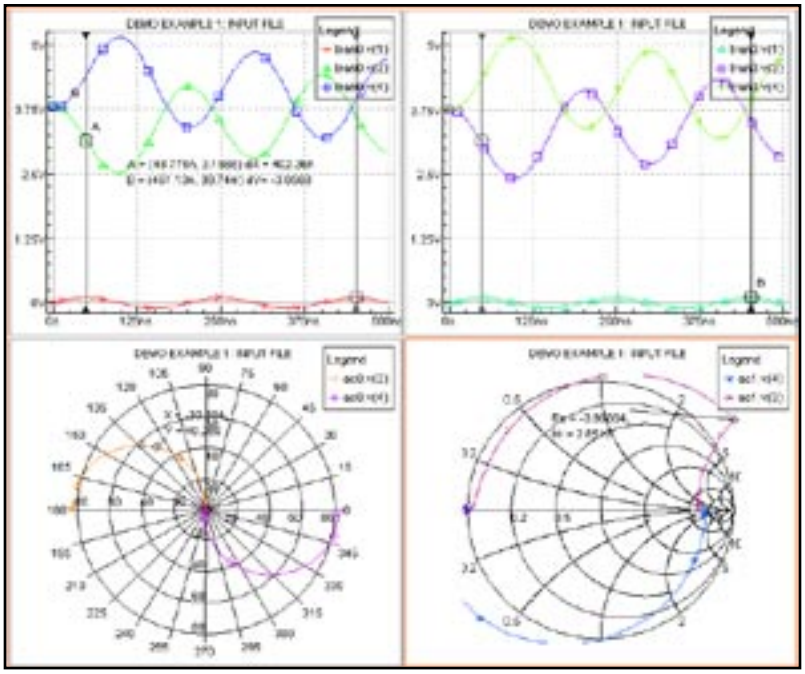

Figure 4 Example of an AB across two charts and data markers in a Smith and Polar chart.

Calendar of Events

January

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21 ASP DAC - Japan
22 ASP DAC - Japan
Electronic Imaging, Santa Clara CA
23 ASP DAC - Japan
Electronic Imaging, Santa Clara CA
24
25
26
27 Design Con - Santa Clara, CA
28 Design Con - Santa Clara, CA
29
30 EDS Fair - Japan
31 EDS Fair - Japan

February

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21 Int'l Forum on Semicon. Tech. - Japan
22 Int'l Forum on Semicon. Tech. - Japan
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26 Compond Semiconductor Outlook - San Diego, CA
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Bulletin Board

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Hints, Tips and Solutions

Colin Shaw, Applications and Support Engineer

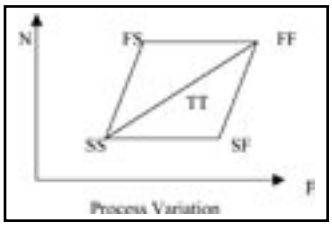
Q. How can I get an accurate FFT spectral plot in *SmartSpice* ?

A. The transient simulation uses an adaptive time-stepping algorithm depending on the change in the circuit waveforms (dV/dT). This means the simulated waveform consists of uneven time steps (more time points are required round a rapidly changing voltage to define the detail). If the normal .FFT command is used, these varying time points need to be interpolated to a regular set to allow the FFT plot to be created.

The act of interpolation leads to a distortion of the true waveform which gives an artificially high noise level (~ -60dB). ***SmartSpice*** includes an option "fft_accurate" which allows the regular time point to evaluated back on the true waveform and therefore reduce the distortion component. The output waveform now shows a noise level of about –280dB which is below present standard measurement accuracy levels.

Q. How do I simulate across process corners in one simulation deck ?

A. The foundry often provides a process model library where parameters are sectioned in terms of their change to variations in say the definition of the N & P type devices in the CMOS process. This is the typical SS, SF, FS, FF & TT that people refer to when showing the process spread in electrical performance. For each of these variations there should be an entry point in the model library and then you can include the following syntax flow in the main deck:




```
.LIB mod1.lib
.ALTER
.DEL LIB mod1.lib
.LIB mod2.lib
```

Q. I can create a single voltage waveform source but can I create a single modulated input voltage source?

A. Yes you have the capability in ***SmartSpice*** to create a complex waveform in PWL file (piecewise linear) but for a modulated waveform this would be to complex a file for all the data points required. We have the capability to do 2 forms of modulation, Amplitude and Frequency for a single element.

Frequency Modulation:

```
.param fm =200K
V1 1 0 sffm(1 1 2k 10 fm )
.tran .05U 50m ;sweep fm 5k 20k 5k
```

Amplitude Modulation:

```
.param fr =20K
V1 1 0 am(1 1 1k fr 0)
.tran .05U 50m ;sweep fr 5k 20k 5k
```

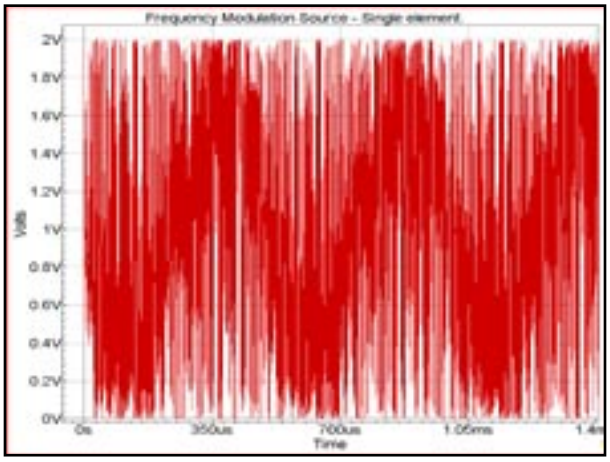


Figure 1. Frequency modulated source - single element.

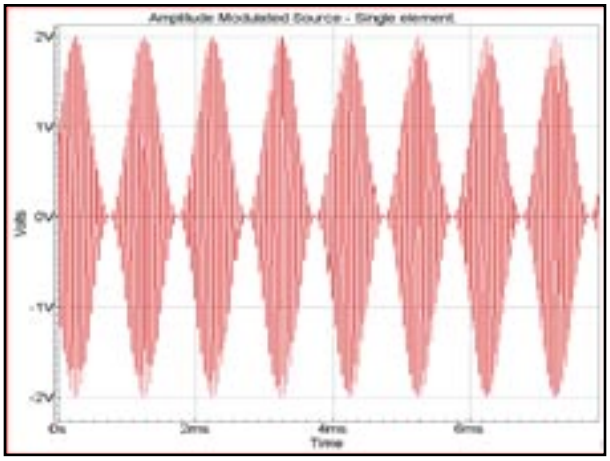


Figure 2. Amplitude modulated source - single element.

Call for Questions

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