Exact2: Interconnect Parasitic Capacitance Simulator from Silvaco

Introduction

Exact2 from Silvaco is a sophisticated, physically-based simulation tool for calculating semiconductor interconnect capacitance values. Its purpose is to build a capacitance coefficient database that is usable by any layout parasitic capacitance (LPE) tool.

In order to accurately calculate these coefficients, it is important that the actual interconnect structures are accurately defined. ***Exact2*** achieves this by means of an internal, physically-based 3D process simulator. Included with the process simulator is an internal 3D field solver that calculates the capacitance for each device layer and structure combination. ***Exact2*** also creates capacitance rule files readable by any LPE tool through the use of analysis script files, written in ***LISA*** code which is, Silvaco's dynamic scripting language.

This article presents an overview of ***Exact2's*** features, capabilities, and use.

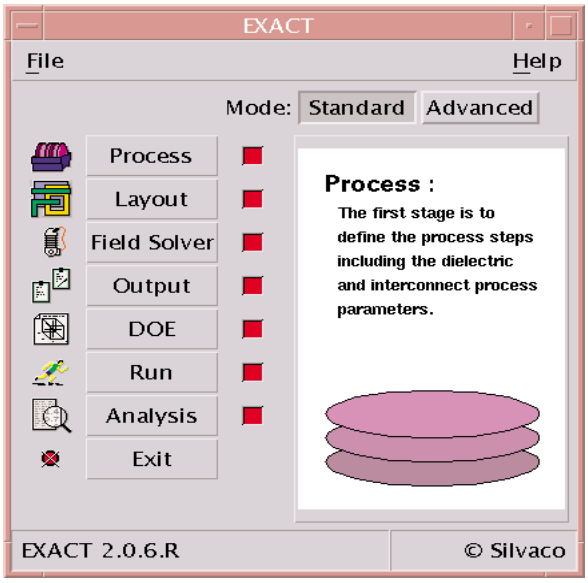

Figure 1. Main ***Exact2*** Window.

Overview of Selected Features and Improvements

Exact2's 3D process simulation engine simulates many varieties of arbitrarily complex interconnects, including:

- multiple dielectrics including low-k materials
- multiple metal materials
- non-planar dielectrics
- damascene processing
- conformal deposition
- lithographic effects

Exact2's processing options are geometric etches and depositions, or realistic etching and deposition. An integral optical solver takes photolithography effects into account. All the relevant properties of realistic etching, deposition, and optolithographic models are defined by the user, including the isotropic degree of an etch or deposition, the critical intensity at which the photoresist will develop, and finally the wavelength, aperture, and shape of the exposure source. ***Exact2*** simplifies worst case modeling and data analysis by applying powerful statistical analysis to geometry dependent parasitics.

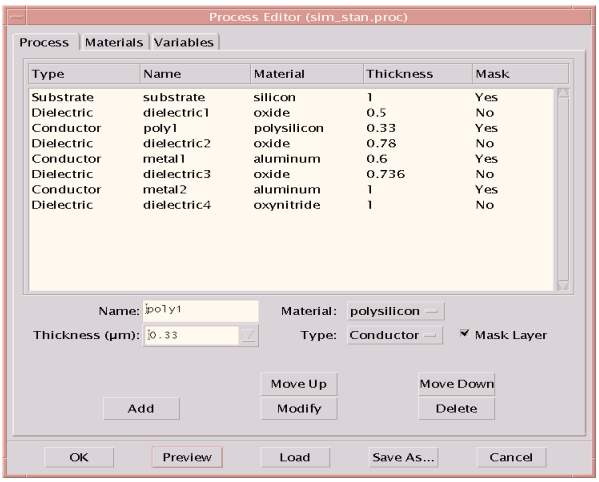

Figure 2a. The Process window allows each layer of a process to be defined.

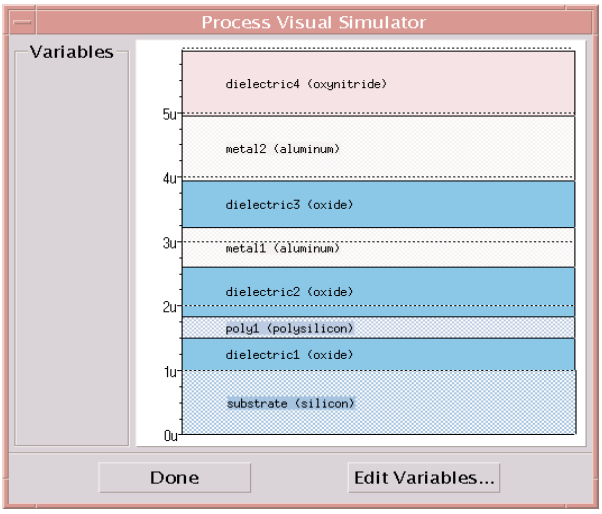

Figure 2b. Preview of the process definition created by the process window.

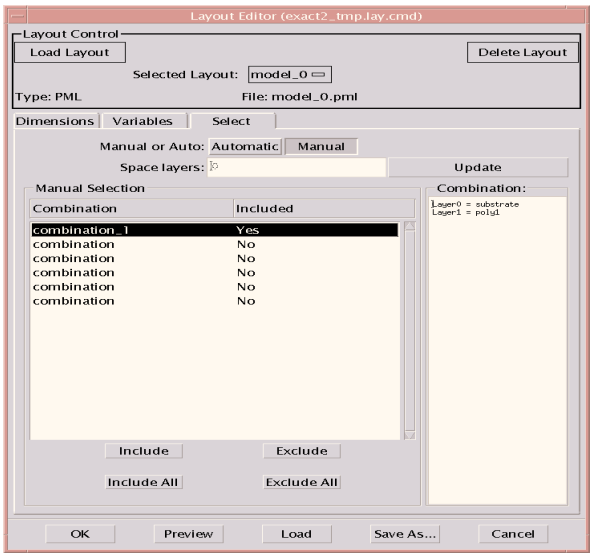

Figure 3a. The Layout window allows layout files to be added and defines the combination of layers to be included in the simulation.

A new paramaterized layout editor and support for the Language for Interfacing Silvaco Applications (***LISA***) enhances custom layouts and analysis capabilities. ***LISA*** also enhances ***Exact2's*** open interface by outputting data to formats recognized by any chip-level LPE tool. In addition, custom equations are easy fit to raw parasitic data.

Exact2 dramatically improves upon its predecessor in several ways, including:

- Extensive use of tool tips throughout the application
- Detailed output logs simplify easier development of models
- Results are now saved in plain text for easier retrieval
- Greater control over the simulation domain
- Simpler, more robust GUI
- Intuitive approach to results analysis
- Plain text configuration files make it easy to run ***Exact2*** without the GUI

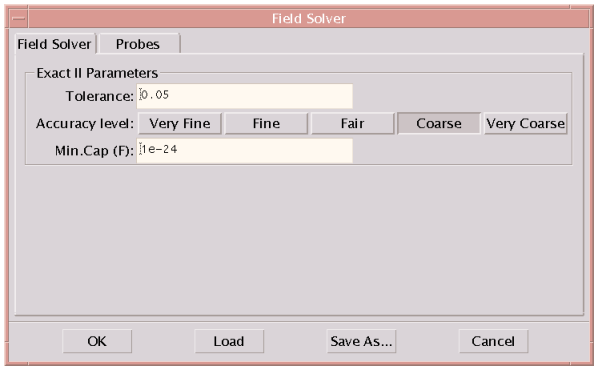

Figure 4. The field solver used by ***Exact2*** can have different accuracy levels that control the final capacitance extracted.

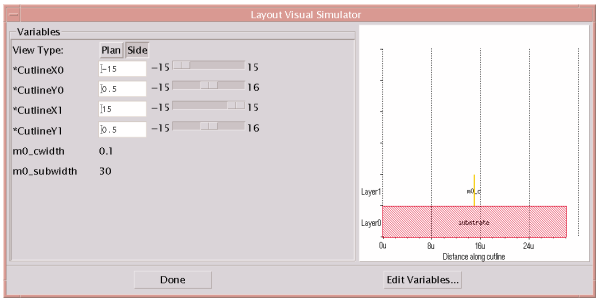

Figure 3b. When a layout file is loaded this preview window shows the shape of the layer and the variables that allow its dimensions to be changed.

The Seven Stages of An *Exact2* Experiment

Figure 1 is the main start-up screen of ***Exact2's*** Graphical User Interface (GUI). There are generally seven distinct stages that comprise a complete ***Exact2*** experiment, and these stages are identified in Figure 1 by the corresponding icons running down the left hand side of the main screen.

The stages are briefly described as:

1. **Process definition**: define layer thickness and film properties
2. **Layout definition:** choose test structures, layouts, and layer combinations for each layout
3. **Field Solver:** control internal field solver attributes
4. **Output**: specify the result parameters and save location
5. **Design of Experiments (DOE)**: describe the upcoming experiments
6. **Run**: perform the calculations and generate the database
7. **Analysis**: analyze, manipulate, and visualize the generated database

Exact2 features two modes of operation (Figure 1): standard and advanced. The following descriptions are based on the standard mode of operation.

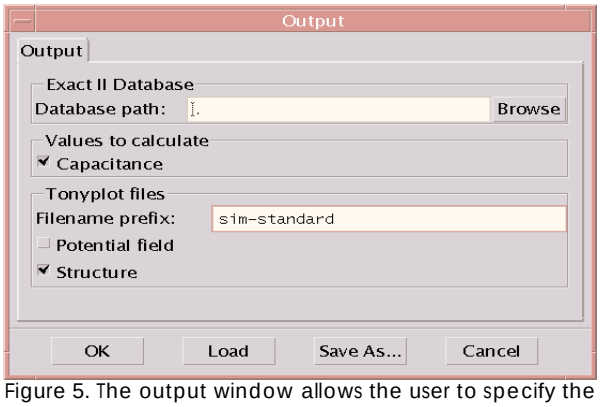

Figure 5. The output window allows the user to specify the database path and output data to be saved.

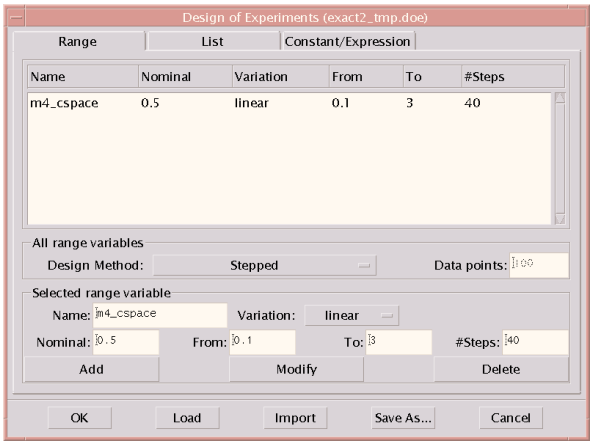

Figure 6. The design of experiment GUI is used to control the variation of any layout and/or process variable.

Stage 1: Process definition

User-specific process are easily created with the process GUI (Figure 2a). This screen is used to input layer definition and thickness, material properties, and parameter variables. Subjects are brought to the foreground by clicking on the relevant folder heading (Figure 2a). The user may preview and modify the created process stack at any time by simply clicking on the preview button in the process GUI. Figure 2b shows a preview of the process defined in Figure 2a.

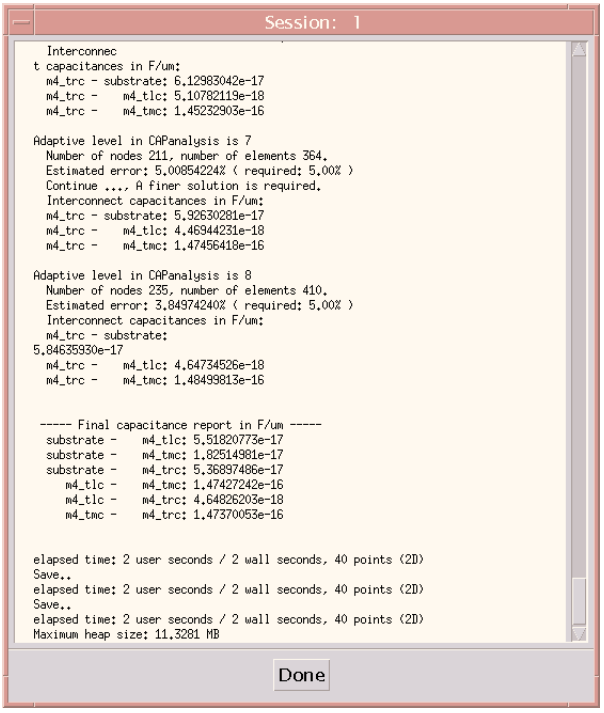

Figure 8. The Run time output window shows the output from the 3D process simulator and the field solver capacitance extraction for the current job.

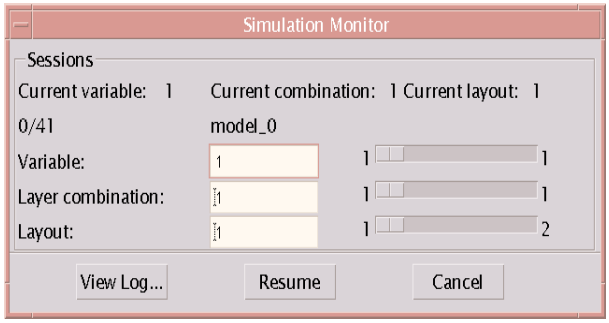

Figure 7a.When the experiments are ready to be executed this Run window shows the status of the submitted jobs.

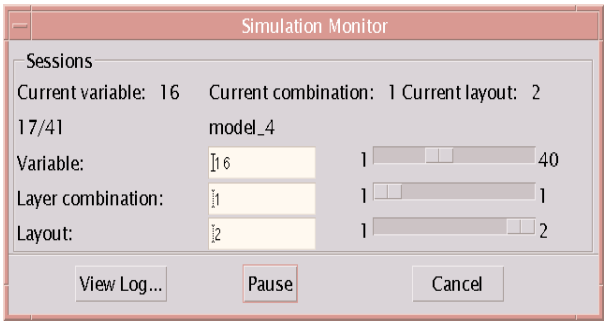

Figure 7b. Simulation monitor window as it appears during the simulations.

Stage 2: Test structure (layout) definition

Once device layers are identified, the test structures' mask layout designs are quickly chosen and added to the experiment with the layout GUI (Figure 3a). Test structures are easily parameterized and defined in any combination of selected layers. For example, combination 1 is chosen (left side of Figure 3a) that corresponds to process layers (right side of Figure 3a). Users can preview the test structure in both plan and side views (Figure 3b), and cut lines through any part of the structure are easily implemented.

Stage 3: Field solver

Figure 4 shows the field solver GUI. This screen is used to adjust of some of the field solver attributes, such as tolerance and accuracy levels. The probes function specifically chooses of which pairs of wires will serve as targets of capacitance calculation. The probes function is brought to the foreground by clicking on the respective folder heading.

Stage 4: Output

Figure 5 shows the output GUI that is used to specify the calculation targets and output directories.

Stage 5: Design of experiments (DOE)

This GUI (Figure 6) define the experiment using predefined variables from the process and layout stages. The only required values are the initial value, final value, number of data points, and the variation form.

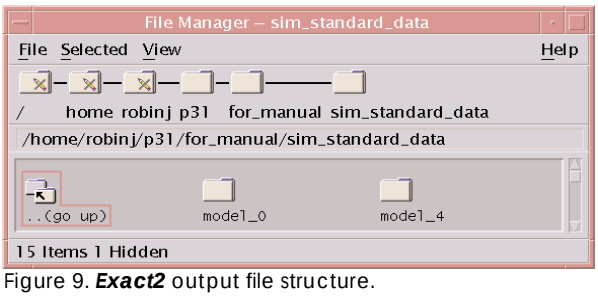

Figure 9. ***Exact2*** output file structure.

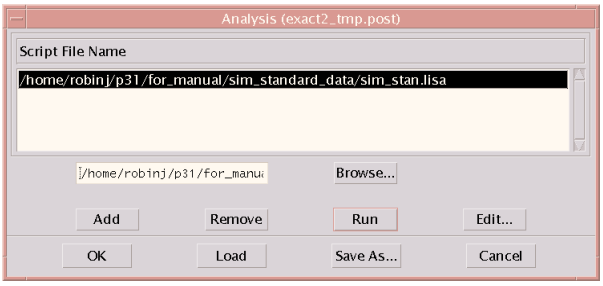

Figure 10. Analysis window used to load and run scripts to export data files that export the capacitance rule files.

Stage 6: Run

The run stage performs all user-specified calculations and reports the status and progress back to the user. Figure 7a shows the screen before calculations are performed, while Figure 7b shows the status further on into the simulation. Clicking the **View log**... button (Figure 8) launches the simulation run time output dialog box, which is useful for reference and error checking. ***Exact2*** outputs a file structure and files that contain each layer's simulation results, as well as their respective combinations and sessions (Figure 9). Users must check out result files before viewing or modifying them..

Stage 7: Analysis.

After a successful simulation run, the script files need to analyze, manipulate, and visualize the generated database are loaded with the analysis GUI (Figure 10). A selected script file appear in a text box to the left of the **Browse**... function and is into the Analysis stage by clicking **Add**. The **Run** button executes any highlighted file. The **Edit**... button launches the built-in text editor for quick modification to the script file(s).

A simple script file that outputs capacitance data in both comma separated values (CSV) format and in ***TonyPlot*** format, is shown below. CSV files are easily loaded into many data management and spreadsheet programs, such as Microsoft™ Excel™. The resulting ***TonyPlot*** file is shown in Figure 11.

```
db = DatabaseLoad(".");

extract_name("m0Ctotal_sub", "substrate", "m0_c");
extract_name("m4Ctotal_sub", "substrate", "m4_tmc");
m0_combinations = {1};
m4_combinations = {1};

table_m0 = select(db, "model_0",
m0_combinations,{"m0_subwidth"}, {"m0Ctotal_sub"});
column_scalar_op(table_m0, "m0Ctotal_sub", table_m0,
"m0Ctotal_sub", "*", 1e15);
save_table(table_m0, CSV, "m0_a.csv");

table_m4= select(db, "model_4",
m4_combinations,{"m4_cspace"}, {"m4Ctotal_sub"});
column_scalar_op(table_m4, "m4Ctotal_sub", table_m4,
"m4Ctotal_sub", "*", 1e15);

save_table(table_m4, CSV, "m4_sim_stan.csv");
save_table(table_m4, TONYPLOT, "m4_sim_stan.str");
```

Conclusion.

Exact2 brings flexibility and simplicity to the creation of a comprehensive and accurate interconnect capacitance database. ***Exact2*** creates the database by means of a 3D process simulator and 3D internal field solver in one self-contained package. ***Exact2*** files are easily imported into LPE tool formats through the use of the ***LISA*** scripting language

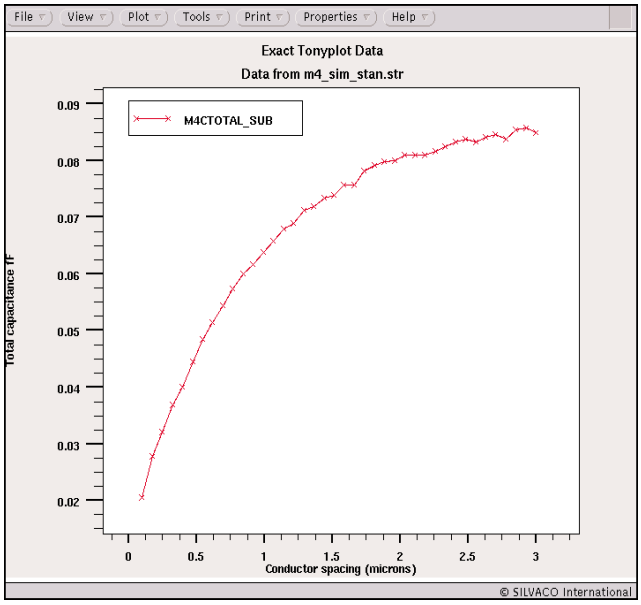

Figure 11. Simulated total capacitance versus conductor spacing.