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The Effect of Carrier Spilling on SRP Accuracy

Introduction

Spreading Resistance Profiling (SRP) retains its popularity in the semiconductor industry by an inexpensive means of capturing dopant profile information. However, device engineers often incorporate SRP data into process simulation studies without properly considering SRP's many limitations. Failing to account for these limitations jeopardizes the reliabilty of the data and potentially lead designers to incorrect conclusions about a device.

This article briefly reviews the general concepts behind spreading resistance profiling and analyzes the impact of carrier spilling on both simulation studies and SRP accuracy. Finally, this article demonstrates how to reliably and accurately into a simulation study. The purpose of this article is not to discourage the use of SRP measurements, but rather to offer suggestions for using SRP measurements in order to obtain the most accurate results.

SRP Measurements

Before proceeding to SRP's limits, it is necessary to revisit the concept of spreading resistance and how SRP data is collected. Spreading resistance (SR) is the resistance associated with a divergent current passing between electrodes on the surface of a semiconductor material. This quantity is determined by applying a known current between the electrodes on the surface of the sample and measuring the voltage drop between the probes. The spreading resistance value is calculated with Ohm's law. For a two probe system, the resistivity of the material is determined with the following expression, where *a* is an empirical quantity related to the effective electrical contact radius [1]:

$$\rho = 2R_{SR} \cdot \alpha$$

Figure 1 is a simple two-probe spreading resistance measurement system. A structure's carrier concentration profile is measured by angle lapping the sample and making a series of SR measurments along the bevel. Profile depth is calculated as a function of the bevel angle. Correction factors are used to convert the spreading resistance values to carrier concentration levels. The technique of using spreading resistance to measure the thickness of diffused layers and impurity profiles was originally proposed by Mazur and Dickey [2] in 1966.

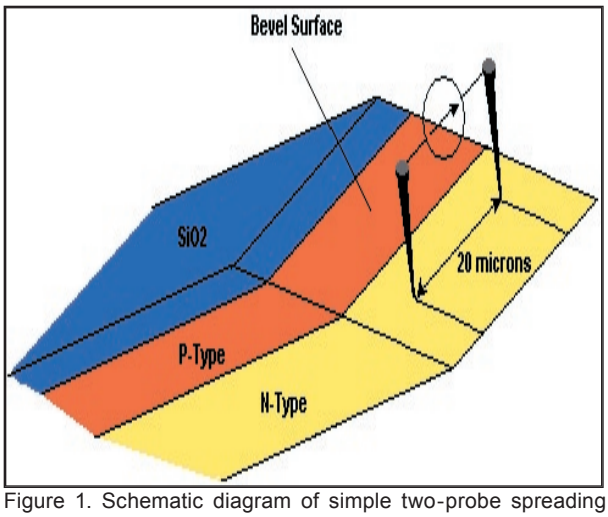

Figure 1. Schematic diagram of simple two-probe spreading resistance measurement system.

Carrier Spilling

The total phenomena that affect SRP reliability are too numeous to describe here. This article focuses on carrier spilling, as it most directly impacts how SRP data is used within a simulation study.

Carrier spilling is a term that describes the diffusion of free carriers from a region of high concentration to a region of low concentration within a device structure. This is best understood by observing two blocks of equally-doped semiconductor as they are brought together. Figure 2 shows dopant and carrier concentrations within two

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neighboring regions of uniformly-doped, N- and P-type silicon. Free carriers migrate across the PN junction from one region to another until the diffusion force is countered by the electric field created by the immobile dopant atoms.

How does carrier spilling affect the accuracy of SRP measurements? To answer this complicated question, we use a process simulation to obtain a better understanding of what is happening inside the structure. It is important to remember that SRP's measure the *carrier* concentration profile and not the actual dopant profile. The dopant profile at operating temperatures is immobile, the carrier profile is not. The very process of beveling the structure affects the boundary conditions of the system and alters the measured carrier concentration.

Figure 3a shows the net doping profile and total carrier profile for a simple gaussian PN junction. The total doping profile indicates a significant amount of carrier spilling in this structure. Carrier spilling from the P-region is dominant, and this places electrical junction (EJ) deeper in the structure than the metallurgical junction (MJ). Figure 3b shows the same profiles for the structure after moving down the bevel, resulting in the removal of 1.75 microns of silicon. Due to the higher concentration of holes, EJ remains deeper than MJ, but here a substaintial portion of the free holes has also been removed. This reduces the effect of forward spilling and results in a slightly shallower (2.78 um vs 2.93 um) electrical junction depth. Continuing this analysis, Figures 3c and 3d show the structure after the removal of 1.8125 um and 1.875 um of silicon, respectively. Enough free holes have been removed from the structure in Figure 3c so that EJ is less than MJ, while in Figure 3d the concentration of electrons in the bulk of the structure overwhelms the remaining holes and eliminates the electrical junction altogether.

S.M Hu [3] originally identified the described carrier spilling effect. He performed an extensive study of the carrier spilling effects on SRP profiles and identified three situations in which carrier spilling could affect the electrical junction at the bevel. Figure 4 presents a diagram taken from [3] that shows the effects of carrier

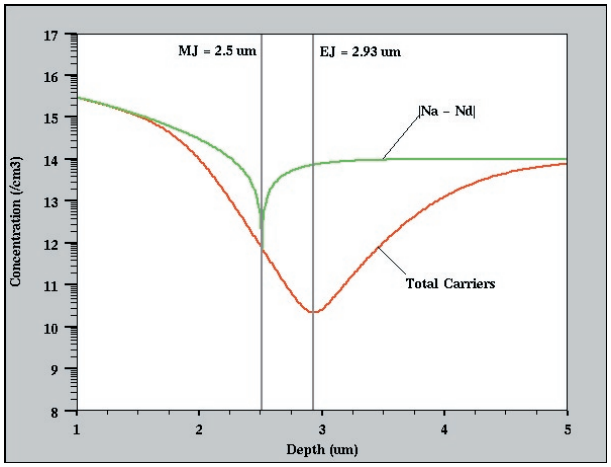

Figure 3a. Net doping and total carrier concentration profiles for simple gaussian PN junction.

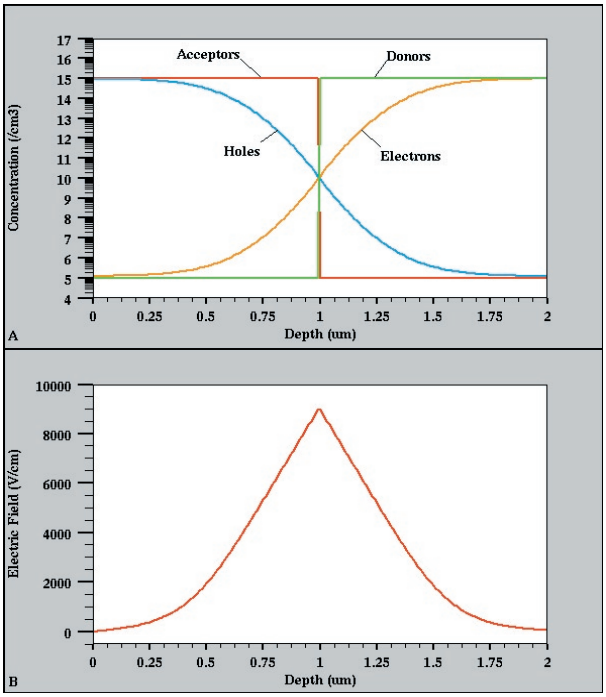

Figure 2. Dopant and carrier concentration profiles in neighboring p- and n-type silicon regions.

spilling on a beveled sample with a diffuse P-layer on a lightly doped N-type substrate. The electronic junction on the bevel is substaintially different from that in the bulk. This is what the spreading resistance is supposed to measue. This diagram is a two dimensional view of the effects in Figures 3a-3d. Hu [3] later went on to study the effects of doping profile shapes, surface charge, and doping levels upon carrier spilling effects.

Comparing Simulated Profiles to SRP Data

While the effect should not discourage the use of SRP measurements, it *must* be properly accounted for when comparing measured and simulated data. This effect prohibits the direct comparison of SRP data to the dopant profiles predicted by a process simulation package like

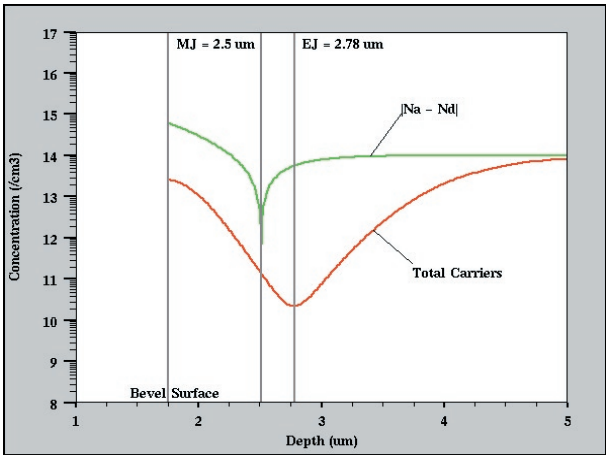

Figure 3b. Net doping and total carrier concentration profiles for simple gaussian PN junction after 1.75 microns of silicon has been removed.

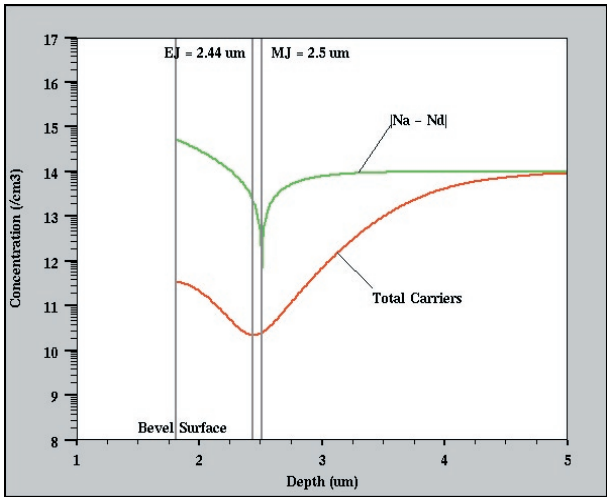

Figure 3c. Net doping and total carrier concentration profiles for simple gaussian PN junction after 1.8175 microns of silicon has been removed.

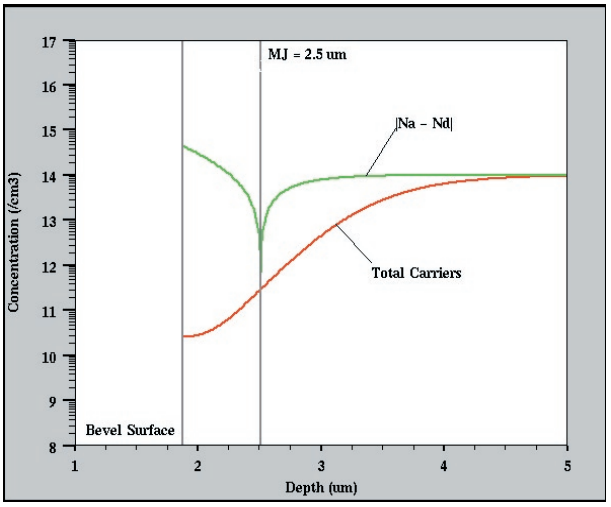

Figure 3d. Net doping and total carrier concentration profiles for simple gaussian PN junction after 1.875 microns of silicon has been removed.

Silvaco ***ATHENA***. First, spreading resistance measures carrier concentration, not dopant concentration. Secondly, users must consider the removal of free carriers due to the beveling process. Silvaco has developed an extraction routine that automatically mimics the SRP process and generates an "SRP-like" carrier profile.

The correct syntax for extracting an SRP profile from a simulated structure is as follows:

```
extract name="SRP" curve(depth, srp
  material="silicon" mat.occno=1\
  x.val=0.5) outfile="srp.dat"
```

A full description of the above syntax is found in Chapter 5 of the *VWF Interactive Tools User's Manual, Vol. 1*. It is also a predefined extraction routines that is available through ***DeckBuilds'*** Extraction menu. Figure 5 illustrate the effectiveness of the SRP extraction routine by comparing the spreading resistance profile predicted by ***ATHENA*** to actual SRP data taken from the source/drain region of an NMOS device. An excellent fit is achieved between the simulated and experimental SRP curves.

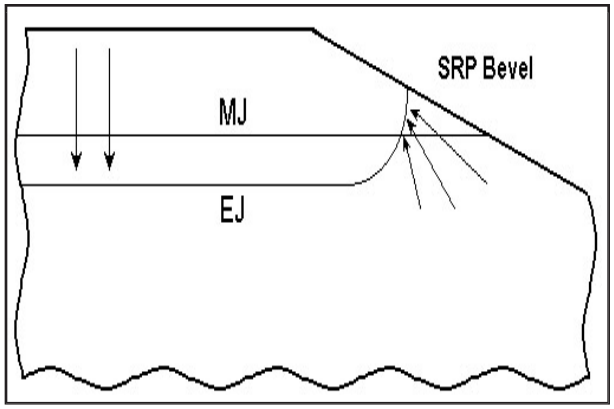

Figure 4. Two-dimensional cross section of beveled PN junction sample showing the qualitative effects of carrier spilling on a diffused p-layer in a lightly-doped n-type substrate.

Summary

This article presented a brief review of spreading resistance profiling and discussed the effects of carrier spilling on the accuracy of SRP measurements. A full discussion of the all the phonomena affecting SRP measurements was not provided. It is *highly* recommended that any engineer who regularly incorporates SRP data into a simulation study reviews the work Hu [3] and others in an effort to better understand the strengths and weaknesses of the spreading resistance measurement process.

References

[1] S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era Volume 1: Process Technology*, Lattice Press, Sunset Beach, CA (1986).

[2] R.G. Mazur and P.H. Dickey, "A Spreading Resistance Technique for Resistivity Measurements on Silicon," J. Electrochem. Soc., **113**, 255 (1996).

[3] S.M. Hu, "Between Carrier Distributions and Dopant Atomic Distribution in Beveled Silicon Substrates," J. Appl. Phys., **53**, 1499 (1982).

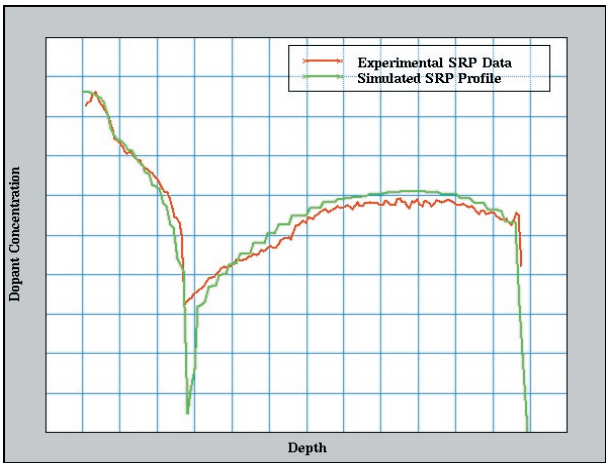

Figure 5. Comparison of simulated and measured SRP profiles for the source/drain region of a NMOS device.