Hints, Tips and Solutions

Colin Shaw, Applications and Support Engineer

Q. How do I make my long simulation more memory efficient ?

When you run a long simulation time analysis the evaluated time points are normally all held in memory until the end time is reached. All the data is then written out to the output rawfile. This means a large amount of system memory can be used up and also has to be tracked. If in the input deck the line ".OPTIONS RAWPTS=300 POST" is included then as soon as the maximum number of points is reached given by "RAWPTS=300" then all the vector data is saved to the raw data output file and the memory is free to be re-used. In this way the output rawfile is incrementally increased in size every time this limit is reached. The memory required by the simulation run is therefore reduced, and with less memory to manage, the simulation is run faster. This is particularly useful on the PC platform where some of the memory is required for the operating system and RAM size is less than 1Gig.

Q. What is the difference between .MODIF & .ALTER for simulation run variance ?

The .ALTER is used to globally change the circuit topology like slotting in another sub-circuit or changing a component. This change in the circuit is like submitting a new deck and can be incorporated in a distributed system among a group of computers to get maximum utilization of the resources. The .MODIF is more for changing parameter values associated with a model etc.

Q. My simulation fails with no convergence what extra information can I obtain ?

The spice simulation of a circuit is based on a good model of the elements and sensible circuit construction. If you include the line ".OPTIONS EXPERT" you will get a lot of reporting turned on showing model card parameter evaluation and floating nodes of the circuit. It would be sensible to cut down the simulation time before turning this option on to save too much duplication of the errors everytime they are encountered. This reporting gives the user more information to construct a better simulation deck. Commonly the model construction can be at fault and this option allows the user to go back to his model provider with highlighted problem areas. The other common problem is having an isolated section of circuitry without a DC path to ground. This can happen if a section of circuitry is connected only through a set of capacitance elements for example. Here the user will need to add conductance to ground to these nodes to allow spice to achieve a DC solution .OPTIONS DEPATH =<val> .The spiceusr1.pdf in chapter 2.12 contains options broken up into categories like convergence and we welcome any customer feedback on the manual information.

Q. I kill my SmartSpice program but the license is not available in Linux ?

When you invoke ***SmartSpice*** you can run it in the Foreground or the background by use of the "&" character at the end of the command line. Programs run in the background return the prompt straight away to the invoking window, programs run in the foreground wait for the completion of the program to return to the prompt. If the program is run in the foreground and then <cntrl>"C" is done the operating system still holds onto the process hence License is not available. To put a process into the background the <cntrl>"Z" should be done AND then the command "bg" to place in the background and the system will release the process. The License is therefore available for the next version of ***SmartSpice.*** (There is a License time-out feature but this will take a while to release the License)

Q. I know SPICE is an Analog simulator but can I generate a digital source ?

There are 2 steps to generating a digital source, first the waveform timing and second the pulse train of "0"'s and "1".

A SPICE input deck example is:

Digital source config.

```
* PWLFILEDESC.
.param tri=150ps tfi=150ps
* PWLFILEDESC format is:
*  ( datatype start delay  vlow vhigh  fall
rise )
* datatype= 1 - time current pairs, = 2
time voltage pairs
*
vin inp 0  pwlfiledesc( 2  0  3ns  0v  3.3v
'tri' 'tfi' ) pwlfile test3.dat


vcc 0   vss    dc -3.3v
m1 2  inp  vss  vss  pm  w=32u l=1.6u
m2 2  inp  0    0    nm  w=10u l=1u
C1 2 0 0.01f
```

```
.MODEL  NM    NMOS   LEVEL    = 49
.MODEL  PM    PMOS   LEVEL    = 49

.tran 0.1ns 50ns 0.1ns
.print v(inp) v(2)
.temp 125
.option nomod
.END
```

and the referenced file (test3.dat) contains the digital string "010110010"

What noise analysis can I do on my circuit in *SmartSpice*?

There are 3 ways to take account of noise in your circuit. First there is the traditional .NOISE analysis used to calculate the noise of each component. From there the spectral density is obtained and the integrated noise over the specified frequency range used to calculate the output and the input referred noise. Second there is the .TRAN NOISE which calculates the noise contributions of each circuit node and solves the stochicometric set of equations for each time point in the transient analysis. And finally there is a new spice element "N" introduced in ***SmartSpice*** 2.3.8.C, and higher, to allow users to inject noise at a particular circuit node. This noise is in addition to the element sources of noise and allows for contributions like substrate referred noise from other parts of the circuit and general circuit succeptability to external noise sources.

Q. My long simulation run consumes all resources and then freezes ?

This happens when you use a PC system with less than 1Gig of RAM or a small amount available hard disc space and a very long simulation time recoding all circuit node activities. A new feature ".OPTIONS SAFEMODE" was introduced to warn of this happening and it stops the simulation when either the hard disc space or the available memory gets below 50Megs. It is then up to the user to close other programs and free more resources or continue at risk running out of space. The other ways are to limit the simulation time to something more reasonable or limit the vectors that are saved rather than having everything saved even circuit nodes that are not critical. To do this instead of the ".SAVE ALL" you can use 2 pre-defined macros to record vectors from part of the whole circuit.

Xx - defines

Q. My simulation fails because SmartSpice cannot find a binned model, what does this mean ?

Normally when a MOS model is extracted for a range of devices it is scaleable over the range of device geometries i.e. it is a continuous varying function over the required

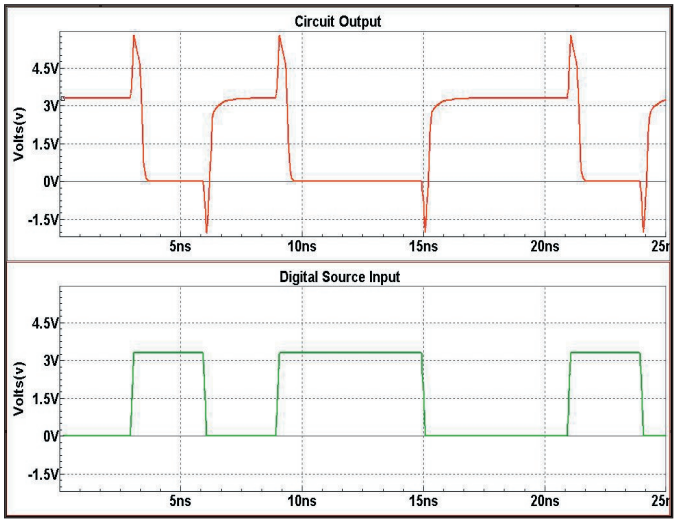

Figure 1. Digital source - input and circuit output.

operating region for all device geometries. Sometimes there is too much variation in the output characteristics to be covered by one continuous model parameter set e.g. "straight" and "dog-bone" layout designs which contain very different electric field patterns. The total operating region is therefore broken up into sub-sections and a model produced for each of these subsets of device geometry. This is a binned model where each region is a different set of model card values for a smaller range of device properties like width, length and temperature. In this way a group of model card parameter sets can be used to cover a wide variation in say gate width and length variations not possible from a single scaleable model. In the simple case these bins are ranges of Width and Length transistor geometries that say what model card parameter set should be used. The only problem with this approach is a discontinuity at the boundary of one model set to another and can be thought of as trying to approximate a curve with a set of straight lines. Your error is because the device geometry is not covered by any of the specified ranges in the model library. Typically the binned model will have a model name of say nch.1, nch.2, nch.3 etc. and you device geometry is not allowed for in the say Lmin to Lmax range of any of these binned model sections.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

Phone: (408) 567-1000 Fax: (408) 496-6080

e-mail: support@silvaco.com

Hints, Tips and Solutions Archive

Check our our Web Page to see more details of this example plus an archive of previous Hints, Tips, and Solutions

www.silvaco.com