# UFSOI Version 7.0 (UFPDB Version 2.0) Model Released in *SmartSpice*

## Introduction

Version 7.0 of the University of Florida Silicon-On-Insulator (UFSOI), released in 2002, is now available with Silvaco SmartSpice by setting LEVEL to 21. ***SmartSpice*** uses version 7 by default, but versions 4.5, 5.0, 5.0 rev 1.0, and 5.0 rev 6.0 are still available through resetting the VERSION and REVISION parameters.

## Model Features (prior to version 7.0) [1]

The UFSOI is a physical, charge-based, and process-based SOI MOSFET model that has evolved from the basic modeling of thin-film devices. The charge modeling is physically linked to channel-current modeling. All terminal charges and their derivatives are continuous for all bias conditions. The UFSOI model includes both NFD/PDB (Partially Depleted Bulk) and FD (Fully Depleted) models, which are set with the BODY parameter in version 6.0 and later. In previous versions, FD and NFD models were selected with NFDMOD parameter:

| BODY | model |
|---|---|
| 0 | FD |
| 1 | NFD/PD |
| 2 | Bulk-Si |

Table 1. BODY values (version 6.0 and later).

| NFDMOD | model |
|---|---|
| 0 | FD |
| 1 | NFD |

Table 2. NFDMOD values (previous versions).

The other parameters are process-based and are directly related to the device structure and material properties. This model is charge-based in order to ensure charge conservation and proper accounting for all transcapacitances. The model is extended to account for an accumulated charge in the body that can drive a floating-body mode dynamic bipolar effect in all regions of operation. There is optional accounting for LDD and LDS.

Additional, recently-added physical effects are:

- polysilicon-gate depletion
- inversion-carrier energy quantization
- GIDL/GISL (version 6.0 and later)
- narrow-width effects
- junction tunneling (NFD/PD model)
- RSCE/halo effects (NFD/PD model)
- carrier-velocity overshoot (version 5.0 and later)
- Account for hot-carrier effects on the channel thermal noise (version 5.0 and later)

Temperature dependence and accounting for self-heating are implemented in both models, without the need for additional parameters.

## A Unified PD/Bulk-Si Model

In Version 6.0, the NFD model is expanded to serve as a unified **process-based compact model** for PD SOI and Bulk-Si MOSFETs that use a single, small set of process-related parameters. This feature, enabled by the process-basis of the model, **allows direct performance comparison of the two mainstream CMOS technologies** without ambiguities in device structure [2].

Figure 1 shows the predicted current-voltage characteristics of PD/SOI and bulk-Si MOSFETs. This reflects the unified feature of UFPDB, and stresses the higher currents and kinks in the PD/SOI characteristics that result from the floating-body effect. The sub-threshold characteristics of both models are compared in Figure 2. The same set of model parameters was used for both devices.

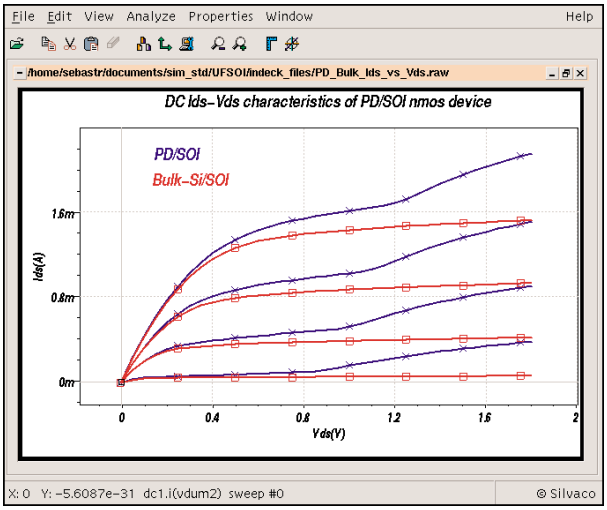


Figure 1. Ids vs Vds characteristics in PD and Bulk-Si mode of the UFPDB model.

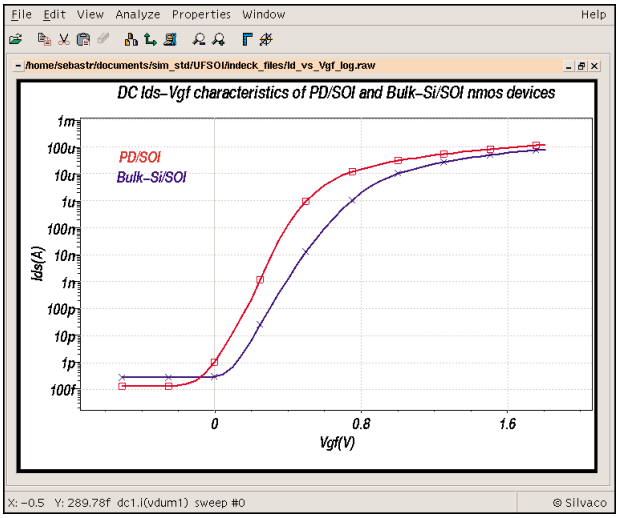


Figure 2. Subthreshold characteristics in PD/NFD and Bulk-Si mode.

The bulk-Si option internally ties the substrate to the body, sets the back-gate oxide thickness to near-zero, and updates the substrate density to reflect the bulk-Si doping. In the Bulk-Si mode, the substrate becomes the well, and this charge reflects the source/drain-junction areal capacitance. In this case, the device has four terminals and the command line in the netlist, like any other MOSFET device, becomes:

```
Mxxx ND NGF NS <NB> ...
```

## Improvements in version 7.0 [3]

Version 7.0 includes the upgraded UFPDB version 2.0 model that includes gate-body tunneling current ($I_{tung}$ in Figure 3), exchange energy for inversion carriers, a strained Si/SiGe-channel option, and allowance for arbitrary gate dielectric (KD parameter). With these upgrades, the model is applicable to CMOS devices scaled to the bulk-Si limit (Lgate ~ 50 nm).

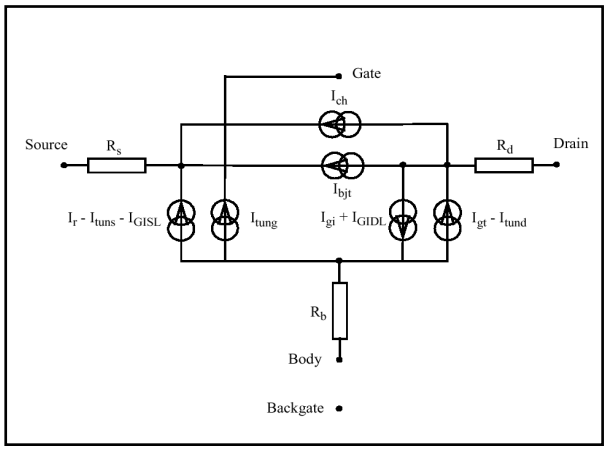


Figure 3. The static UFSOI model.

The current sources in the static model are :

- $I_{ch}$ : channel current
- $I_{bjt}$ : parasitic bipolar effect
- $I_r$: recombination current
- $I_{gi}$ : impact ionization current
- $I_{gt}$ : thermal generation current
- $I_{tund}$ : drain/body tunneling current
- $I_{GIDL}$ : Gate Induced Drain Leakage current
- $I_{GISL}$ : Gate Induced Source Leakage current
- $I_{tuns}$ : source/body tunneling current
- $I_{tung}$ : gate/body tunneling current

Gate-body tunneling current is only important to floating-body PD/SOI devices (Figure 4), so the feature is selectable only in NFD/PD model. Indirect valence band-conduction components are included that depend on both bandgap narrowing and channel quantization. The modeling is valid for all inversion and accumulation conditions and is applicable only for N+ polysilicon gates on NMOS devices, and P+ polysilicon gates on PMOS devices. This effect is taken into account by setting MOX parameter different from 0 (Table 3)

| Parameter | Description | Default | Typical |
|---|---|---|---|
| MOX | Electron effective mass (normalized to free electron mass) in gate dielectric (0 for no gate-body tunneling current) | 0.0 | 0.36 |

Table 3. Gate-Body tunneling current related parameter.

The following parameters are used for smoothing the Igb (gate-bulk) current. Default values are typically used.

| Parameter | Description | Default |
|---|---|---|
| SVBE | Smoothing parameter for gate-body current in inversion region (0 for no current) | 13.5 |
| SCBE | Smoothing parameter for gate-body cu rent in accumulation region (0 for no current) | 0.04 (NMOS)<br>0.045 (PMOS) |
| FFACT | Factor for gate-body current smoothing in accumulation region | 0.5 (NMOS)<br>0.8 (PMOS) |

Table 4. Gate-Body tunneling current smoothing parameters.

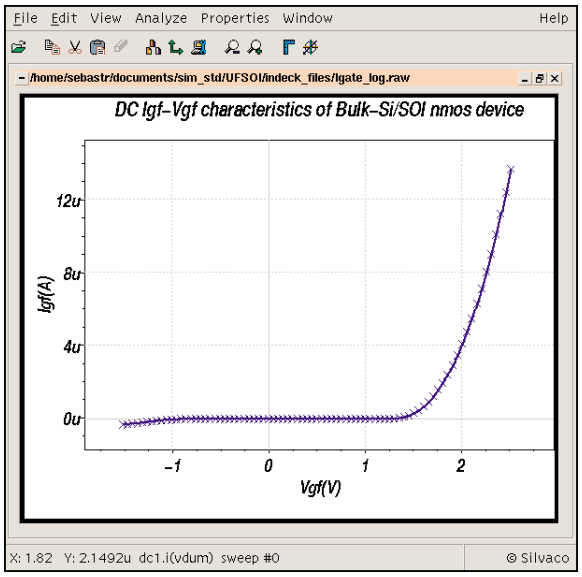


Figure 4. Itung vs Vgate characteristic.

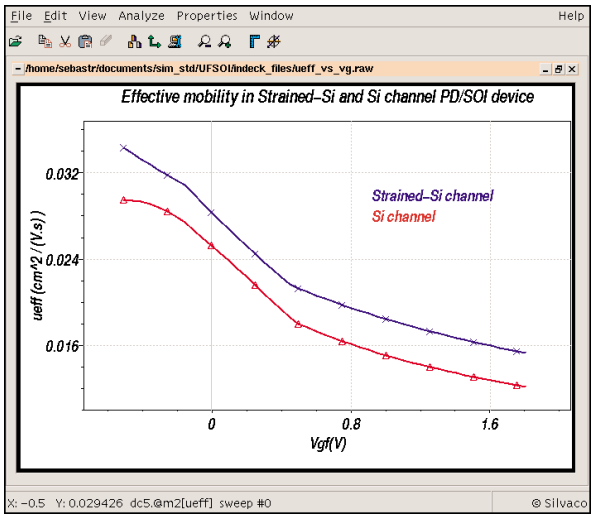


Figure 5. Field-effect mobility with strained- and unstrained-Si channel on a L = 60nm device.

Strained-Si channel property is a consequence of the pseudomorphic nature of a Si film on a SiGe layer. The deposited Si layer conformd atom-by-atom to the underlying SiGe lattice pattern and results in an enhanced-mobility device (Figure 5). The strained-Si option in UFSOI Version 8.0 is selected by setting the DEG parameter to the correct value and is deselected by setting DEG to zero (default value, cf table 5). This effect has an impact on other parameters (VO, VSAT, U0 and NBL to control threshold voltage) that must be evaluated in order to compare strained- and unstrained-Si devices.

A comparison of strained- and unstrained-Si channel SOI ring-oscillator with equivalent modelcards shows a period of 100ps for strained-Si, and 140ps for unstrained-Si (Figure 6).

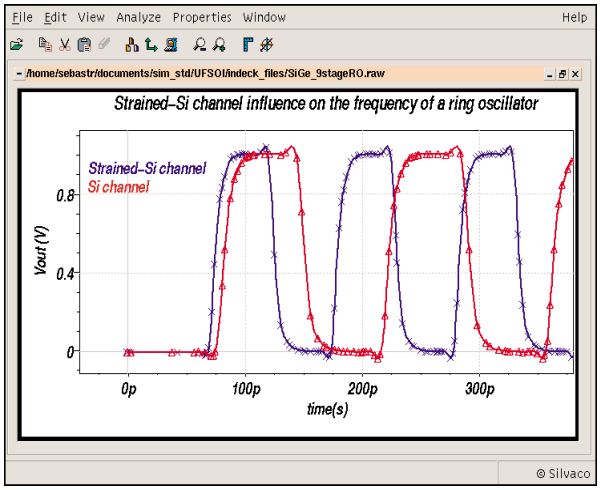


Figure 6. strained- and unstrained-Si devices ring oscillator.

Speed improvements are implemented in version 7.0. All of these improvements make the UFSOI model even closer to the real behavior of the device and make the simulation faster and more accurate. Strong and weak inversion threshold voltages are no longer iteratively calculated.

| Parameter | Description | Default | Typical |
|---|---|---|---|
| DEG | Bandgap narrowing in strained Si channel (0 for no SiGe) | 0.0 eV | 0.1 eV |

Table 5. Strained-Si channel related parameter.

## References

[1] UFSOI MOSFET MODELS (Vers. 6.0), User's Guide, SOI group, University of Florida, June 2001.

[2] J.G. Fossum, "A Unified Process-Based Compact Model for Scaled PD/SOI and Bulk-Si MOSFETs", MSM 2002, Univ. Florida, april 2002.

[3] UFSOI MOSFET MODELS (Vers. 7.0), User's Guide, SOI group, University of Florida, June 2002.