

# Simulation Standard

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## Simulation of Single-Event Effects in FinFETs Using the *ATLAS 3D* Device Simulator

### Introduction

A great deal of recent industry attention has focused on the use of non-planar multi-gate device structures in future generation MOS devices that feature channel lengths below about 50 nm [1-3]. The devices are based upon silicon-on-insulator (SOI) substrates, and employ three-dimensional (3D) structures that achieve fully depleted operation with near-ideal, sub-threshold slopes. Like their single-gate planar counterparts, these new SOI devices contain isolated channel regions. The transient charge injection from ionizing radiation events, including so-called "single events," can change the body potential of SOI MOSFETS and initiate transient transistor action [4-5]. This article illustrates the use of *ATLAS 3D* Device simulations to examine the impact of charge injection in these highly scaled 3D device structures.

### Device Structure

Fully depleted SOI devices have long been of interest. However, the scalability of the single-gate devices have so far been limited by silicon thickness control, as well as the need for ultra thin silicon and/or buried oxides. Double gate devices, which have a gate on both the top and the bottom of the channel, often overcome these limitations [6], but process integration issues limit the practical implementation of devices with high transistor densities. Two proposed 3D-device structures are each a variation of the double gate device: the FinFET essentially turns the double gate device on its side [1], while the tri-gate device uses a thin gate oxide on three sides of the device, instead of on only two [2]. Both devices use elevated (thicker) source and drain regions, and is contain electrically floating body regions. Figure 1 illustrates the device structure.

### Device Simulation

In a laboratory simulation, *ATLAS 3D* Device was used to simulate the impact of single-event charge injection into various regions of a FinFET device. Figure 2 is the

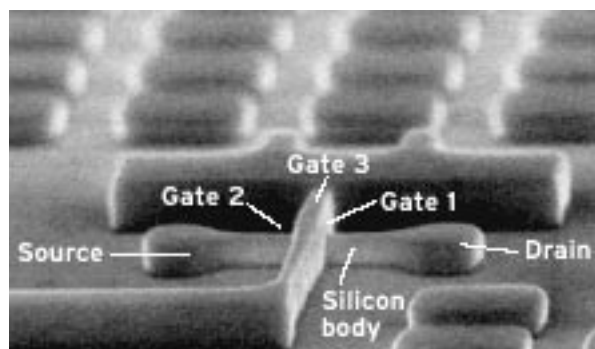


Figure 1. 3D device structure such as used for the FinFET [1] and Tri-Gate [2] devices. Figure from [3]. (COPYRIGHT IEEE Spectrum).

simulated device structure as viewed with *TonyPlot 3D* and *TonyPlot 2D*. The starting point was the device published by Huang, et al [1]. Device parameters were calibrated based on published physical dimensions with other parameters set to best match the published DC current values for the PMOS device. Appropriate changes were then made in order to create the NMOS device used in these simulations. The drain and source doping is  $N^+$  ( $1 \times 10^{19} \text{ cm}^{-3}$ ) and that of the body is  $P^-$  ( $1 \times 10^{16} \text{ cm}^{-3}$ ). The gate workfunction was set to 4.6 eV in order to achieve a reasonable threshold voltage of about 0.2 volts [7, 8]. The subthreshold DC - IV characteristics (Figure 3) indicate a slope of 64 mV/decade.

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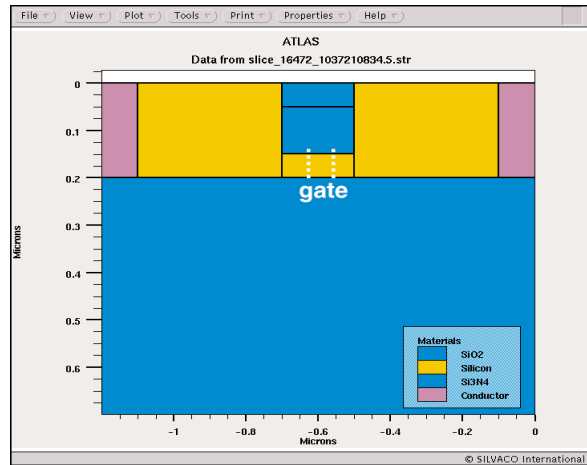
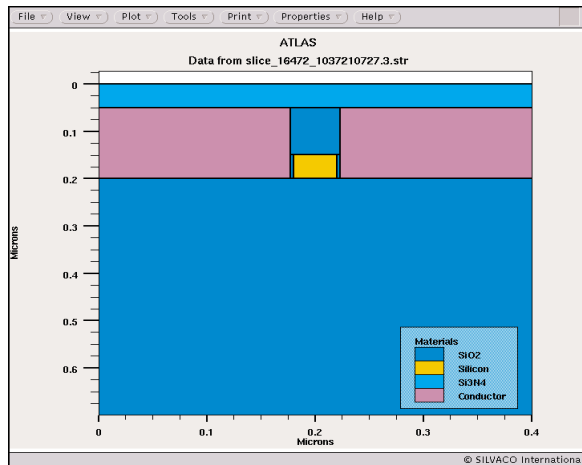
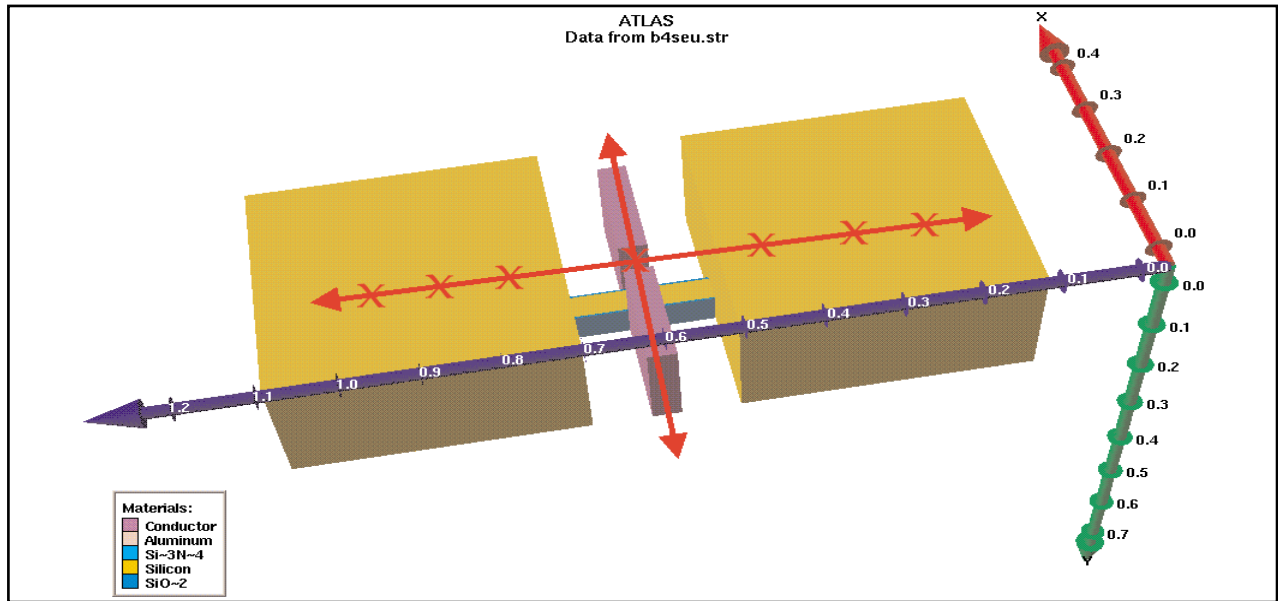


Figure 2. Simulated FinFET device. Top: 3D view with some layers not shown. The arrows show the cross section locations, the "X" 's show approximate locations for simulated "hits". Bottom left – cross section along the gate; bottom right – cross section along the channel from drain to source.

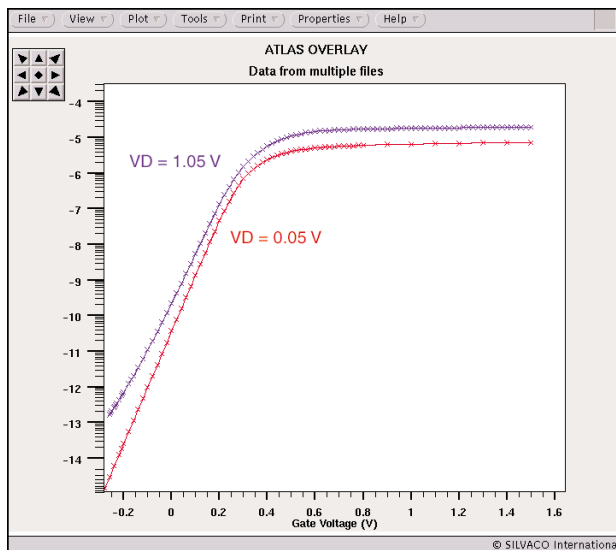


Figure 3. Simulated DC IV curves for the NMOS device. The subthreshold slope is 64 mV/decade.

The charge (electron-hole pair) generation is defined using the `singleeventupset` statement of *ATLAS 3D* Device [9]. The statement used for these simulations is (where the z-value of the entry and exit coordinates were varied for the different hit locations):

```
singleeventupset entry="0.1,0.0,0.2" \
  exit="0.1,0.05,0.2" radius=0.05 \
  density=1.e18 t0=4.e-12 tc=2.e-12
```

Two things worth noting:

- (1) the scale of the pulse's temporal profile is on the order of the carrier, which is the transit time across a biased junction (i.e. ~ 10 ps)
- (2) the spatial profile of this pulse would cause truncations of the generation region by the device active region physical limits in the body, as well as in some portions of the drain/source regions

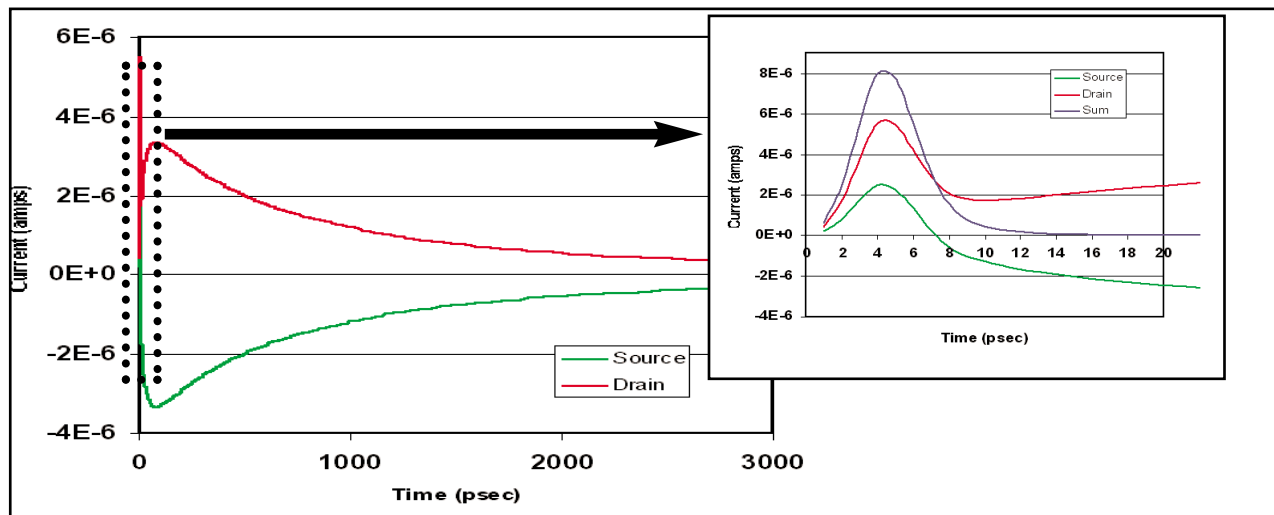


Figure 4. Drain and source currents for the hit to the body region. The insert shows a zoomed-in view of the initial time response due to the injected charge.

## Simulation Results

The FinFET device was biased with the drain voltage at 1.5V, and the gate and source voltages at 0V. In each case, a simulation was performed at various locations for the center of the charge injection track, perpendicular to the wafer surface. The axis of the hit location was simulated for the center of the body region, and for three locations in each in the drain and source regions. (Denoted by the X's in Figure 2, top).

### Case 1: Body Hit

After injection into the body region, a fast pulse is first observed in both the drain and source current (Figure 4). This represents the excess electrons created in the body as they cross the body-drain and body-source junction. The net-induced photocurrent is represented by the sum of the two current pulses (also plotted). Excess holes trapped in the potential well of the n-p-n structure raise the potential of the body region causing the body-source junction to become forward biased (Figure 5) and initiating transistor action. This accounts for the second, longer pulse in Figure 4. While the peak value of the second pulse is less than the first, the characteristic time scale is much longer (nanoseconds compared to picoseconds), and the associated charge (integral of the current) is greater than 50 times that of the initially deposited charge.

### Case 2: Drain and Source Hits

Generally for planar single-gate SOI devices of past and current generation devices ( $\geq 0.13 \mu\text{m}$ ), injection into the body is believed to result in the most pronounced device response since it most efficiently initiates parasitic bipolar action. There has been

some discussion about hits to the drain region also contributing [10] to device response. In the present simulated devices, the dimensions of the drain and source regions are comparable to the radial dimensions of the simulated charge track. Simulations were performed with the center of the track at three different locations within the drain and within the source relative to the body silicon region: at 0.3  $\mu\text{m}$ , 0.2  $\mu\text{m}$ , and 0.1  $\mu\text{m}$  away from the thin body region edge (Figure 2, top). The resulting drain currents for each case are plotted in Figure 6. The same trends are observed for both drain and source with the collection efficiency being somewhat less on the source side due to the lower junction bias.

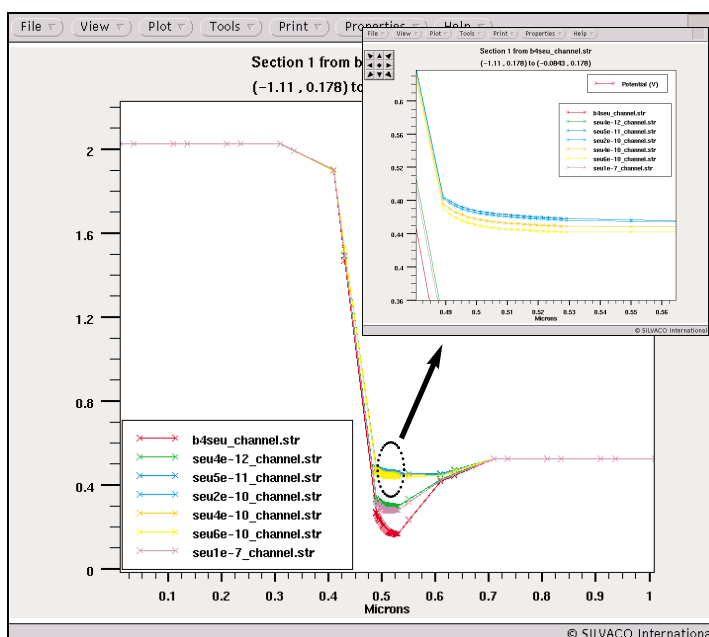


Figure 5. Potential distribution - evolution over time showing the body potential increase due to the charge injection. Plots are shown at times: pre-strike (b4), 4ps, 50ps, 200ps, 400ps, 600ps, and 0.1us.

In both cases, some holes generated in the drain (source) region are able to drift and diffuse to the body junction. The initial fast rise is carriers that are in and near the high field region of the junction, while the longer tail is dominated by diffusion to the junction. For a doping of  $10^{19}\text{cm}^{-2}$  in the drain, the minority carrier lifetime is on the order of 50 ps, and the diffusion length on the order of 0.35  $\mu\text{m}$ . It is for this reason that the initial current decreases as the hit location is moved away from the drain-body junctions from 0.1  $\mu\text{m}$  to 0.3  $\mu\text{m}$ .

Comparing the results from the drain/source regions (Figure 6, left) to that of the body (Figure 4), the former produces a comparable (or larger) device response. This is due to the small device dimensions compared to carrier diffusion lengths (allowing charge collection), and the larger volume of the drain/source silicon leading to increased volume for charge generation to drive the bipolar action.

### Conclusion

**ATLAS 3D** Device simulations are used to simulate the impact of single event charge injection into a sub-50nm FinFET device. Simulation results indicated that the injected charge is amplified by transient transistor action, and that the sensitive areas of such devices may include source and drain regions.

### References

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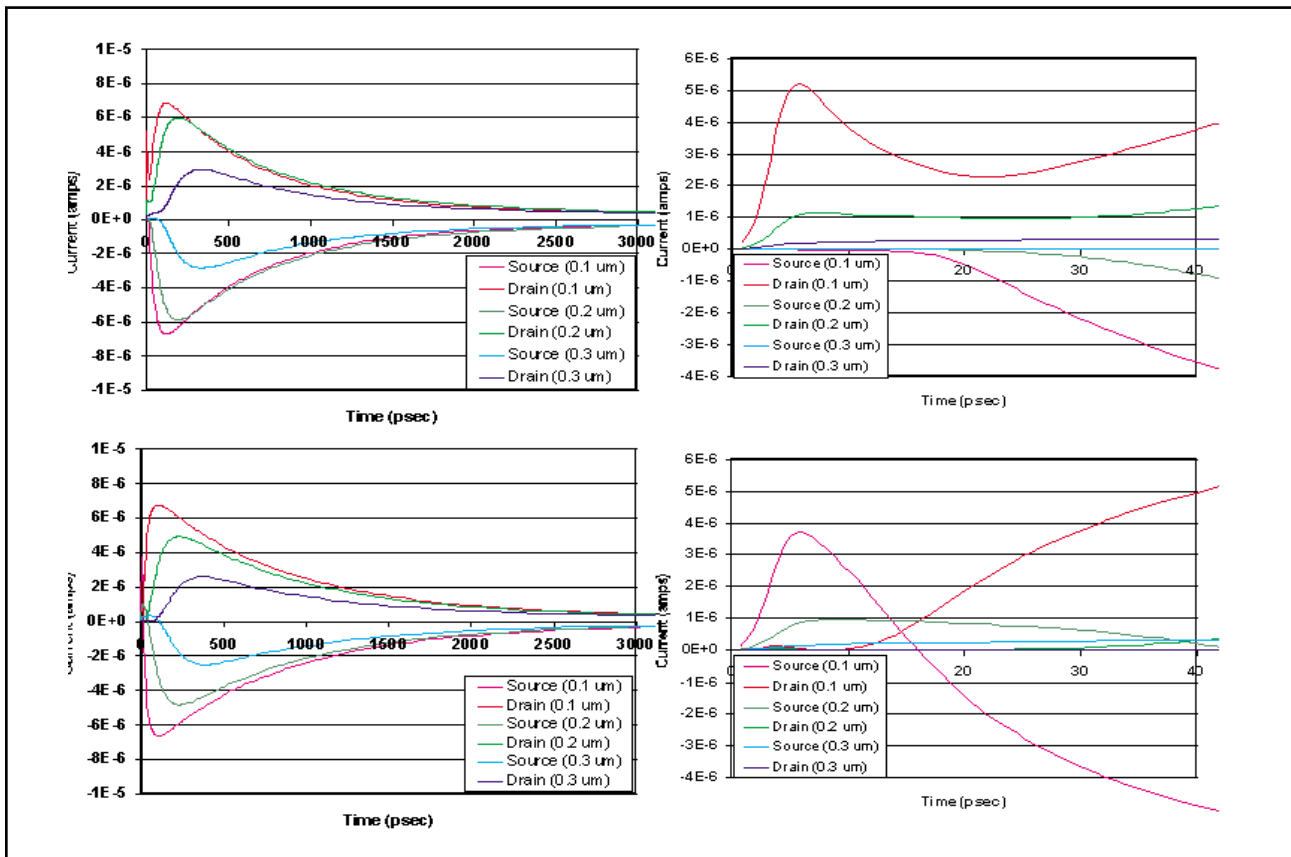


Figure 6. Drain and source currents for the hit to the drain region (top) and source (bottom) at three locations. Figures on the right show initial 40 picoseconds.