Simulation Standard

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RF CMOS Modeling Using *UTMOST III* AC (S-Parameter) Module

This article presents a high frequency SPICE model parameter extraction method for CMOS devices. Current compact MOS models are developed for low frequency applications and provide good fits for DC, conductances and intrinsic capacitances. However for the gigahertz frequency range external components have to be modeled and added to the compact model as macro model elements. The macro model presented in this article provides good results up to 10 GHz. ***UTMOST III*** MOS technology s-parameters (AC) module was used for data collection and modeling. The BSIM3v3.1 MOS SPICE model was used as the core model of the macro. The details of the RF macro and modeling method is described in two IEEE papers given as a reference at the end of this article. Our purpose here is to provide a practical application note for RF CMOS modeling.

The success of a RF macro model depends very much on the DC core model extracted for the MOS device. In particular the GM and GDS parameters should be modeled very well. The "s-meas" routine in the AC routines section of the ***UTMOST III*** MOS technology should be used for RF data collection. Proper probe and Network Analyzer calibration and "dummy" device measurements should take place before the actual device AC measurements. The DC bias conditions should be specified in the "Set Measurements" screen of the "s-meas" routine. (Figure 1.).

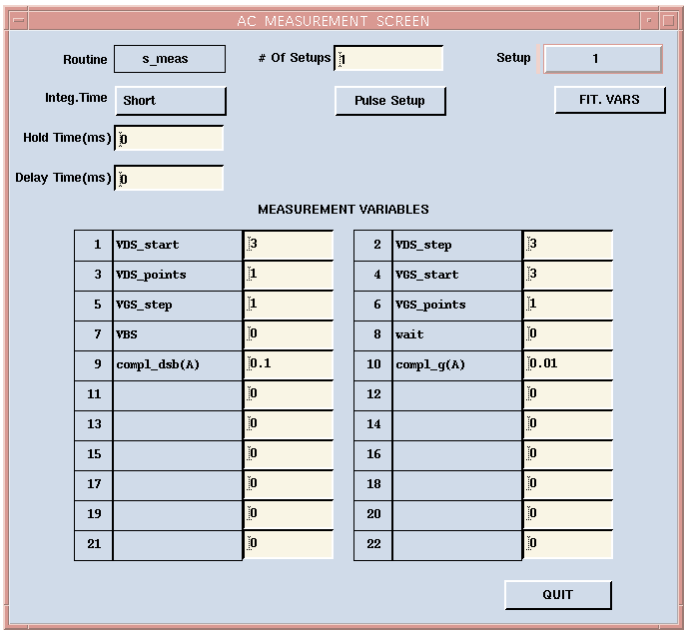

Figure 1. The Set Measurement Screen of the "s-meas" routine.

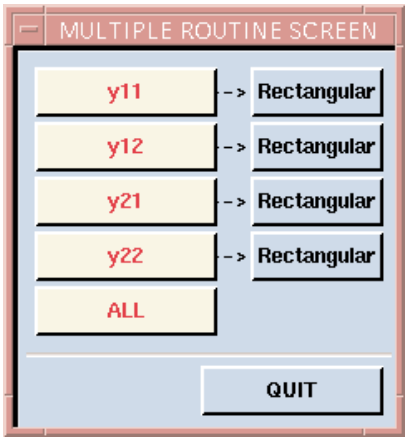

Figure 2. Multiple Selection Screen of the "y-plots" routine.

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The s-parameters of the MOS device should be measured for the specified frequency range (Figure 3). The measured data should be stored in the ***UTMOST III*** log file. The log file should be loaded and the results should be viewed using the "y-plots" routine. In order to see all four y-parameters the "Multiple Select" button inside the "Routine Control Screen" should be pressed and "ALL" button should be toggled until it changes color to red. (Figure 2.)

Once the RF data collection is complete the macro model should be loaded for optimization. The three files (netlist, control and model) of the macro model used in this example are given in Figures 4, 5 and 6 respectively.

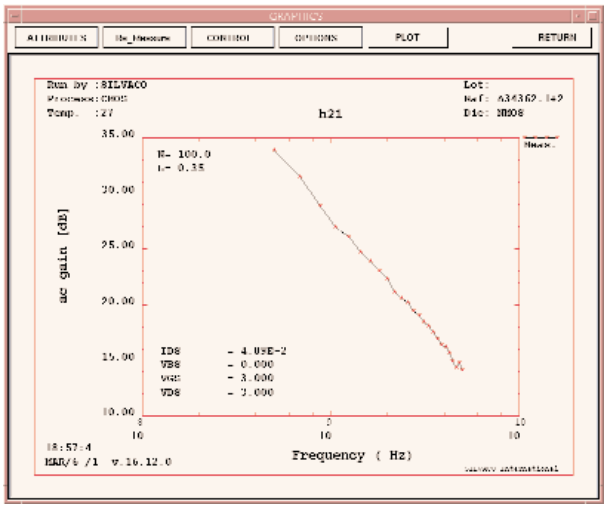

Figure 3. Gain of the MOS transistor measured with s-meas routine.

```
NETLIST FILE
VGS   5   0   3.00

VDS   6   0   3.00

VBS   9   0   0.00

VSS   7   0   0.00

M1 1 2 3 4 MMOD   W=1.0000E-04 L=3.500E-07
RG   5   2 75.74
RD   6   1 16.1
RS   7   3 1.1E-3
CGS 2   3 0
CGD 2   1 0
DSB 4   3 DSBM
DDB 8   1 DDBM
RDSB 8 4 132
RDB 8   9 132
RSB 4   9 132
```

Figure 4. The netlist file of the RF macro model.

```
*UTMOST INTERFACE
.OPTIONS TNOM= 27.00
*UTMOST INTERFACE
.TEMP      27.00
*UTMOST INTERFACE
.net VGS VDS lin 25    500000000.0    5000000000.0
*UTMOST INTERFACE
.print net S11
*UTMOST INTERFACE
.print net S12
*UTMOST INTERFACE
.print net S21
*UTMOST INTERFACE
.print net S22
*UTMOST INTERFACE
.OPTIONS GMIN=1.00E-18 RELTOL=1.00E-10 VNTOL=1.00E-06
ABSTOL=1.00E-12
*UTMOST INTERFACE
.OPTIONS NUMDGT=5
```

Figure 5. The control card file of the RF macro model.

```
.LIB TMP_MOD
.MODEL MMOD NMOS (
+ LEVEL   = 8.000000e+00  VERSION  = 3.100000e+00  TNOM   = 2.700000e+01
+ TOX     = 7.000000e-09   XJ       = 1.500000e-07   NCH    = 1.700000e+17
+ VTH0    = 4.628370e-01   K1       = 4.478257e-01   K2     = -2.256200e-02
+ K3      = 2.219889e+01   K3B      = -3.439966e+00  W0     = 1.366820e-06
+ NLX     = 2.567817e-07   DVT0W    = 0.000000e+00   DVT1W  = 0.000000e+00
+ DVT2W   = -3.200000e-02  DVT0     = 1.573282e+00   DVT1   = 4.624292e-01
+ DVT2    = -2.000000e-01  U0       = 5.339190e-02   UA     = 1.303231e-09
+ UB      = 3.000000e-19   UC       = 2.931232e-11   VSAT   = 9.923400e+04
+ A0      = 1.226818e+00   AGS      = 3.235326e-01   B0     = 2.074168e-07
+ B1      = 1.000000e-07   KETA     = -3.377960e-02  A1     = 0.000000e+00
+ A2      = 1.000000e+00   RDSW     = 1.125955e+03   PRWG   = 0.000000e+00
+ PRWB    = 0.000000e+00   WR       = 1.000000e+00   WINT   = 1.504420e-07
+ LINT    = 1.793858e-08   XL       = 0.000000e+00   XW     = 0.000000e+00
+ DWG     = -6.235501e-09  DWB      = 4.459600e-09   VOFF   = -1.500000e-01
+ NFACTOR= 1.058016e+00  CIT      = 0.000000e+00   CDSC   = 1.760576e-04
+ CDSCD   = 0.000000e+00   CDSCB    = 0.000000e+00   ETA0   = 1.647241e-01
+ ETAB    = 0.000000e+00   DSUB     = 5.696590e-01   PCLM   = 1.273635e+00
+ PDIBLC1= 6.371016e-03   PDIBLC2  = 1.000000e-05   PDIBLCB = 0.000000e+00
+ DROUT   = 5.913154e-03   PSCBE1   = 4.843489e+08   PSCBE2= 1.596200e-05
+ PVAG    = 1.905288e-01   DELTA    = 9.395578e-03   HDIF   = 3.000000e-07
+ MOBMOD = 1.000000e+00   PRT      = 0.000000e+00   UTE    = -1.500000e+00
+ KT1     = -3.143000e-01  KT1L     = 0.000000e+00   KT2    = 0.000000e+00
+ UA1     = 4.010000e-09   UB1      = -5.610000e-18  UC1    = -5.600000e-11
+ AT      = 3.300000e+04   NQSMOD   = 0.000000e+00   WL     = 0.000000e+00
+ WLN     = 1.000000e+00   WW       = 0.000000e+00   WWN    = 1.000000e+00
+ WWL     = 0.000000e+00   LL       = 0.000000e+00   LLN    = 1.000000e+00
```

```
+ LW     = 0.000000e+00  LWN      = 1.000000e+00  LWL    = 0.000000e+00
+ CAPMOD = 2.000000e+00  CGDO     = 1.935193e-10  CGSO   = 6.569662e-10
+ FC     = 5.000000e-01  CJ       = 0.000000e+00  CJSW   = 0.000000e+00
+ DLC    = 1.600000e-07  DWC      = 0.000000e+00  PRDSW  = -3.900000e+01
+ PVTH0  = -1.200000e-02 PVSAT    = 5.000000e+03  LKETA  = 1.400000e-02
+  )
.MODEL DSBM D (
+ LEVEL  = 3.000000e+00  W        = 1.000000e-04  L      = 6.000000e-07
+ JS     = 5.530000e-07  RS       = 3.510000e-07  CJ     = 5.292377e-04
+ PB     = 7.212762e-01  M        = 3.392038e-01  CJP    = 1.787730e-10
+ VJP    = 1.000000e+00  MJP      = 2.203447e-01  )
.MODEL DDBM D (
+ LEVEL  = 3.000000e+00  W        = 1.000000e-04  L      = 6.000000e-07
+ JS     = 5.530000e-07  RS       = 3.510000e-07  CJ     = 5.292377e-04
+ PB     = 7.212762e-01  M        = 3.392038e-01  CJP    = 1.787730e-10
+ VJP    = 1.000000e+00  MJP      = 2.203447e-01  )
.ENDS

.ENDL TMP_MOD
```

Figure 6. The SPICE model file of the RF macro model.

If you are not familiar with ***UTMOST III***'s macro modeling facility please refer to the ***UTMOST III*** *Extraction Manual Volume 2*, Appendix B: Macro Modeling with ***UTMOST***.

As can be seen from the netlist file in Figure 4 there are additional junction diode (drain and source to substrate) models. Also the external Gate , Drain and Source resistances were used. Even though the gate to drain and gate to source capacitances were added as additional elements, their values were set to zero and internal overlap capacitances were used instead. The substrate resistance network was kept simple and consists of only three resistors.

Some of the external macro model elements can be extracted directly from the measured y-parameters. For example:

```
Cgg = Abs [ Imag(Y11) / w ]

Cgd = Abs [ Imag(Y12) / w ]

Cgs = Cgd

Cgb = Cgg - Cgd - Cgs

Rg = Abs [ Real(Y12) / Imag(Y12)x(Imag(Y11)]

Rd = Abs [ ((Real(Y21)-Real(Y12)) / Imag(Y12)^2]

Rs = Abs [ (Real(Y11) / (Imag (Y11)^2) - Rg -
  (Cgd^2)/(Cgg^2) x Rd] x (Cgg^2) / (Cgs^2)
```

The measured or y parameters can be viewed in a table format. Press the “s-parameters” button in the system screen to view the s-parameters table.

The above equations are based on the assumption that the MOS transistor is operating in a linear region. As it is difficult to extract the substrate network resistance values, it is recommended to optimize those parameters directly on the measured data. For the details of the extractions and derivations of the equations please refer to the IEEE papers listed at the end of this article.

In this example the measured and simulated data provided a good match up to 5 GHz. (Figure 7.) The external elements of the macro were optimized on y-parameter plots using the global optimization technique. The region of interest can be defined by drawing an optimization box around the selected y-parameters. Certain external macro elements will be more dominant for modeling certain y-parameters. Therefore selecting the external elements for optimization and y-parameters where those elements will be optimized should be handled carefully.

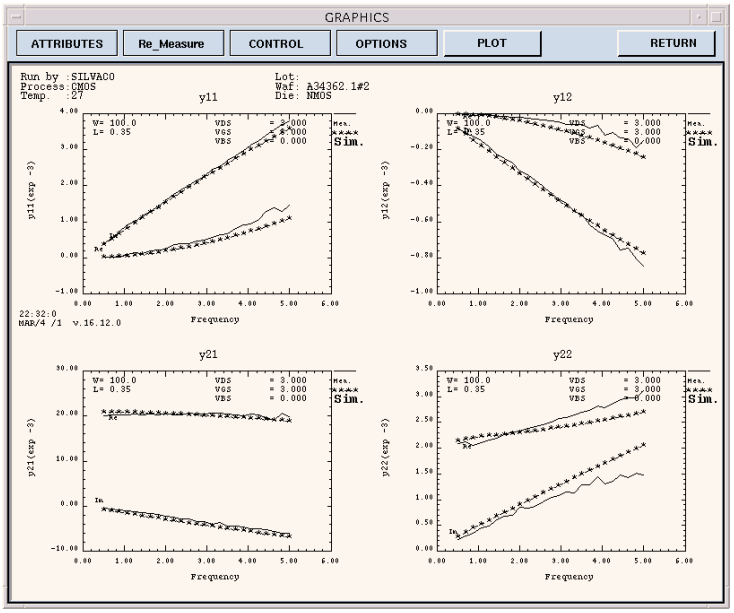

Figure 7. Measured vs. Simulated y-plots data.

References

[1] Accurate Modeling and Parameter Extraction for MOS Transistors Valid up to 10 GHz. IEEE Transactions on Electron Devices, Vol. 46, No 11, November 1999.

[2] MOS Transistor Modeling for RF IC Design. IEEE Transactions on Solid-State Circuits, Vol. 35, No. 2, February 2000.

New Improvements in TFT Models: Amorphous (Level=35) and Poly-Silicon (Level=36) TFT

Introduction

New improvements have been added to Shur models. These enhancements include self-heating effect and a new charge conservation model.

Self-Heating

The self-heating effect is a major feature for TFT which exhibit low thermal conductivity ([1],[2]). The self-heating is activated with SHMOD selector (model parameter). If this parameter is set to 1 and the thermal resistance is different from 0, an internal single thermal node and a thermal circuit are created. The thermal circuit includes a thermal resistance and a thermal capacitance in parallel.

Modified Device Declaration

Syntax

```
Mxxx nd ng ns mname <M> <OFF> <IC=vds, vgs>
+ <TEMP=val or DTEMP=val> <L=val> <W=val> <NRS=val>
+ <NRD=val> <AD=val> <AS=val> <PD=val> <PS=val>
+ <GEO=val> <RTH=val> <CTH=val> <NOSELFT=val>
```

New instance parameters:

RTH: Thermal resistance (deg. C / W). The default value is the model parameter RTH0.

CTH: Thermal capacitance (W.s/ deg. C). The default value is the model parameter CTH0.

NOSELFT: Selector to de-activated self-heating at device level. It overrides SHMOD model parameter. The default value is 0.

New Model Parameters

Parameter	Description	Units	Default
SHMOD (SELFT)	Self-heating selector	-	0
RTH0	Thermal resistance	$^oC/W$	0.0
CTH0	Thermal capacitance	$W.s/^oC$	0.0

New Output Device Variables

Parameter	Description	Units
TEMPNODE	Number of temperature node	-
TDEV	Device temperature when self-heating is turned on	deg. C
DELT	Device temperature difference when self-heating is turned on	deg. C

Characteristics

Curves Id-Vd exhibit different behavior according to parameters related to temperature. Whereas the curves show more saturation with DVTO model parameter (>0) than the curves without self-heating , the curves with DMU1 (<0) give less current and can lead to gds < 0 (Figure 1). This can be explain by the following equations:

$$Vteff = VTO - DVTO \cdot (temp - TNOM)$$

And

$$Tmu1 = MU1 + DMU1 \cdot (temp - TNOM)$$

Since the model parameter DVTO (>0) decreases the threshold voltage, the ids current increases. On the contrary, DMU1 (<0) decreases ids current since Tmu1 (FET mobility) decreases.

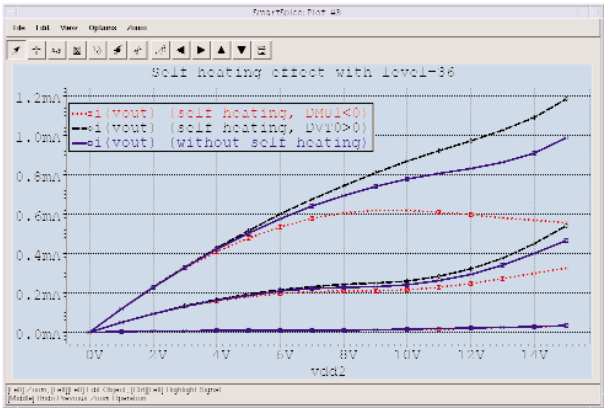

Figure 1 : Self-heating effect with level=36

New Charge Conserving Model

In Shur capacitance model, the charges qgs and qgd are numerically calculated from the capacitance capgs and capgd. This leads to problems of charge non-conservation. The charge based approach announced in [3] is presented here. This charge conservating model is selected with CAPMOD=-2 and is based on Leroux's charge model (level=15). This new model also allows speed up (factor 2.5) and simple extraction (only one parameter).

New Model Parameter

Parameter	Description	Units	Default
TC	Characteristic temperature	K	390

Description of the Charge Model

This charge model is the same as in level 15 (Leroux's model). Please refer to ***Smartspice/UTMOST*** manual for more information (equations, parameters,...) about this model charge.

New Output Device Variables

When CAPMOD = -2, the following output variables are available:

Parameter	Description	Units
QG	Gate charge	C
QD	Drain charge	C
QS	Source charge	C
CGGS	Derivative of Qg over Viss	F
CGGD	Derivative of Qg over Vidd	F
CDGS	Derivative of Qd over Viss	F
CDGD	Derivative of Qd over Vidd	F
CSGS	Derivative of Qs over Viss	F
CSGD	Derivative of Qs over Vidd	F
GCGGS	Derivative with time of Cggs	F/s
GCGGD	Derivative with time of Cggd	F/s
GCDGS	Derivative with time of Cdgs	F/s
GCDGD	Derivative with time of Cdgd	F/s
GCSGS	Derivative with time of Csgs	F/s
GCSGD	Derivative with time of Csgd	F/s
CQG	Current due to gate charge	A
CQD	Current due to drain charge	A
CQS	Current due to source charge	A

Demonstration of the Charge Conserving Feature

A 5-stages ring-oscillator has been simulated with MOS16 model (level 36) with both Shur capacitance and Leroux's charge models. It has been observed that no differences are noticed in the output voltage of the first stage (Figure 2). On the other hand, a evolution of the corresponding gate charge in one among transistors of the first stage can be observed on Figure 3. The gate charge is not conserved with Shur model (CAPMOD=0).

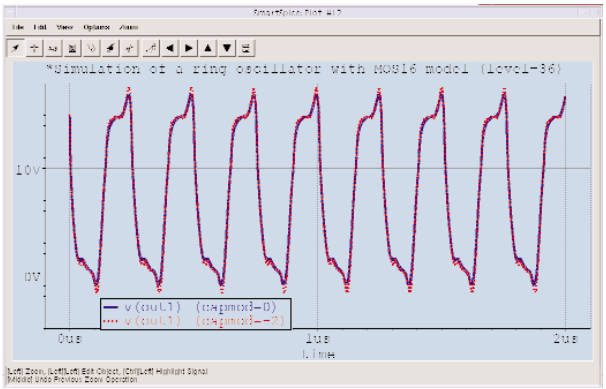

Figure 2. Output of the first stage of a ring oscillator.

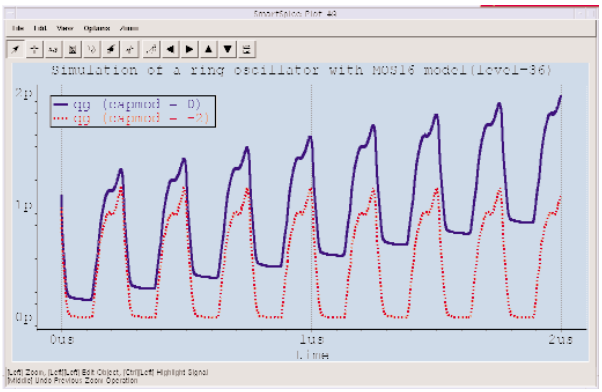

Figure 3. Gate charge evolution of a transistor in a ring oscillator.

New Improvements Selector

Smart selector has been added to select different Silvaco improvements. This selector is compatible with existing RPI flag selector as following:

- if RPI is given, Smart = 0,
- if RPI is not given, Smart is the model parameter SMART (RPI has priority over SMART);
  - if SMART = 0, this is equivalent to RPI given,
  - if SMART = 1, this is the Silvaco implementation of the Shur model with some corrections (equivalent to RPI not given in the previous version of SmartSpice);
  - if SMART = 2, this is equivalent to SMART = 1 with new limitations. The new limitations allows to reduce up to a factor 2 the number of iterations during an OP analysis.

By default, SMART = 2 (the default is the last improvement)

References

[1] M. S. Shur and al., "Modeling and scaling of a-Si:H and Poly-Si Thin Film Transistors", Material Research Society Proceeding, Amorphous and Microcrystalline Silicon Technology, 467, 1997.

[2] G. A. Armstrong and al., "Modeling of Laser-Annealed Polysilicon TFT Characteristics", IEEE Electron Device Letters, vol. 18, No. 7, July 1997.

[3] "New parameters for TFT model: Amorphous (level=35) and Polysilicon (level=36) TFT", Simulation Standard, Volume 10, Number 1, January 1999, pp 9.

BSIM4_U (BSIM4 Universal Routine)

Application

This routine is a multitarget/geometry routine used to extract all kind of characteristics. There is the possibility to trace three different targets. This routine is based on full SMU definition. This definition could be done for 3 different targets grouped together in 4 different setup. It means that 12 different bias conditions can be defined. One device is associated with one setup therefore with one, two or three targets.

This routine has been especially written to measure the gate current for MOS transistors (Figure 1). This routine is available for SOI and MOS technology.

For this both technologies the option macro modeling capability is available. Exchange, rubberband, fit and modeling are not available.

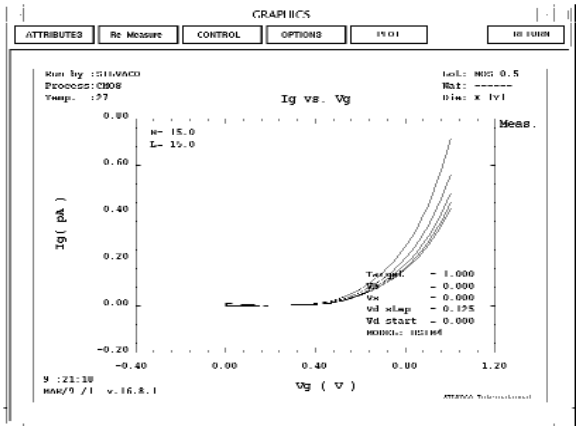

Figure 1. One Target IG vs VG-VD Measurement Data Set.

Data Acquisition

This routine has been written to work especially with HP4155/56 instruments. Each SMU can be fully configured. Each SMU can be either in current or in voltage. The current in each SMU can be limited. The number of section can be different to follow the target. The routine support six SMU maximum.

The Figure 2 shows a characteristics for four devices. This example shows all flexibility allowed by this routine.

Four different setup have been defined, for each setup different targets are measured.

Setup 1 : 3 targets (ID/VD-VG, ID/VG-VB, ID/VG-VD) applied on the device (15u/15u).

Setup 2 : 1 target (ID/VG/VD) applied on device (10u/0.8u).

Setup 3 : 2 targets (ID/VG-VD, IB/VG-VD) applied on device (10u/0.7u).

Setup 4 : 1 target (IS/VD-VG) applied on device (10u/0.65u).

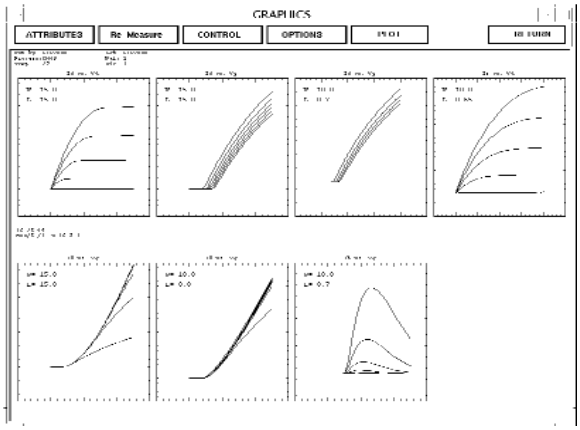

Figure 2. Four devices with different number of targets each.

Measurement Setup

The DC MEASUREMENT SETUP shows two SMU by two SMU. Each SMU can be fully configured. You can measure only one SMU each time.

The parameters will depend on the SMU configuration. If the SMU1 is defined as VAR1 and is connected with the Drain then the parameters displayed will be Vd start, Vd stop, Vd step, Vd points. Whereas if the variable is VAR'1 the parameters displayed will be Vd offset and Vd ratio.

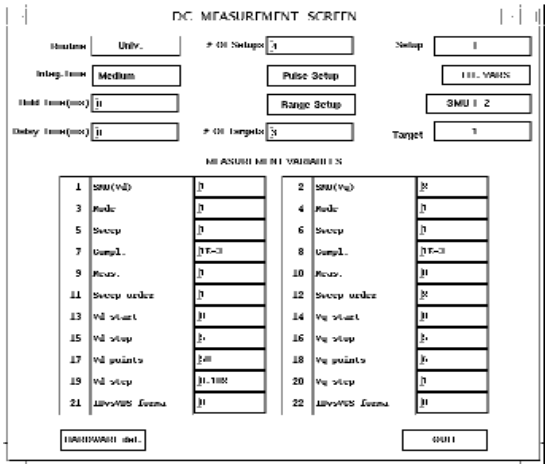

Figure 3. The Universal Measurement Setup Screen for SMU1-2 page.

In this example

Vd is defined as sweep order 1 from 0 to 5 V with a step of 0.102. The sweep is linear and done on voltage source. The current corresponding to Vd is measured, so Id is measured.

Vg is defined as the second sweep from 0 to 5 V with 6 points (therefore 6 sections in the curve).

In the section “Measurement variables” all meaning will be defined.

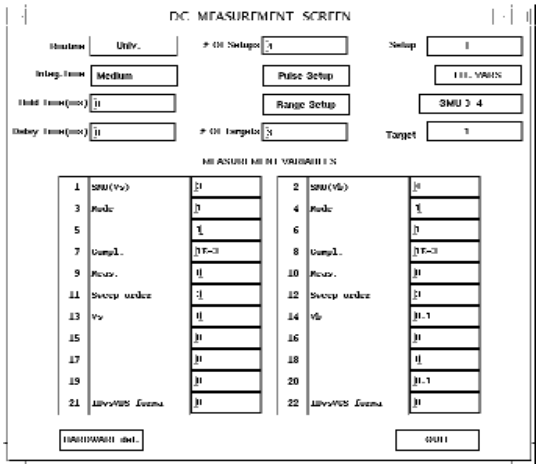

Figure 4. The Universal Measurement Setup Screen for SMU3-4 page.

To complete device polarization, the SMU3 is used as a voltage source with the constant value 0 V , and SMU4 is used as a voltage source with the constant value 0.1 V for the bulk node.

In the case of polarization, the measured current will be ID = f(VDS, VGS) curve.

The following is used for macro modeling or SOI technology when we need more than four SMU.

Measurement Variables

The Table 1 shows the different measurement variables with their possible values. All these variables correspond to one SMU. We call here Y the mode (current of voltage) and x the electrode name (Drain, Gate etc...).

VAR1’ is calculated following the equation: VAR1’ = ratio*VAR1 + offset.

Each SMU can be configured in voltage or current:“Mode”. If you want to sweep in voltage you tape 1 and 2 in current. For the measure it’s the same thing.

The “sweep mode” is used for the main and the second sweep. “Measure” is used to select which SMU you want to use for the measurement.

Number	Name	Description
1/2	SMU_no	SMU number 1 to 6.
3/4	Mode	SMU mode: 1=’V’, 2=’I’, 3=’COM’.
5/6	Sweep	Sweep mode: <2=linear, 3=log10, 4=log25, 5=log50.
7/8	Compl.	Compliance for the SMU.
9/10	Meas.	1=the SMU is measured. 0=the SMU is not measured.
11/12	Sweep order	1=VAR1, 2=VAR2, 3=CONST, 4=VAR1’, 5=Not Used.
13/14	Yx start	Start value of the electrode x sweep range (for VAR1 or VAR2). A constant for CONST. Offset value for VAR1’.
15/16	Yx stop	Stop value of the electrode x sweep range (for VAR1, VAR1’ or VAR2). A constant if “Sweep order=3”.
17/18	Yx points	Number of points for the sweep (for VAR1 or VAR2). Ratio value for VAR1’.
19/20	Yx step	Step value. For VAR1 or VAR2. step = (stop - start) / (points -1).
21/22	IDvsVDS format IDvsVGS format	If “IDvsVDS format” or “IDvsVGS format” is equal to 1 then the current target will be convert to ALL_DC format in the log file.

Table 1. Measurement Variables

The “Sweep order” allows to select between the main sweep (VAR1), the second sweep (VAR2,VAR1’) and a constant. The instrument can accept VAR1, VAR1+VAR2 and VAR1+VAR1’.

IDvsVDS format, IDvsVGS format allows to write the log file in the ALL_DC format. Conversely the routine can read log files in ALL_DC format.

The Table 2 shows an example of measurement variables configuration (Figures 3 and 4) in order to measure an Id/Vd-Vg. In the case where the SMU are configured as following SMU1=Vd, SMU2=Vg, SMU3=Vs , SMU4=Vb , SMU5=V#5,SMU6=V#6.

SMU5 and SMU6 are not used.

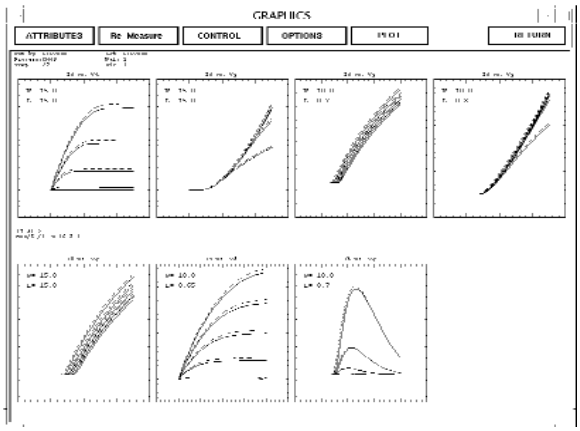

Figure 5. Four devices with different number of target curves Simulated Using Simulated Option.

SMU1-2	SMU1-2	SMU3-4	SMU3-4	SMU5-6	SMU5-6
SMU(Vd) = 1	SMU(Vg) = 2	SMU(Vs) = 3	SMU(Vb) = 4	SMU(V#5) = 5	SMU(V#6) = 6
Mode = 1	Mode = 1	Mode = 1	Mode = 1		
Sweep = 1	Sweep = 1				
Compl. = 1E-3	Compl. = 1E-3	Compl. = 1E-3	Compl. = 1E-3		
Meas. = 1	Meas. = 0	Meas. = 0	Meas. = 0		
Sweep order = 1	Sweep order = 2	Sweep order = 3	Sweep order = 3	Sweep order = 5	Sweep order = 5
Vd start = 0	Vg start = 0	Vs = 0	Vb = 0.1		
Vd stop = 5	Vg stop = 5				
Vd points = 50	Vg points = 6				
Vd step = 0.102	Vg step = 1				
IDvsVDS forma = 0	IDvsVGS forma = 0	IDvsVDS forma = 0	IDvsVGS forma = 0	IDvsVDS forma = 0	IDvsVGS forma = 0

Table 2. ID vs VD-VG measurement variables configuration.

Environment

In the DC MEASUREMENT SCREEN there's a button for the target number selection and for the target selection. For each setup you can select up to 3 targets. The SMU x-y button allows to select SMU page. Each SMU page contain two SMU definitions. The HARDWARE def. button allows to display the HARDWARE CONFIGURATION SCREEN.

In the Setup and Result Screen the attributes button allows to change the Multiroutine Depth. The Multiroutine Depth is the number of target in which you can change the Y scale. The Y scale is changed in the Routine Cntl / Multiple Select.

In the DATA SETUP SCREEN the target number is selected with a button in the right. In the SPAYN DATA SCREEN a button allows to select which target to use for the used point. In the OUTPUT LOG FILE SCREEN the Log X data option named TABLE allows to write in log file uniquely the SMU used and the SMU measured. The TABLE.UNIV option allows to get all currents and voltages during the measurement (SMU 1 to 6).

Local Optimization

The local optimization is available for multi target / geometry capability. The user can select in the TARGET SELECTION SCREEN which target he want to optimize. In the TARGET SELECTION SCREEN for each row a button allows to select which target to optimize. This selection will be available for all devices chosen in the geometry button. So if you want to optimize target 1 of device 1 and target 2 of device 1 you must use two rows in the TARGET SELECTION SCREEN. Also, be careful if you select two devices with a different target number.

Global Optimization

The global optimization is available for multitarget / geometry capability. The user create a box on the target he wants to optimize. Example Figure 6 only two target is optimized. If there's no box nothing will be optimize. To optimize an entire target you must create a box including all curves.

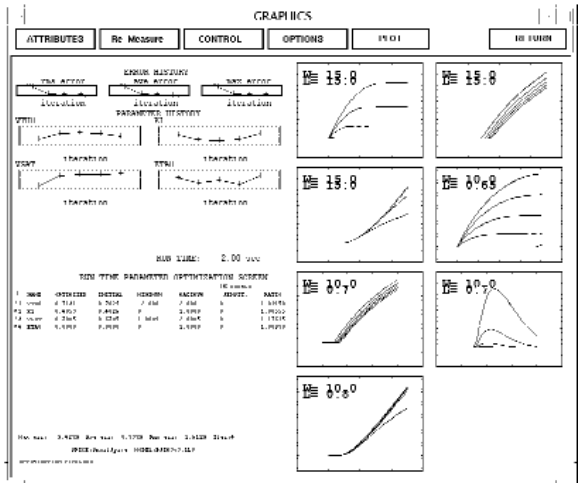

Figure 6. Four devices with different number of targets. Curves, Simulated Using the Simulate Option.

Macro Modeling

Macro modeling is available for both SOI and MOS technologies.

Parameter Labels (constant or equation)

Parameter Labels are defined with the Parameter Definition statement .PARAM in the .net file. Parameter Labels can be defined as constant numerical values or as an equations defined with constant numerical and / or previously specified Parameter Labels.

Equations must be enclosed by single quotes (‘) or normalized delimit character (External SPICE dependent). Once defined, a Parameter Labels can be used in the netlist or model card when a constant numerical value is expected.

For the MOS technology the following parameters are indispensable to define all electrodes. In the case where the macro model is defined with six pads.

Example

```
.PARAM Vd_VAL    = 0.000000e+00
.PARAM Vg_VAL    = 1.100000e-01
.PARAM Vs_VAL    = 1.000000e+00
.PARAM Vb_VAL    = 0.00000e+00
.PARAM V#5_VAL   = 0.000000e+00
.PARAM V#6_VAL   = 0.000000e+00
```

For the SOI technology

Example

```
.PARAM Vd_VAL    = 0.0000000e+00
.PARAM Vg_VAL    = 0.0000000e+00
.PARAM Vs_VAL    = 0.0000000e+00
.PARAM Vbg_VAL   = 0.0000000e+0
.PARAM Vbd_VAL   = 0.0000000e+00
.PARAM V#6_VAL   = 0.0000000e+00
```

Power Sources

Power Sources are available to drive the macro-device.

G Voltage Controlled Current Source

H Current Controlled Voltage Source

I Constant Current Source

V Constant Voltage Source

For the MOS technology the power sources are defined as following.

```
Vd 1 0 ’Vd_VAL’
Vg 2 0 ’Vg_VAL’
Vs 3 0 ’Vs_VAL’
Vb 4 0 ’Vb_VAL’
V#5 4 0 ’V#5_VAL’
V#6 5 0 ’V#6_VAL’
```

For the SOI technology.

```
Vd   1  0 ’Vd_VAL’
Vg   2  0 ’Vg_VAL’
Vs    3  0 ’Vs_VAL’
Vbg 4  0 ’Vbg_VAL’
Vbd 5  0 ’Vbd_VAL’
V#6 5 0 ’V#6_VAL’
```

Control Statements File

The format of the Control Statements File for the macro-model must match the routine used to measure the macro-device. The power source names used in the circuit must match the power sources name in the Control Statement File. The values of the power source sweep and step parameters are not important since UTMOST will substitute them with the values stored in the Measurement Screen relative to the routine used. It is essential that the measurement and simulation bias conditions be identical.

Following power sources defined previously the control statement for MOS can be:

Example

```
*UTMOST INTERFACE
.DC Vd 0 5.000 0.100 Vg 1.0 5.0 1.0
.PRINT DC I(Vd)
```

For SOI technology:

Example

```
*UTMOST INTERFACE
.DC Vd 0 5.000 0.100 Vg 1.0 5.0 1.0
.PRINT DC I(Vbd)
```

Conclusion

The new BSIM_U routine permits all the measurements for device characteristic measurement. This routine allows the parameter optimization corresponding to the gate current using Global and Local optimization. Based on full SMU definition, this routine is able to combine different kind of characteristics together, for characterization and parameter optimization.

Calendar of Events

October

1
2 ISCS-Monterey, CA
2000 SOI-Wakefield, MA
3 ISCS-Monterey, CA
2000 SOI-Wakefield, MA
EDA & Test Expo 2000-
Hisinchu,Taiwan
4 ISCS-Monterey, CA
2000 SOI-Wakefield, MA
EDA & Test Expo 2000-
Hisinchu,Taiwan
5 ISCS-Monterey, CA
2000 SOI-Wakefield, MA
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25 LCD/PDP Int'l 2000,
Pacifico, Yokohama
26 LCD/PDP Int'l 2000,
Pacifico, Yokohama
27 LCD/PDP Int'l 2000,
Pacifico, Yokohama
28
29
30
31

November

1
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4
5 2000 GaAs IC Tech - Seattle WA
6 2000 GaAs IC Tech - Seattle WA
ICCAD 2000 - San Jose, CA
7 2000 GaAs IC Tech - Seattle WA
ICCAD 2000 - San Jose, CA
8 ICCAD 2000 - San Jose, CA
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Bulletin Board

*Silvaco becomes e*ECAD Vendor Partner*

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Silvaco now commits to including Linux as a platform for most of its products. Linux is rapidly gaining general acceptance as an operating system. Contact your local representative for information on the latest tools to be included in the Linux line-up.

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For more information on any of our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

Mustafa Taner, Applications and Support Engineer

Q. How can I measure CJSWG (CJGATE) Capacitance using *UTMOST III*?

A. For the ***UTMOST III*** versions greater than 17.2.0.R, the ***UTMOST*** users can measure the CJSWG (CJGATE) capacitance using the "CJ/CJSW" routine.

The CJ/CJSW routine in MOS technology has been modified to measure the CJSWG (Peripheral portion of the junction capacitance under the gate) capacitance.

In order to extract the additional CJSWG capacitance there should be three structures available in the test die:

1) The Area structure (typically a large diode). Used to extract CJ
2) The Periphery structure (finger structure, periphery maximized). Used to extract CJSW
3) The Gated diode structure. This structure could be a MOS transistor with very large width. Used to extract CJSWG.

The area and periphery values of each diode should be entered into ***UTMOST***'s "Device Pads Screen". In order to open the "Device Pads" screen press the "Hardware" button from the main ***UTMOST*** screen and select the "Probing"menu option. Then press the "Devices" button. (Figure 1).

In addition to the Area and Periphery values, the width of the region which remains under the gate should be entered for the CJSWG structure. The gate width value of the CJSWG structure can be entered under the "Width" column of the "strategy" screen. The CJ and CJSW structures do not require any "width" or "length" value entered in the strategy screen. They can be left blank as long as their total area and periphery values are given in the "Device Pads Screen". The Periphery of

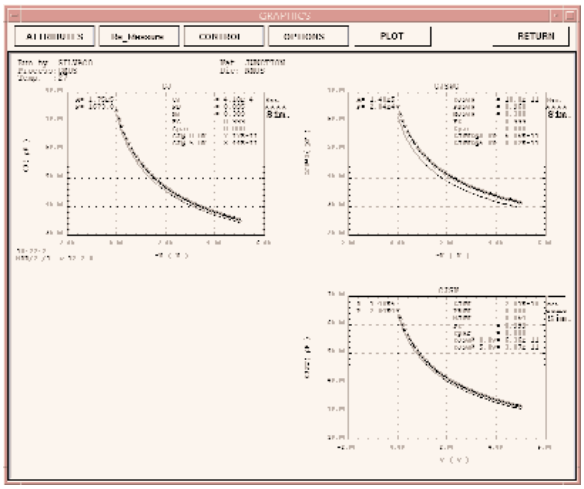

Figure 2. CJ/CJSW routine measured and simulated curves including the CJSWG data.

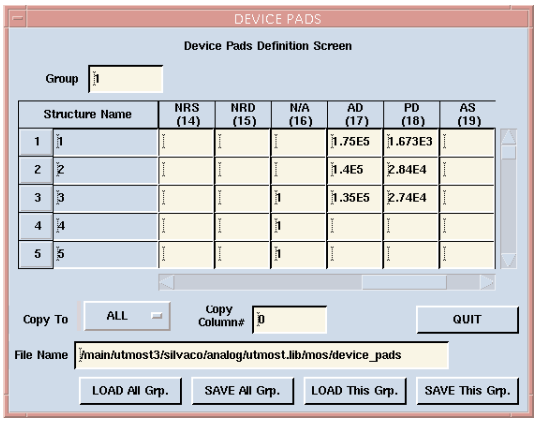

Figure 1. Device Pads screen with three structures' Area and Periphery values entered.

the CJSWG structure should not include the under the gate side of the diode. It should only include the sides which are not under the gate.

To measure the third structure (CJSWG) the "CJSWG_measure" flag in the Set Measurement screen of the CJ/CJSW routine should be set to "1". After the flag is set to "1" the user can proceed with measurement and parameter extraction. The system will prompt the user with messages to connect the proper structures before each measurement. After the data collection the standard ***UTMOST III*** "Fitting" and "Optimization" procedures can be applied. (Figure 2.)

If there is no CJSWG structure available and only CJ and CJSW values need to be extracted, then the "CJSWG_measure" flag should be set to "0".

The total capacitance of the CJSWG structure will be calculated as :

```
CJtotal = CJ x Area3 + CJSW x Periphery3
+ CJSWG x Width
```

Area3: Total area of the CJSWG diode.

Periphery3: The Periphery of the CJSWG diode excluding the "under the gate" portion.

Width: The width of the region which remains under the gate.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

Phone: (408) 567-1000 Fax: (408) 496-6080

e-mail: *support@silvaco.com*

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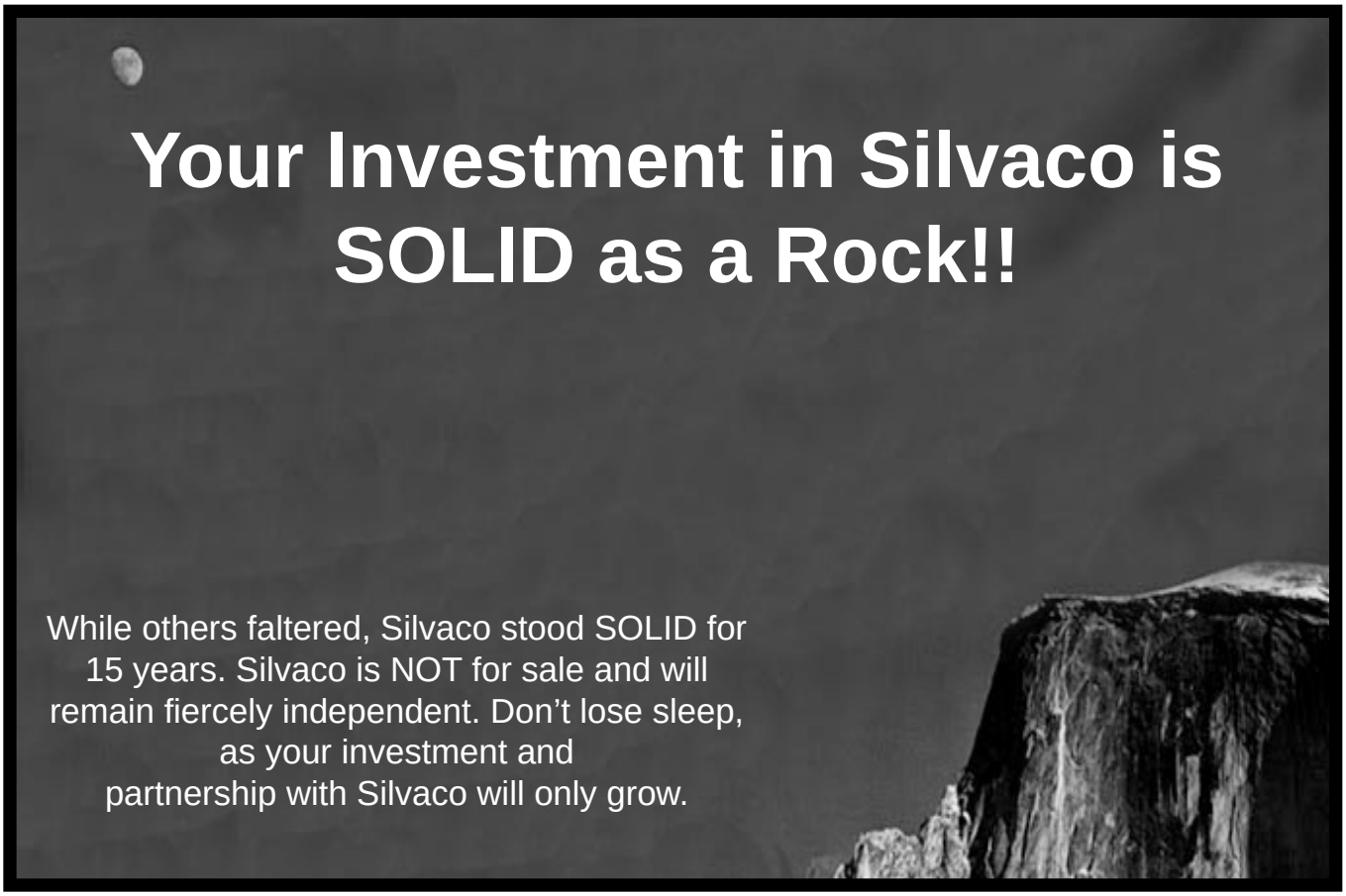

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