Simulation Standard

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Simulating Impurity Freeze-Out During Low Temperature Operation

Introduction

The low temperature operation of many device structures has been shown as an effective method for improving device performance without reducing device size. Performance improvements for MOS-based technologies include increased operating speed, enhanced latch-up immunity, and better subthreshold characteristics [1]. By modeling low temperature phenomena, numerical simulation of device operation at low temperatures provides an effective means for analyzing such performance improvements before investing manufacturing time or money. It is the purpose of this paper to discuss the modeling of the dopant freeze-out phenomenon in ***ATLAS*** and provide an application example of its use.

At low temperatures, the thermal energy within a semiconductor is not high enough to fully activate all of the donor and acceptor impurity atoms. As a result, the carrier concentrations will not equal the concentration of dopant atoms. Figure 1 shows simulated data of the equilibrium electron concentration as a function of temperature for n-type silicon doped at 10^{16} cm^{-3}. Below 100 K there is not enough thermal energy within the silicon to fully ionize the impurity atoms. This region of operation is known as the freeze-out regime. At temperatures between 100 K and 550 K, sufficient thermal energy resides within the silicon to fully ionize the impurity atoms. This region of operation is known as the extrinsic regime. As the temperature increases beyond 550 K, the intrinsic carrier concentration approaches and then exceeds the impurity concentration and the silicon returns to intrinsic-type behavior [2].

Device Model

Within ***ATLAS***, Poisson's Equation is used to relate the electrostatic potential to the space charge density in a semiconductor device. The local space charge density is the sum of all positive and negative charges including all mobile and fixed charges, electrons, holes, and ionized impurities. Poisson's equation including the carrier

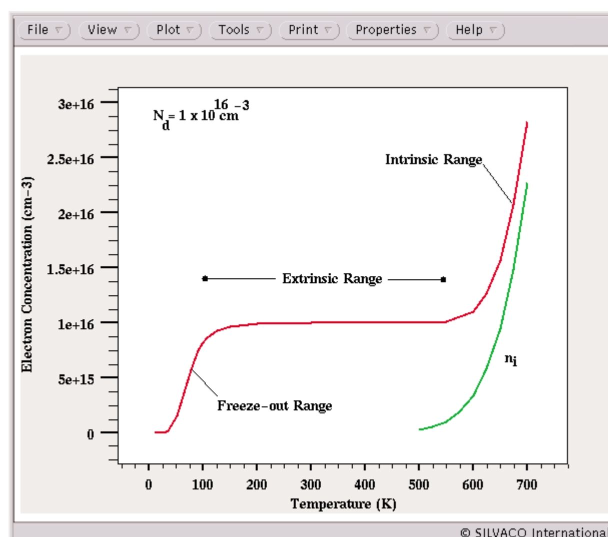

Figure 1: Electron concentration as a function of temperature in n-type silicon.

concentrations, ionized donor and acceptor impurity concentrations, and charge due to the presence of traps and defects has the form [3]:

$$div(\varepsilon \nabla \Psi) = q(n - p - N_D^+ + N_A^-) + Q_T \quad (1)$$

where ε is the dielectric constant, Ψ is the electrostatic potential, q is electronic charge, n and p are the electron and hole concentrations per unit volume, respectively, and N_D^+ and N_A^- are the ionized impurity concentrations.

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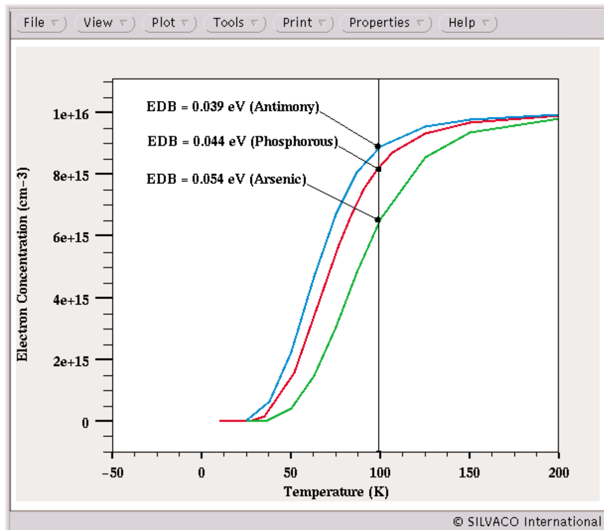


Figure 2: Electron concentration as a function of temperature for n-type silicon with varying values of ionization energy.

By default, ***ATLAS*** assumes complete ionization of all dopant impurities and that no traps or defects exist within the device (i.e. $N_D^+ = N_{D,Total}$, $N_A^- = N_{A,Total}$, and $Q_T = 0$). To account for the loss of space charge due to the incomplete ionization of dopant atoms, the incomplete ionization model available in ***ATLAS*** must be explicitly invoked using the MODELS statement.

Impurity freeze-out is modeled in ***ATLAS*** using Fermi-Dirac statistics and degeneracy factors associated with the conduction and valence energy bands. The ionized donor and acceptor concentrations are calculated as [3]:

$$N_D^+ = \frac{N_D}{1 + GCB \exp\left(\frac{\varepsilon_{Fn} - EDB}{kT_L}\right)} \quad (2)$$

$$N_A^- = \frac{N_A}{1 + GVB \exp\left(\frac{\varepsilon_{Fp} - EAB}{kT_L}\right)} \quad (3)$$

where EDB and EAB are the respective donor and acceptor ionization energies and GCB and GVB are the respective degeneracy factors. N_D^+ and NA are the net compensated n-type and p-type doping concentrations, respectively. Where net compensated doping is defined as [3]:

If $N_{total} \equiv (N_{D,total} - N_{A,total}) > 0$

Then $N_D = |N_{total}|$ and $N_A = 0$

Otherwise $N_A = |N_{total}|$ and $N_D = 0$

The incomplete ionization model may be explicitly set by including the INCOMPLETE parameter on the MODELS statement. Table 1 lists the default parameter values for EDB, EAB, GCB, and GVB in ***ATLAS***. Figure 2 shows simulated data obtained for electron concentration as a function of temperature for three different ionization energies. As can be seen, even at 100 K the ionization

	EDB	EAB	GCB	GVB
Default	0.044eV	0.045eV	2	4

Table 1. Default model parameters for incomplete ionization.

energy can have a substantial effect on carrier concentration therefore it is highly recommended that accurate ionization energies are determined for low temperature simulation. A more complete list of ionization energies is available in [4].

For heavily doped structures, the assumption of a localized ionization energy does not hold up. Simply modeling the temperature dependence of the ionization energy will not adequately account for the underlying physics. It is generally accepted to assume total ionization for doping concentrations above some threshold (3×10^{18} cm^{-3} in ***ATLAS***) and to use some transitional function to determine the partial ionization between complete ionization and that predicted by Equations 2 and 3 [5]. When simulating devices doped beyond

$$EDB = 44.0 - 3.6\times10^{-8} \cdot \sqrt[3]{N_D} \quad (4)$$

$$EAB = 43.8 - 3.037\times10^{-5} \cdot \sqrt[3]{N_A} \quad (5)$$

threshold, the ionization energies used in Equations 2 and 3 may be modified to obtain more accurate results as follows [3]:

Complete ionization is assumed for structures doped higher than 3×10^{18} cm^{-3}. For structures with doping levels between 10^{18} cm^{-3} and 3×10^{18} cm^{-3}, linear interpolation is used to fit the ionization energies. The modified ionization model may be selected using the IONIZ parameter on the MODELS statement.

Application

The importance of modeling incomplete ionization in the freeze-out regime will be illustrated by examining the saturation behavior of a DMOS device. Figure 3 presents the base DMOS device structure used for this

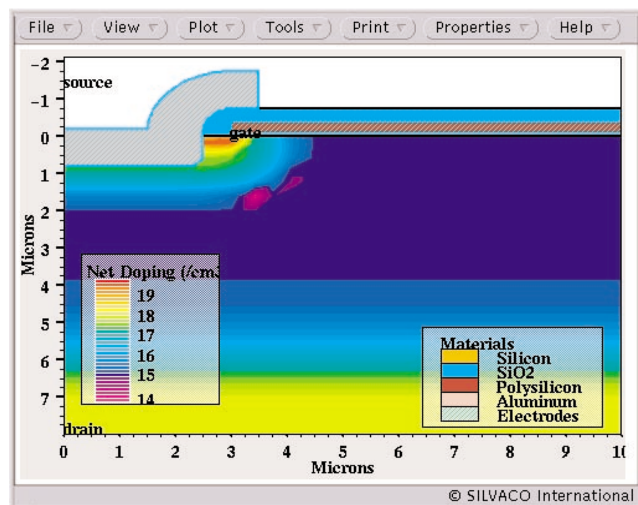


Figure 3: Simulated cross section of the DMOS device.

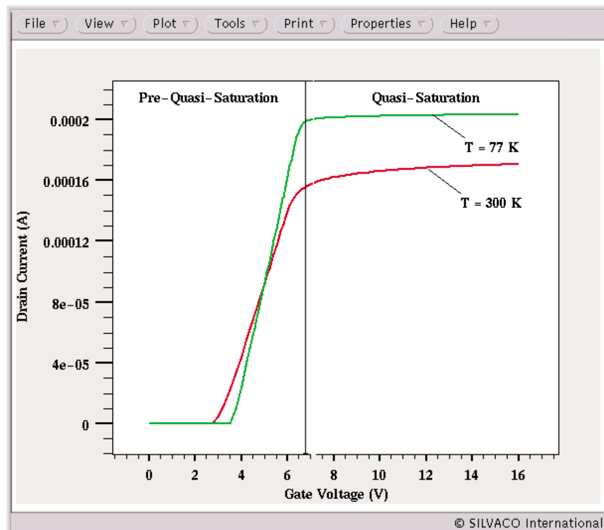


Figure 4: Saturation characteristics for DMOS device at 77 K and 300 K.

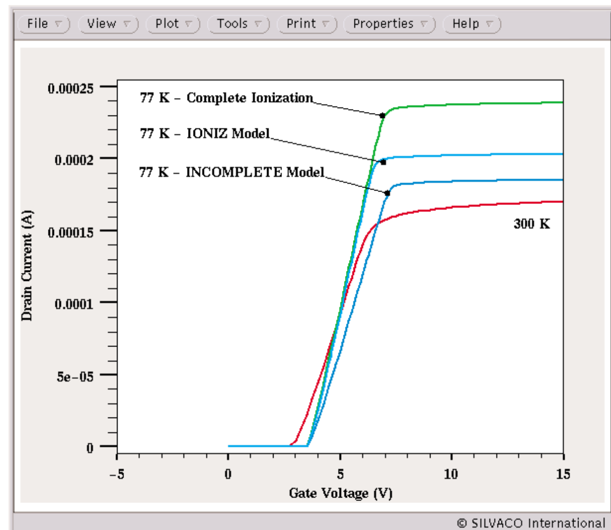


Figure 5: Saturation characteristics for DMOS device at 77 K and 300 K (alternate model sets).

analysis. The device has a lateral channel extending 1.8 µm beneath the gate oxide with a peak doping density of $5\times10^{15}cm^{-3}$. Below the lateral channel, an n-type epilayer of 6 µm doped at 10^{15} cm^{-3} is used to sustain high voltage. The gate is n^+ polysilicon doped at 10^{16} cm^{-3}. The gate oxide is 60 nm thick. For this work, only half of the device structure was simulated as it was adequate for examining the influence of dopant freeze-out.

In the on-state, a DMOS device conducts current from the source through the lateral channel beneath the gate oxide and finally to the drain via the substrate epilayer. Figure 4 presents the simulated subthreshold characteristics for the DMOS device described above at both 77 K and 300 K. As the device turns on, the drain current increases with gate voltage over an isolated voltage range. This region of operation is referred to as the pre-quasi-saturation region. Beyond the pre-quasi-saturation region, the drain current saturates becoming independent of the gate bias. This region of operation is referred to as the quasi-saturation region and it represents an important aspect of DMOS behavior [1].

In the pre-quasi-saturation region, electrons are exposed to a large electric field and traverse the lateral channel at their saturation velocity. As a consequence, the drain current is the product of the electron concentration and the saturation velocity. Electron concentration therefore is a primary factor in determining the resulting drain current and accounting for incomplete ionization at low temperatures is essential [1]. Also note in Figure 4 the higher transconductance seen for the 77 K device in the pre-quasi-saturation region.

For the DMOS device biased to quasi-saturation, the situation is different. The large electric field experienced during pre-saturation is no longer present and the charge carriers no longer travel at their saturated velocity. Variations in device performance in this region between the 77 K and 300 K device are primarily related to the temperature dependence of the carrier mobilities [1]. Figure 5 compares the predicted saturation behavior for the DMOS device using three different model sets, one disregarding incomplete ionization, another incorporating only the local space charge model, and the final set accounting for dopant concentrations above threshold. As can be seen, the simulation results obtained without an incomplete ionization model predict a much high saturation current due to increased carrier mobility and no loss of carrier concentration. The other two simulations predict saturation currents above that of the 300 K device, but their saturation currents have been reduced due to incomplete ionization.

Summary

A brief review of the incomplete ionization model available within ***ATLAS*** has been presented. The importance of modeling incomplete ionization during low temperature simulations was shown through the analysis of the subthreshold behavior of a DMOS device. It was shown that for device simulations below 100 K accurate modeling of incomplete ionization is necessary to maintain accuracy.

References

[1] C. Liu, K. Lou, and J. Kuo, "77 K Versus 300 K Operation: The Quasi-Saturation Behavior of a DMOS Device and its Fully Analytical Model," IEEE Transactions on Electron Devices, vol. 40, pp. 1636-1644, September 1993.

[2] E. Yang, Microelectronic Devices, New York, McGraw-Hill, 1988.

[3] *ATLAS User's Manual*, Silvaco International, November 1998.

[4] S.M. Sze, Physics of Semiconductor Devices, New York, John Wiley & Sons, 1981.

[5] S. Selberherr, "MOS Device Modeling at 77 K," IEEE Transactions on Electron Devices, vol. 36, pp. 1464-1474, August 1989.

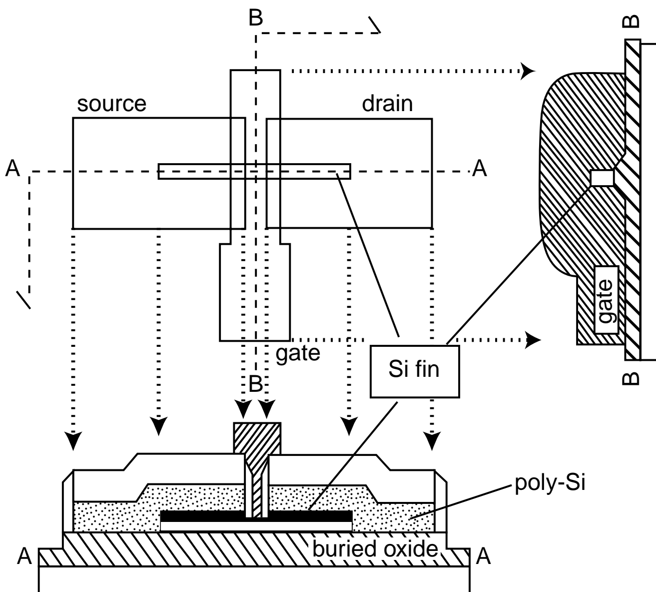
Simulation of Vertical Double-Gate SOI MOSFETs Using *Device3D*

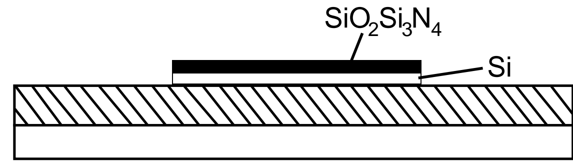
I. Introduction

This article will present the simulation methodology of a self-aligned double-gate MOSFET structure (FinFET) using SILVACO 3-D simulation suite. The double-gate MOSFET is one of the most attractive alternative to classical MOSFET structure for gate length down to 20nm. The main advantage of the FinFET is the ability to drastically reduce the short channel effect. In spite of his double-gate structure, the FinFET is closed to its root, the conventional MOSFET in layout and fabrication. 3-D numerical simulations of the FinFET are performed in this article, in order to validate the basic principles and to uncover several important aspects: evaluation of the length , width and quantum effects.

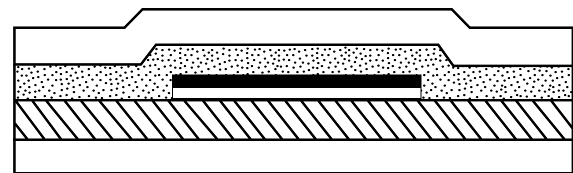
II. Device Features

The features of the structure are shown in Figure 1 are: (1) a transistor is formed in a vertical ultra –thin Si fin and is controlled by a double-gate, which considerably reduced short channel effects; (2) the two gates are self aligned and are aligned to S/D; (3) S/D is raised to reduce the access resistance; (4) Up to date gate process: low temperature, high –k dielectrics can be used and (5) the structure is quasi-planar because Si Fin is relatively short [1,2].

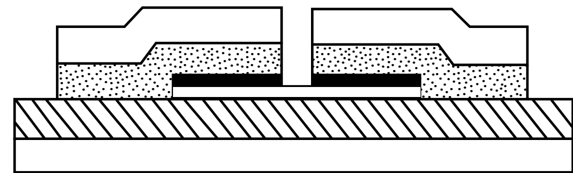




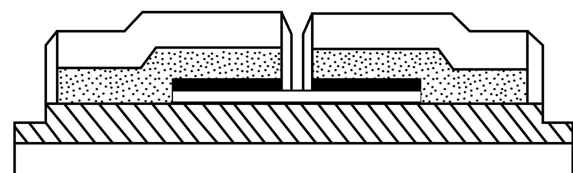
(1) After depositing Si_3N_4 and SiO_2 stacked layer, Si fin was formed.



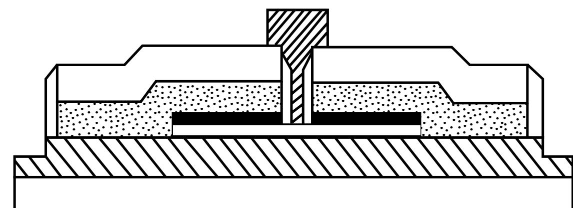
(2) Phosphorus-doped-poly Si and SiO_2 stacked layer deposited.



(3) Source and drain were etched while Si fin was covered by the mask layer.



(4) Spacer SiO_2 layer was etched down into buried oxide layer.



(5) After depositing B-doped SiGe, gate pattern was delineated.

Figure 1. FinFET layout design and device structure. The bottom is A-A cross section and the right is B-B cross section.

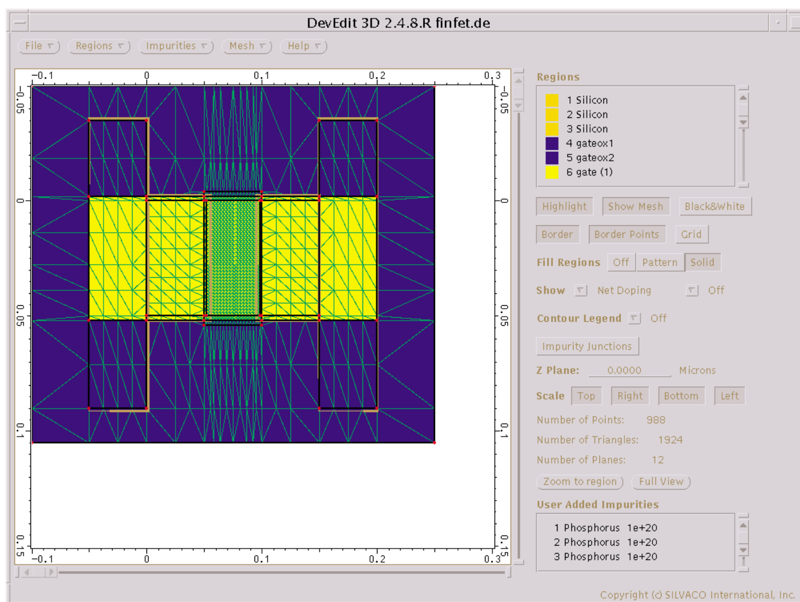


Figure 2. Illustration of DEVEDIT3D used to build the FinFET structure

by drawing first the FinFET, from the bottom view (Figure 2),in a (x,y) plane before extending it in the z-direction.

The z-direction in this case corresponds to the vertical to the substrate. The final 3-D structure is shown in ***TonyPlot3D*** (Figure 3).

The basic characteristics of this Finfet was Tox=2nm length=50nm width=50nm and Fin height=50nm. Note that we have defined a parametrized structure for subsequent use in our automation tool which make much more easier any kind of variation (length, width ..) to perform large scale simulation.

The main physical effects (mobility, carrier statistics, recombination) were expressed by a set of models universally used for simulating the MOS technology: mobility dependence of the electric field and doping level, Boltzmann statistics and Schokley-Read-Hall generation recombination mechanisms[3].

III. Device Simulation

The 3-D SILVACO simulation suite including ***Device3D***, ***DevEdit3D*** and ***TonyPlot3D***, allows device engineers to study deep sub-micron devices which are 3-D by nature like the FinFET presented above. Furthermore, 3-D simulations give access to data impossible to measure like charge distribution, potential, electric field and current lines.

A 3-D FinFET structure was designed by using ***DevEdit3D***. This is an advanced tool for structure editing and mesh generation. The device structure was realized

IV. Simulation Results

Typical I-V characteristics of a 50-nm gate length are shown in Figure 4. The leakage current caused by DIBL was well suppressed.

The rool-off of a FinFET with a width of 50nm is well controlled as can be seen in Figure 5. This result can be correlated to the good control of the channel potential due to the double gate.

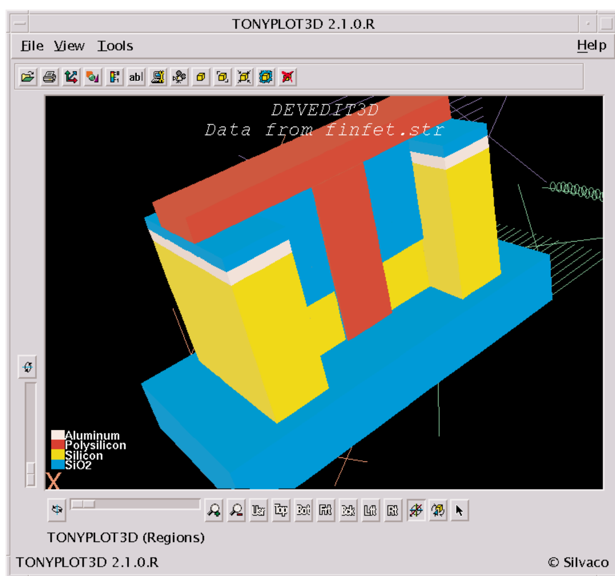


Figure 3. Plot of a 50-nm FinFET 3-D structure for a width of 50nm

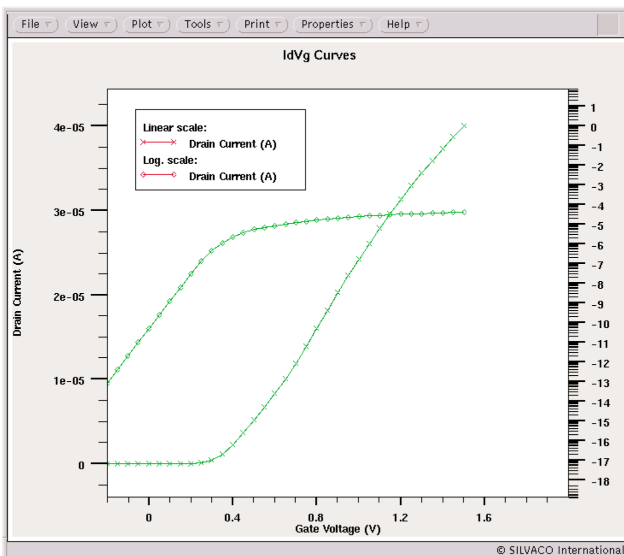


Figure 4. 50-nm FinFET IdVg curves for a width of 50nm.

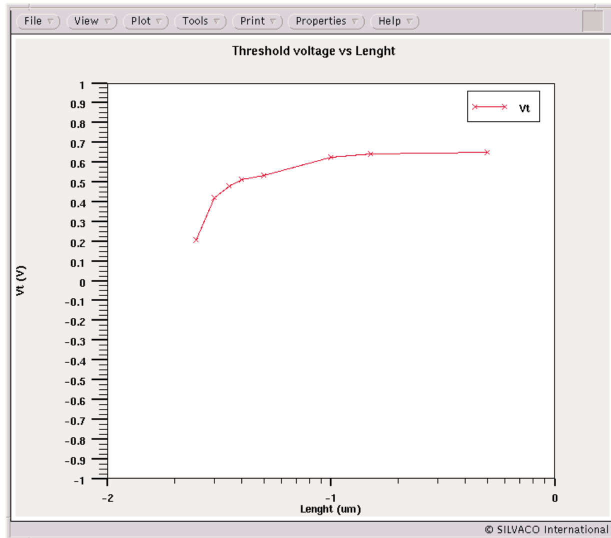


Figure 5. Threshold voltage as a function of gate length for a width of 50-nm.

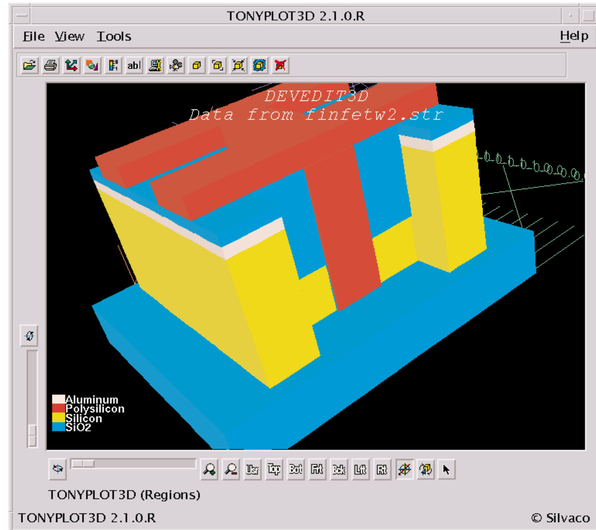


Figure 6. Structure of a 2-parallel channel device. Gate length 50-nm.

The width of this FinFET is adjusted by the number of Si fins. Let say you want to double the width of your device then you have to put 2 Fins between source and drain (Figure 6).

Note that this can be achieved very simply using the "mirror" feature in ***DevEdit3D***. The resulting I-V curve can be seen in Figure 7: drain current is doubled.

Finally we have made simulations using our quantum module named ***Quantum3D***. The result is plotted in Figure 8. One can see a shift in the threshold voltage indicating some quantum effect. This correction is quite small as indicated in [2].

VI. CONCLUSION

Sub 50-nm FinFETs were successfully simulated using 3-D SILVACO simulation tools. It is very easy to study the impact of the geometry and doping of this 3-D device using ***Device3D***. Indeed more and more people take a look at this novel structure since it is an attractive successor to the single-gate MOSFET

References

[1] D.Hisamato et al. - IEDM'98

[2] X.Huang et al. - IEDM'99

[3] SILVACO International - *ATLAS User's Guide.*

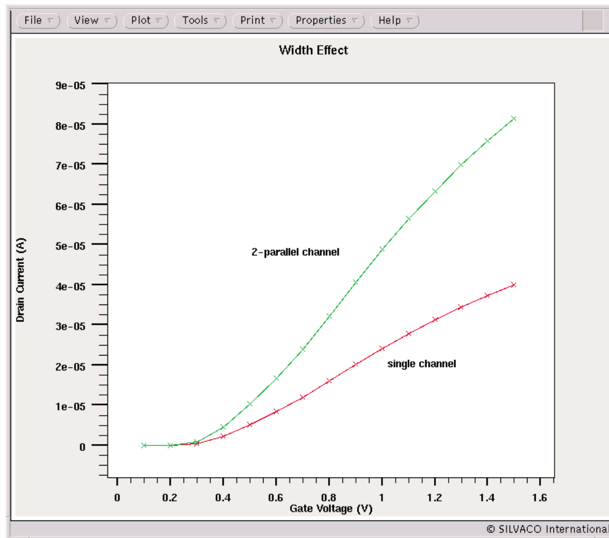


Figure 7. Drain current comparison between single and 2-parallel channel device. Gate length 50-nm.

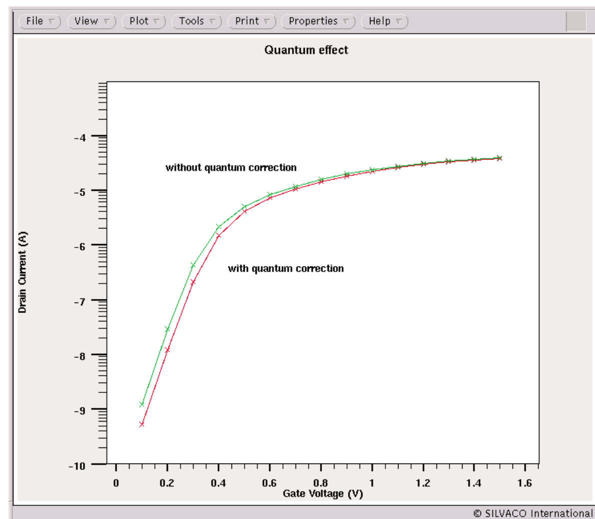


Figure 8. Quantum effect in a 50-nm with a width of 50nm.

Non-Stationary Transport Effects: Impact on Performances of Realistic 50nm MOSFET Technology

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Abstract

We analyze quantitatively the real impact of technology on the needed level for carrier transport modeling. The results, based on theoretical analyzes, are applied to existing devices. This work shows which recipes must be used to evaluate the performances of advanced device architectures (down to 50nm gate length). An original point of this work is the investigation of technology influence (channel doping and LDD doping) on injection velocity at source side and on drain current. The results open the perspective of specific engineering of access regions in order to take full advantage of non-stationary effects on the drain current.

1. Introduction

For MOSFETs with gate length ranging around and below 0.1µm, it is now well established that the Drift-Diffusion (DD) model fails to predict velocity overshoot and carrier diffusion due to electronic temperature gradients. Moreover, this model neglects the dependence of hot-carrier effects on carrier energy, giving unphysical results for issues related to impact ionization and reliability. Hence, advanced models become mandatory for accurate simulation of nowadays devices, even if the question of the needed accuracy of modeling level for practical applications still remains. Solutions like Monte-Carlo (MC) simulation are very accurate [1], but CPU-consuming, therefore difficult to be applied for technology optimization. For this reason we preferred to use an advanced energy transport model available in commercial tools [2], which combines the advantages of satisfactory accuracy and fast calculations.

After a short description of the simulated devices, we calibrate the transport model on MC data. Then we analyze how non-stationary effects impact the device behavior and the dependence of this impact on main technological parameters.

2. Simulated Devices

Many previous works are performed on simplified devices (constant channel doping, no LDD, no pockets). Since doping profiles strongly influence the spatial variations of electric field, realistic devices are needed for accurate conclusions on non-stationary effects. Consequently we have decided to use devices obtained by simulating the technological process of our 50nm technology [3]. Devices are designed with LDD extensions and pockets, and the oxide thickness is 2.3nm. It was demonstrated that DIBL is a major concern for an accurate analysis of velocity overshoot [4], consequently we optimized the shorter device (L_g=50nm) to have an I_{off} lower than 0.1nA/µm. Longer devices have the same structure, which ensures low DIBL.

3. Calibration of Energy Balance Model

The simulations were performed with Drift-Diffusion (DD) and a modified Energy Balance (EB) models of Atlas (Silvaco). The main parameters (mobility, carrier statistics, recombination) are expressed by the same models in EB and DD, with the difference that in EB they are no longer electric field dependent, but carrier energy dependent [2]. Compared to DD, EB considers two additional equations: the conservation of the carrier energy and the energy flux. A critical parameter in EB model is the energy relaxation time, τ_{rel}, which governs the magnitude of the non-stationary effects. Figure 1 shows that τ_{rel} has a strong impact on terminal currents. The variation of I_{Dsat} (drain current at V_G=V_D=1.5V) versus τ_{rel} is linear for trel between 0.05ps and 0.5ps, and becomes saturated outside this range (inset in Figure 1).

When τ_{rel} decreases, carrier energy reaches equilibrium with electric field faster, which implies less non-stationary effects. Moreover, for τ_{rel}l<0.01ps the DD regime is attained and the EB current is limited to the value

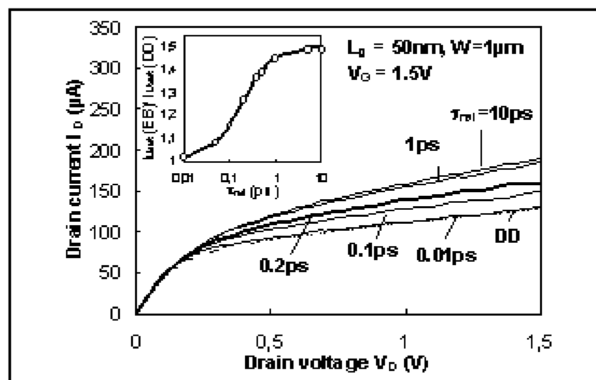

Figure 1. Influence of energy relaxation time, τ_{rel}, on $I_D(V_D)$ curves (inset: variation of ratio $I_{Dsat}(EB)/I_{Dsat}(DD)$ with τ_{rel}).

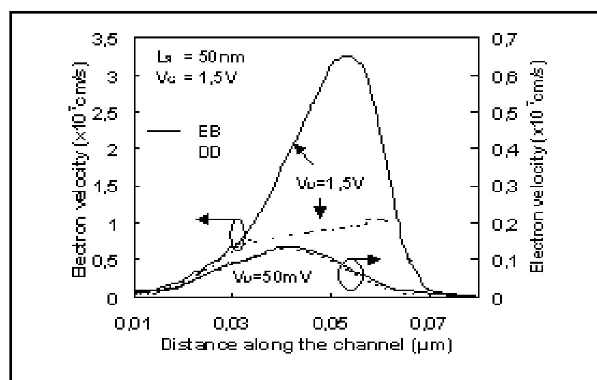

Figure 2. Profiles of velocity at 10Å channel depth obtained by EB and DD at low and high drain voltage.

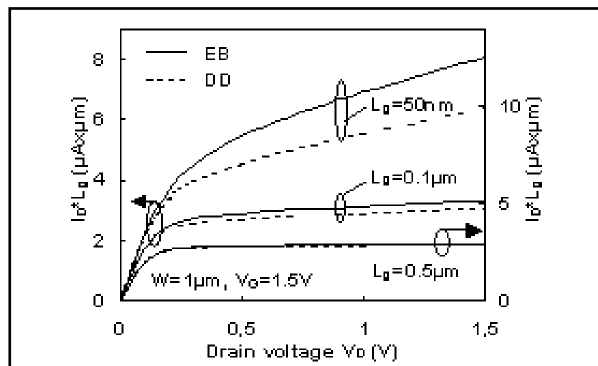

Figure 3. I_D*L_g (V_D) characteristics simulated with EB and DD for different channel lengths.

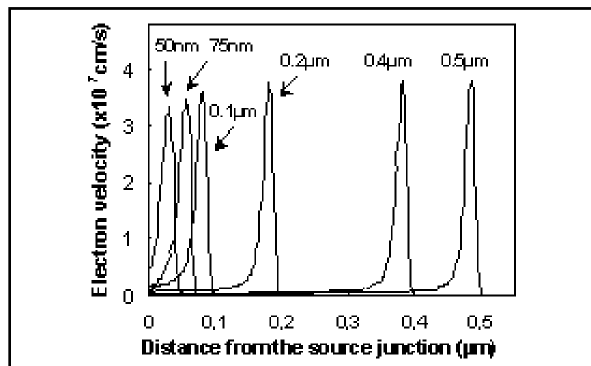

Figure 4. Profiles of velocity in the channel at 10Å depth for various L_g (V_G=V_D=1.5V).

predicted by DD model. Since very controversial values of τ_{rel} (from 0.1 to 1ps) are given in the literature, we calibrated our simulator on MC data, the best match between EB and MC results being obtained for τ_{rel} = 0.2ps.

Impact ionization is modeled by the Selberherr [2] model in both DD and EB. In EB the effective field depends on the carrier energy, through an energy relaxation length related to τ_{rel} [2].

4. Simulation Results

4.1. Velocity Overshoot

The first effect of non-stationary transport in very short channels is the velocity overshoot, which impacts directly the drain current. The electric field-dependence in DD model does not allow to simulate the velocity overshoot phenomenon. This explains the difference between the drain current obtained by EB and DD: (a) at high V_D the EB drain current is significantly higher, because in DD model the velocity is limited to the saturation value (about 10^7 cm/s, Figure 2), leading to under-estimated drain current; (b) at low VD however, the velocity profiles in the channel are almost the same for both models (figure 2), even in very short channels, which implies the same drain current level.

It is worth noting that the difference between currents predicted by EB and DD depends strongly on the channel length, channel doping and LDD region doping. We discuss in the following the impact of each parameter.

Channel length. When the channel length increases, the difference between DD and EB decreases as shown in Figure 3, and becomes negligible for L_g>0.25µm. I_{Dsat}(EB)/I_{Dsat}(DD) ratio is about 1.3 for L_g=50nm and 1.02 for L_g=0.25µm. The practical consequence of this analysis is that we can evidence an inferior limit of the channel length for using the classical DD model. In our case this limit is about 0.25µm, therefore for shorter gate lengths the use of advanced models is necessary for obtaining accurate simulation results. We mention that this limit can also slightly vary as a function of gate-channel and source/drain-channel architecture.

Figure 4 presents the variation of the EB electron velocity along the channel for different L_g. An interesting result is that the velocity overshoot at the drain side increases slowly with L_g, while the opposite behavior was expected. The explanation is that carriers are strongly accelerated in short channels, but they cannot reach the maximum velocity, as they are rapidly collected in the drain. When L_g increases the maximum velocity increases and becomes saturated for L_g=0.2µm. However, this phenomenon is not reflected in the drain current because near the drain the increase of the velocity with L_g is accompanied by a strong decrease of the carrier concentration.

Moreover, it has been shown that the current enhancement is due to the increase in the velocity at the source side, where the carrier concentration is gate

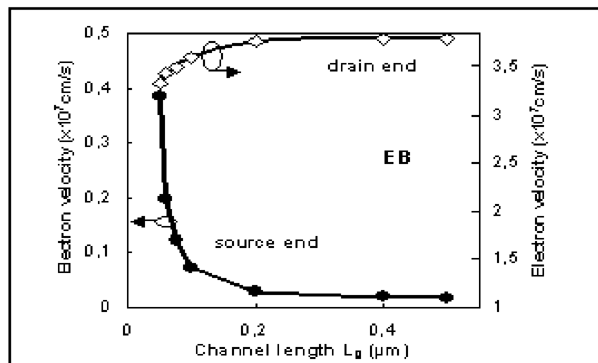

Figure 5. Drain and source–end velocity obtained by EB model as a function of the channel length (V_D=V_G=1.5V).

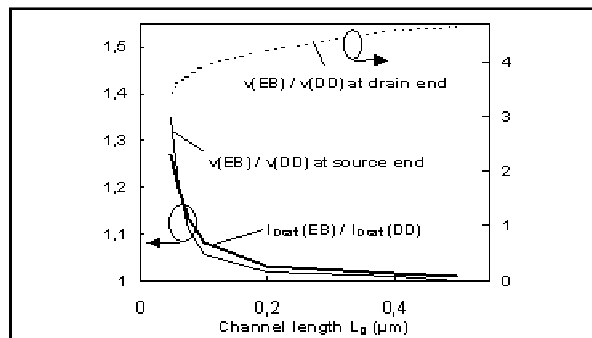

Figure 6. Variation of ratio I_{Dsat}(EB)/I_{Dsat} (DD) and v(EB)/v(DD) at source and drain end as a function of the gate length (V_G=V_D=1.5V).

Implanted Dose ($x10^{14}cm^{-2}$)		v_{source} (_10^7cm/s)	$I_{Dsat(EB)}/I_{Dsat(DD)}$
Channel	0.1	0.97	1.34
(LDD dose:	0.2	0.73	1.31
0.8 $x10^{14}$)	0.3	0.58	1.28
LDD	0.5	0.54	1.22
(Channel dose:	1	0.78	1.33
3 $x10^{13}$)	2	1.14	1.45

Table 1. Impact of channel/LDD doping (L=50nm) on source velocity and drain current.

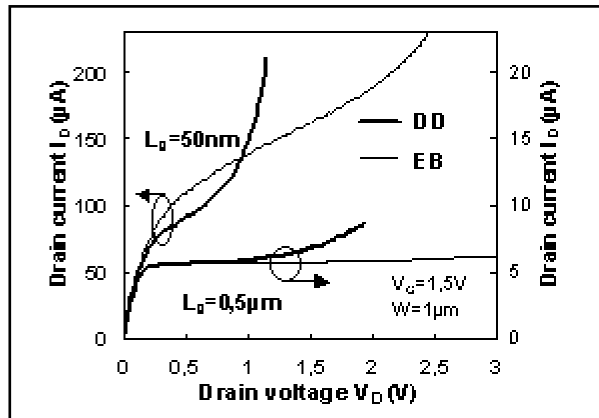

Figure 7. $I_D(V_D)$ curves obtained by EB and DD with impact ionization model at different L_g.

controlled [5]. Indeed, Figure 5 shows that the source velocity increases for shorter channels (because of a higher electric field at the source end), which is reflected by a higher current. The argument of source-side controlled current is also confirmed by the current enhancement in EB compared with DD (Figure 6). At the drain side the ratio between velocity (v) in EB and DD is about 3.5 for L_g=50nm, while the current increases only by 30%. This last value is in good agreement with the ratio between velocities in EB and DD at the source side. The same conclusions are obtained for longer channels (Figure 6).

Channel/LDD doping. For lower channel doping or higher LDD doping, the electric field at the source side increases, which implies a higher velocity (Table 1). However, changes in doping imply V_T variations, which makes difficult the evaluation of the impact of doping induced-velocity enhancement on I_D. A first order decorrelation of the two effects can be obtained by taking into account the ratio $I_{Dsat}(EB)/I_{Dsat}(DD)$. Higher velocity is reflected by a more important increase in the drain current, independent on doping (Table 1). This result opens the perspective of specific engineering of the access regions (LDD, pockets, channel doping) to improve injection velocity, *separately* of V_T adjustments. This type of evaluation only begins to appear in the literature [6].

We have also verified the importance of using realistic devices: simulations on simplified structures overestimate the impact of non-stationary effects on the terminal currents.

Finally, it is important to note that quantum effects will have to be taken into account for a more accurate analysis of the impact of velocity overshoot on drain current.

4.2. Impact ionization

While the classical DD model can be satisfactory for simulating channels longer than 0.25µm, impact ionization needs an energy dependent-model even at much higher lengths. The DD model depends on electric field, which leads to a strong over-estimation of impact ionization for all channel lengths.

Figure 7 presents $I_D(V_D)$ curves for short and long channels, illustrating the over-estimation of the avalanche region by the DD model. Therefore EB model must be used for impact ionization at all channel lengths. Accurate simulation of impact ionization is a very important issue for simulating substrate current and hot carrier effects in bulk devices. This is also a critical point for reproducing accurate ID(VD) curves and kink region in partially depleted SOI devices [7].

5. Conclusion

In this paper we have presented the impact of the modeling level on the electrical behavior of 50nm bulk MOSFET technology. For accurate conclusions, realistic devices have been considered in simulation. The current enhancement due to non-stationary effects must always be referred to the velocity at the source side of the device, and not to drain side. For reproducing the impact of velocity overshoot advanced models are necessary for channel lengths below 0.25µm, while for impact ionization an energy dependent model must be considered even for much higher dimensions. An original analysis in this work is the quantitative evaluation of technological parameters impact on injection velocity and drain current. The results show that for taking full advantage of non-stationary effects on device performances specific engineering of access regions have to be envisaged.

References

[1]. M. Fischetti, S. Laux, Phys. Rev.B, no.14, p.9721, 1988.

[2]. ***ATLAS** Users Manual*, Silvaco.

[3]. C. Caillat et al., 1999 VLSI Tech. Dig., p. 89-90.

[4]. C. Jungeman et al., Proceedings ESSDERC 1999, p. 236.

[5]. G. Baccarani et al., Solid State Electronics, vol. 28, no.4, p. 407, 1985.

[6]. S. Odanaka, A. Hiroki, IEEE Trans. on Electron Dev., vol. 44, no. 4, p. 595, 1997.

[7]. D. Munteanu et al., Proceedings of International SOI Conference, p. 58-59, 2000.

Calendar of Events

November

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5	2000 GaAs IC Tech - Seattle WA
6	2000 GaAs IC Tech - Seattle WA ICCAD 2000 - San Jose, CA
7	2000 GaAs IC Tech - Seattle WA ICCAD 2000 - San Jose, CA
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December

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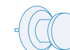
Bulletin Board



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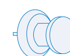

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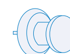

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Hints, Tips and Solutions

William French, Applications and Support Manager

Q. Can ***ATLAS*** be used to perform large signal sinusoidal analysis ?

A. The ***ATLAS*** syntax is flexible enough to allow the definition of sinusoidal nodal voltages by defining them on the SOLVE statement line. To illustrate this the structure shown in Figure 1 has been used. Before the sinusoidal pulse is applied a dc operating condition is set with

```
Vcollector=2V
Vbase=0.7V
Vemitter=0V
```

The sinusoidal pulse is then specified on the SOLVE statement as a part of a transient analysis run. For instance the syntax

```
SOLVE TRANS.ANALY FREQUENCY=5.0e8 \
VBASE=0.8 TSTOP=2.0e-8 TSTEP=3.125e-11 \
CYCLES=10
```

will result in a sinusoidal waveform with a magnitude of (VBASE-Vdc)=(0.8-0.7)=0.1V with a frequency of FREQUENCY and continue on for a maximum of 10 cycles. When applied to the structure in Figure 1 the resultant base voltage vs time characteristic is shown in Figure 2. As shown the curve appears fairly "uneven" which is caused by the internal timestep control producing nonlinear time steps. Although, each solution is correct the user may wish to produce a more smoothly varying response. This may be obtained by defining a smaller tolerance for the time step algorithm, for instance with the syntax

```
METHOD NEWTON  TOL.TIME=1e-6
```

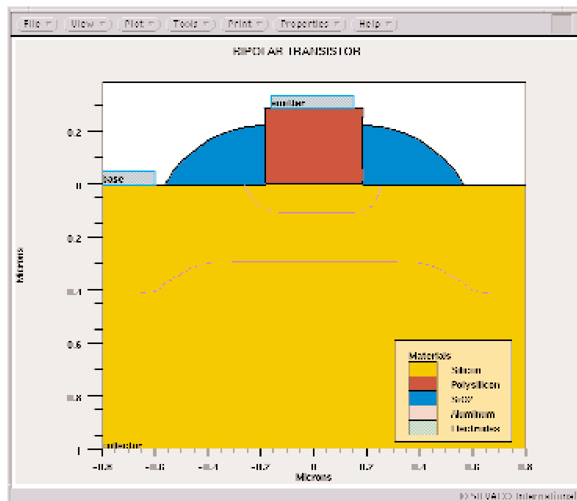

Figure 1: Two-dimensional structure of a BJT used in this study.

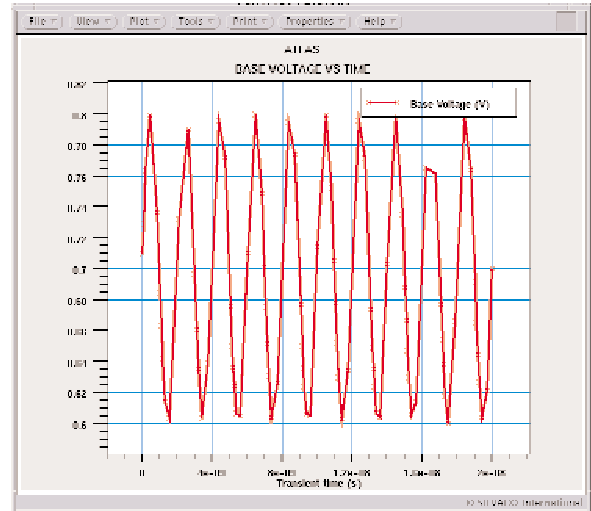

Figure 2: Simulated base voltage versus transient time from Atlas. Although the simulation converges correctly the sinusoidal curve has not been well reproduced.

The resultant curve is shown in Figure 3 where the sinmusoidal curve has become much smoother.

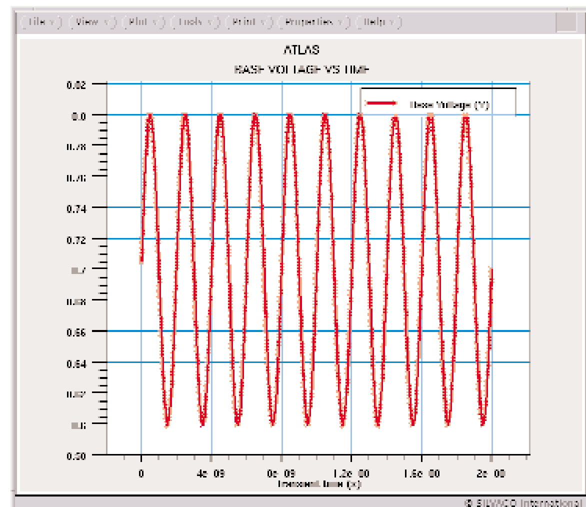

Figure 3: Simulated base voltage versus transient time from Atlas with an improved tolerance set on transient time stepping algorithm.

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