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Modeling and Parameter Extraction Technique for HV MOS Devices with BSIM3v3

Takao Myono, SANYO Electric Co., Ltd.

1. Introduction

We have developed several kinds of HV MOS devices whose device structures and doping levels in the offset regions differ depending on the specifications of the devices. We have developed the bi-directional HV MOS device (e.g., it can be used as a bi-directional MOS switch) with both drain and source offset regions, and we previously described its SPICE model [4] – [5] based on BSIM3v3 [1] – [3]. On the other hand, the uni-directional HV MOS device has only a drain offset region. That is, it does not have a source offset region with corresponding source resistance.

In this paper, I have used the same technique to model uni-directional HV MOS devices as previously reported for bi-directional HV MOS devices [4] – [5] while adopting a new parameter extraction technique. With the new uni-directional HV MOS modeling technique, the simulated I-V characteristics of the uni-directional *n*-channel HV MOS device match the measured characteristics well, which confirms its effectiveness.

2. Uni-directional HV MOS Device Technology

Figure 1 shows the structure of our 45 V *n*-channel HV MOS device, with a gate-oxide film thickness (Tox) of 1350Å, channel length (L) of 3.2µ m and offset of 3.2µ m. A n-offset region of low doping concentration is used in the drain region, in order to realize high uni-directional drain-source breakdown voltage. Based on our device simulations, we consider that the basic operation of the bi-directional HV MOS device is as explained below , and this is also valid for the uni-directional HV MOS device. When drain-source voltage (V_{ds}) is applied to the HV MOS device, a depletion region grows in the *n*- offset. The effect of the electric field from the gate electrode on the depletion region causes the drain-side channel terminal voltage to saturate at a low voltage. This reduces the voltage across the channel, and hence increases the breakdown voltage between the drain and source. Moreover, as the drain-side channel terminal voltage saturates in the triode region, g_m is reduced.

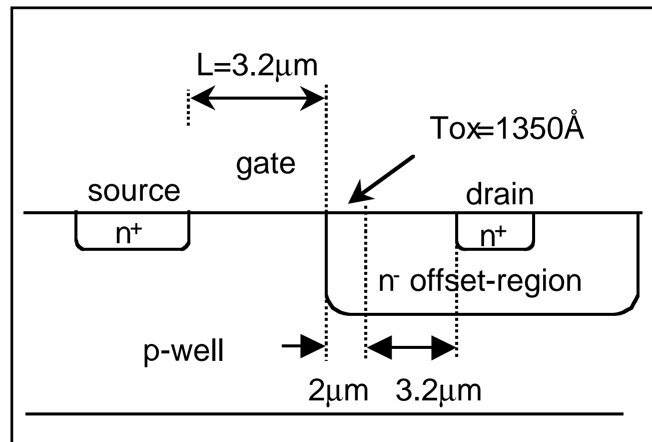

Figure 1. Schematic structure of the uni-directional n-channel HV MOS device.

3. Application of Bi-directional HV MOS Model to Uni-directional HV MOS Device

In this section, I directly apply the bi-directional HV MOS model and its parameter extraction technique to the uni-directional HV MOS device, and investigate the results. The bi-directional HV MOS model parameter extraction technique is outlined below [4] – [5]:

1) First, extract all BSIM3v3 parameters by the standard method.

2) Then set the value of *VSAT* to a large value (e.g., $1x10^9$ m/sec) assuming a long-channel device.

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3) Optimize AGS and $DELTA$ at the same time. This is to optimize the saturation voltage of the drain-side channel terminal V_{dsat} and the source resistance due to the offset region.

Using the above procedure for the bi-directional HV MOS device, the parameter AGS optimizes V_{dsat} and source resistance in a well-balanced manner, and the measured and simulated I-V characteristics match well. Furthermore, this method can precisely reproduce the g_m-reduction phenomenon, which is inherent to HV MOS devices. On the other hand, step II in Table 1 shows the parameters obtained by directly applying the bi-directional HV MOS device model and parameter extraction technique to the uni-directional HV MOS device, and Figure 2 shows a comparison of the measured and simulated I-V characteristics. In Figure 2 large discrepancies are observed between the measured and simulated I-V characteristics.

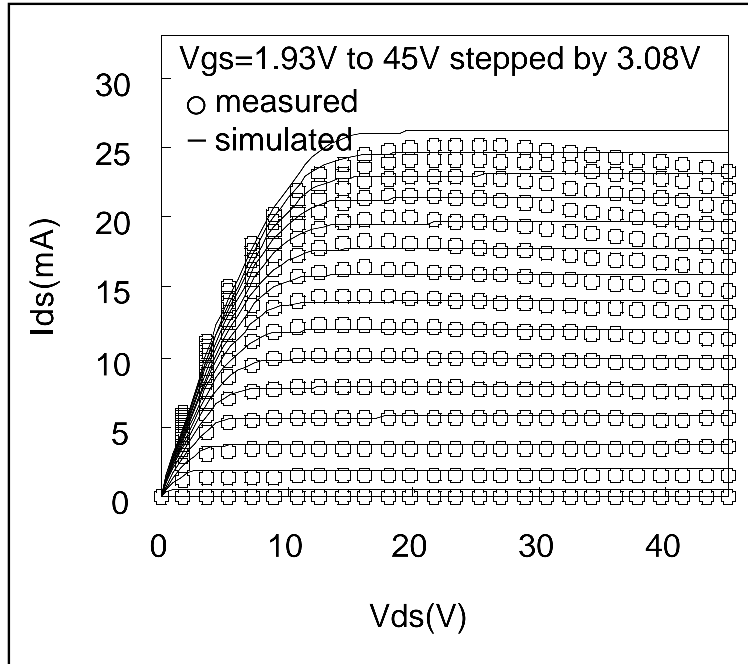

Figure 2. Comparison between measured and simulated. (with the bi-directional HV MOS model) I-V characteristics of the 45V HV MOS device.

4. Proposed Uni-directional HV MOS Device Modeling Technique

In this section I propose a uni-directional HV MOS modeling technique: I use the bi-directional HV MOS model in [4] – [5] as a basis, and the main equations are as follows:

$$G_{ds0} = \mu_{eff} \frac{\varepsilon_{ox}}{T_{ox}} \frac{W}{L} \left(V_{gs} - V_{rs} - V_{th} - \frac{V_{ds}}{2} \right), \quad (1)$$

$$V_{rs} = (A_{bulk} - 1) \frac{V_{ds}}{2}, \quad (2)$$

$$I_{ds} = \frac{G_{ds0} V_{ds}}{1 + G_{ds0} R_{ds}}, \quad (3)$$

$$A_{bulk} \equiv f_1 (AGS, V_{gs}), \quad (4)$$

$$V_{dsat} \approx \frac{V_{gs} - V_{th}}{A_{bulk}} \equiv f_2 (AGS, V_{gs}), \quad (5)$$

$$V_{ds} = V_{dseff} \equiv f_3 (AGS, DELTA, V_{ds}, V_{gs}). \quad (6)$$

Here, W is the channel width, μ_{eff} is the effective mobility, ε_{ox} is the permitivity of the silicon-oxide film, V_{th} is the threshold voltage, AGS is the gate bias coefficient of the A_{bulk}, V_{dsat} is the saturation value of the drain-side channel terminal, V_{dseff} is the effective drain-source voltage and $DELTA$ is the effective drain voltage smoothing parameter of V_{dseff}. Where, V'_{ds} is the drain-side channel terminal voltage, which is equivalent to the V_{dseff} of BSIM3v3.

V_{rs} is voltage drop across the source resistance in the offset region. It cannot be eliminated from equation (1) as V_{rs} is inherent for the bi-directional HV MOS model with BSIM3v3. Hence, it is necessary to compensate for part of the drain current component by V_{rs} in equation (1) for the uni-directional HV MOS model. Here, I define the drain current I_{drs0} in which the voltage Vrs in equation (1) is eliminated as shown below. I_{dsr0} is a model equation for the uni-directional HV MOS device model.

$$G_{dsr0} = \mu_{eff} \frac{\varepsilon_{ox}}{T_{ox}} \frac{W}{L} \left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right), \quad (7)$$

$$I_{dsr0} = \frac{G_{dsr0} V_{ds}}{1 + G_{dsr0} R_{ds}}. \quad (8)$$

Further, by defining I_{vrs} as the variable component of drain current due to V_{rs}, I obtain the following expression:

$$I_{ds} = I_{dsr0} - I_{vrs}. \quad (9)$$

The above expression indicates that the way to compensate for I_{vrs} in the uni-directional HV MOS model is to optimize I_{dsr0} by making it larger than I_{ds} by the value of I_{vrs}. Here it can be assumed that the value of I_{ds} is equivalent to the measured data. Suppose the parameter AGS is set to a large negative value, the value of A_{bulk} in equation (4) increases, which in turn decreases the value of V_{dsat} in equation (5) and results in

decreasing the value of I_{dsr0}. At the same time, A_{bulk} increases the value of I_{vrs} larger. So, A_{GS} cannot optimize V_{dsat} correctly, and I_{ds} cannot represent the g_m-reduction (refer to section 7.). In addition, the value of I_{vrs} cannot be obtained directly by calculation; instead use the following equation:

$$I_{vrs} = I_{dsr0} - I_{ds} \,. \qquad (10)$$

I propose the following model which can express the g_m-reduction.

1) BSIM3v3 SPICE model combines the source and drain resistance with R_{ds} (whose value depends on V_{gs}) as follows:

$$R_{ds} = \frac{RDSW\left(1 + PRWG \cdot V_{gs}\right)}{W}, \qquad (11)$$

where $RDSW$ is the source and drain resistance per unit channel width and $PRWG$ is a V_{gs} coefficient. R_{ds} is incorporated in the drain current expression of the simplified model as an explicit function of G_{ds0} shown in equation (3), and R_{ds} hardly affects the saturation voltage (V_{dsat}) of BSIM3v3. Note that G_{ds0} has R_{ds} in its denominator, and by making Rds a function of V_{gs}, it is possible to accurately express the gm-reduction for I_{dsr0} and I_{ds} mathematically.

2) R_{ds} provides the g_m-reduction for I_{dsr0} and I_{ds}, but they are not the same. I_{dsr0} with a larger absolute value has larger g_m-reduction, so that it can give most appropriate g_m-reduction in order to compensate the value of I_{vrs}, which is $I_{dsr0} - I_{ds}$.

3) R_{ds} has little influence on V_{dsat}, and it can be utilized independently of AGS.

4) AGS can be used to optimize the absolute value of I_{ds}, through V_{dsat}.

5) For HV MOS devices, both V_{gs}-caused mobility degradation effect and gm-reduction occur at the same time and influence of the latter is more predominant. So in the HV MOS model, it is possible to ignore the mobility degradation effect. By defining μ_{eff} as a constant regarding to V_{gs}, we can obtain about five times faster optimization of the parameters for the parameter extraction tool.

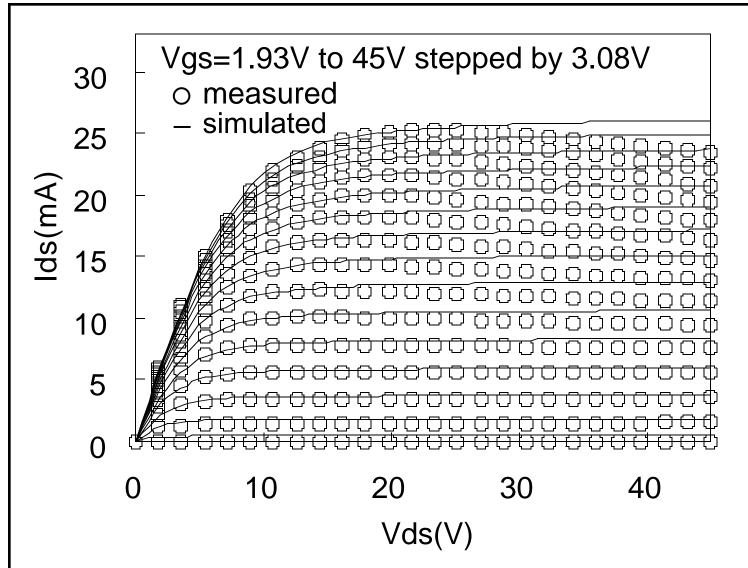

Figure 3. Comparison between the measured and simulated (with the uni-directional model) I-V characteristics of the 45V n-channel HV MOS device.

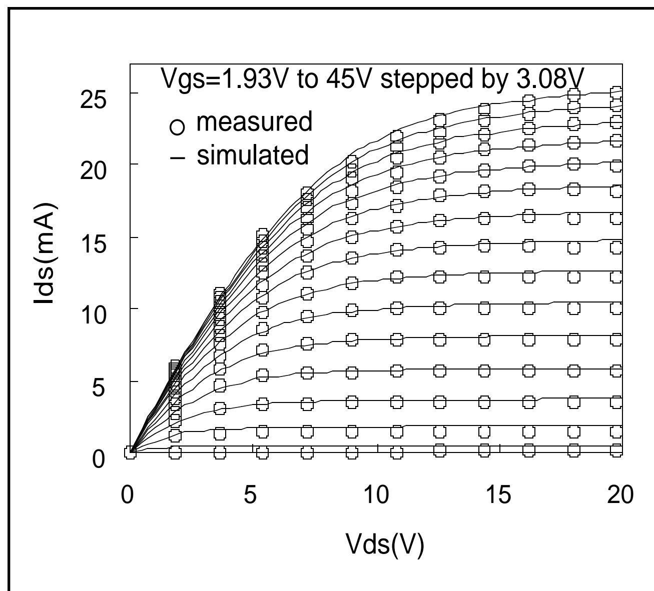

Figure 4. Comparison between the measured and simulated (with the uni-directional HV MOS model and PCLM=0) I-V characteristics in the triode region.

5. Proposed Parameter Extraction Technique for Uni-Directional HV MOS Device Modeling

In this section I describe the proposed parameter extraction technique for the uni-directional HV MOS model which can be implemented by using a SPICE model parameter extraction system, such as ***UTMOST*** [6].

1) First, extract all BSIM3v3 parameters by the standard method (step I in Table 1).

2) Then set the value of $VSAT$ to a large value (e.g., $1x10^9$) assuming the long channel model.

3) Optimize the parameters of $U0$, $RDSW$, $PRWG$, AGS, and $DELTA$ together in all the triode region (up to close to the saturation region) i.e., from (V_{ds}=0V, V_{gs}=1.93V) to (V_{ds}=20V, V_{gs}=45V). $RDSW$

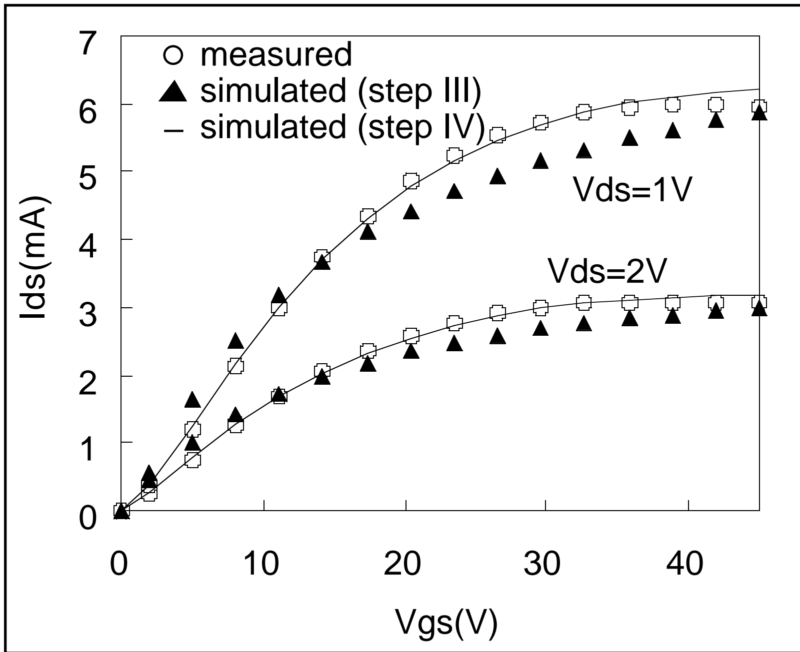

Figure 5. Comparison between the measured and simulated (with the uni-directional HV MOS model) Ids-Vgs characteristics in triode region.

and *PRWG* have to be optimized such that R_{ds} expresses g_m-reduction of I_{dsr0} while *AGS* has to be optimized such that A_{bulk} and V_{dsat} compensate for I_{vrs}.

4) Optimize *PDIBLC1* and *PDIBLC2*

Since optimization of the absolute value of I_{ds} and g_m interact with each other, it is necessary to optimize them simultaneously. Step III in Table 1 shows extracted parameter values based on the above procedure, and Figure 3 shows a comparison between the measured and simulated I-V characteristics. I see that good agreement is obtained between the measured and simulated results (except for the region where negative g_{ds} appears.).

In Figure 3, accuracy of simulation decreases in the linear region with higher value of V_{gs}. This is because R_{ds} provides the g_m-reduction in all the region. However, g_m-reduction due to the drain-side offset region appears only in the saturation region. To compensate for the worsening accuracy, it is effective to implement Step III again by setting the channel length modulation parameter *PCLM=0* (or optimize). The 0 value of *PCLM* amplifies the g_m-reduction in the saturation region, so that V_{gs} dependence of R_{ds} is optimized smaller (Step IV in table 1). As a result of this, gm-reduction caused by Rds in the linear region gets smaller. Step IV in Table 1 shows the parameters with *PCLM=0* and Figure 4 shows the comparison between the measured and simulated I-V characteristics in the triode region. Figure 5 shows I_{ds}-V_{gs} characteristics in triode region. Note that I_{ds} monotonically increases under the condition of $V_{gs} \geqq 40$V, however, Ids slightly decreases when $V_{gs} \geqq 40$V, and this phenomenon is more predominant when V_{ds} = 1V than V_{ds} = 2V. This is due to the decrease of the channel voltage of the drain terminal by the influence of the gate electric field.

	AGS	U0	UA	RDSW	PRWG
Step I	0.084	616	$0.7x10^{-8}$	$3.8x10^{3}$	0.0
Step II	-0.049	520	$0.4x10^{-8}$	$3.8x10^{3}$	0.0
Step III	-0.076	463	0.0	$1.9x10^{3}$	0.092
Step IV	-0.077	588	0.0	$5.5x10^{3}$	0.018

Table 1. Extracted BSIM3v3 Parameter Values for each step.

References

[1] Y. Cheng, M.-C. Jeng, Z. Liu, J. Hubg, M. Chen, P. K. Ko and C. Hu, "A Physical and Scalable I-V Model in BSIM3v3 for Analog/Digital Circuit Simulation, " IEEE Electron Devices, vol.44, no.2, pp.277-284 (Feb. 1997).

[2] J. H. Huang, Z. H. Liu, M. C. Jeng, K. Hui, M. Chan, P. K. Ko and C. Hu, BSIM3 Manual (version 2.0), University of California, Berkeley, (1994).

[3] BSIM3v3 Manual (final version), University of California, Berkeley,(1995).

[4] T. Myono, S. Kikuchi, K. Iwatsu, E. Nishibe, T. Suzuki, Y. Sasaki, K. Itoh and H. Kobayashi, "High-Voltage MOS Device Modeling with BSIM3v3 SPICE Model, "IEICE TRANS. ELECTRON, vol.E82-C, No.4, pp630-637, (April 1999).

[5] T. Myono, E. Nishibe, S. Kikuchi, K. Iwatsu, T. Suzuki, Y. Sasaki, K. Itoh and H. Kobayashi, " Modeling and Parameter Extraction Technique for High-Voltage MOS Device", Proc. of International Symposium on Circuits and Systems, pp.230-233, Orlando Florida (June 1999).

[6] UTMOST III Extraction manual,vol.1, ver. 12.03, SILVACO International, Santa Clara, C

New RF MOSFET Small Signal SPICE Model

Part 2

Ickjin Kwon, Minkyu Je, Kwyro Lee, and Hyungcheol Shin
Department of Electrical Engineering, Korea Advanced Institute of Science and Technology

Parameter Extraction Procedure

RF MOSFET Small –Signal Model and Parameters

Small-signal equivalent circuit of MOSFET after de-embedding parasitics is shown in Figure 1 and small-signal model parameters are listed in Table 1.

Parameter Extraction Strategy

Parameter extraction is performed from real and imaginary parts of the Y-parameters. Each parameter is extracted from the Y-parameter equations which contain frequency terms.

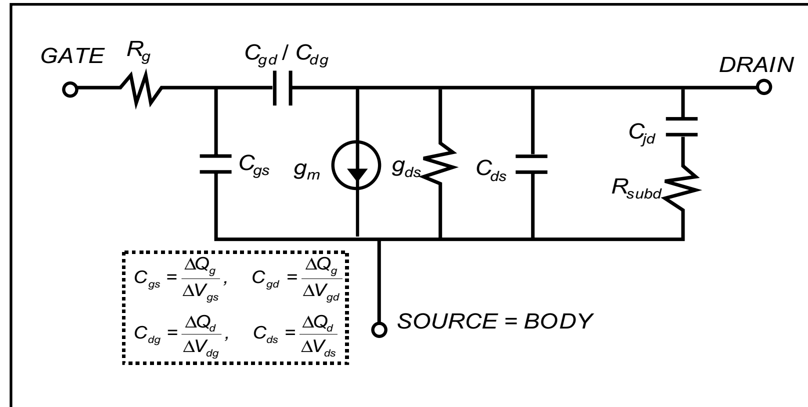

Figure 1. Common-source equivalent circuit of a MOSFET after de-embedding parasitics of on-wafer pads and interconnection lines.

To fit a straight line to the data plot, linear regression is used.

With the X data, the independent variable, and the Y data, the dependent variable, the estimated linear regression model is stated;

$$Y_i = A + BX_i$$

where the parameters, A and B, are estimated by the method of least squares.

A is the intercept :

$$A = \overline{Y} - B\overline{X}$$

B is the slope :

$$B = \frac{\sum_{i=1}^{N}(X_i - \overline{X})(Y_i - \overline{Y})}{\sum_{i=1}^{N}(X_i - X)^2}$$

The standard deviation is defined as

$$\sqrt{\frac{\sum_{i=1}^{N}(Y_i - (A+BX_i))^2}{N-2}}$$

Where (X_i, Y_i) are the data points, N is the number of data points,

$$\overline{X} = \frac{1}{N}\sum_{i=1}^{N} X_i, \text{ and } \overline{Y} = \frac{1}{N}\sum_{i=1}^{N} Y_i$$

Parameters such as C_{gd}, C_{gs}, R_g, C_{dg}, C_{jd}, and C_{ds} are extracted as a function of frequency and in these cases the extracted values are determined by their mean value. The mean of parameter is calculated by

$$\overline{P} = \frac{1}{N}\sum_{i=1}^{N} P_i$$

where P_i are the extracted parameter values as a function of frequency.

Small Signal Model Parameters	Physical Meaning	Unit
g_m	Transconductance	A/V(S)
g_{ds}	Drain Conductance	A/V(S)
C_{gd}	Gate-to-Drain Capacitance	F
C_{gs}	Gate-to-Source Capacitance	F
R_g	Gate Resistance	Ω
C_{dg}	Drain-to-Gate Capacitance	F
R_{subd}	Substrate Resistance	Ω
C_{jd}	Drain Junction Capacitance	F
C_{ds}	Drain-to-Source Capacitance	F

Table 1. Small-signal parameters of RF MOSFET and their physical meaning and unit of parameters.

Extraction Routine

* Note that, ω = 2 <–> π <–> .

Step 1.

g_m is obtained from y-intercept of Re[Y_{21}] versus ω^2 .

Extracted Parameter	Required Equation
g_m	$Y = \text{Re}\ (Y_{21})$ $X = \omega^2$ $Y = A_1 + B_1\ X$ $g_m = Re\ [Y_{21}]\|_{\omega^2=0} = A_1$

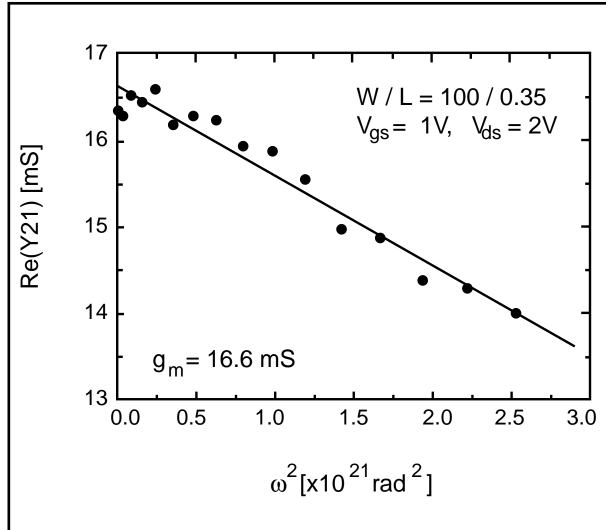

Figure 2. Extraction results of g_m.

Step2.

g_{ds} is obtained from y-intercept of Re[Y_{22}] versus ω^2 .

Extracted Parameter	Required Equation
g_{ds}	$Y = \text{Re}\ (Y_{22})$ $X = \omega^2$ $Y = A_2 + B_2\ X$ $g_m = Re\ [Y_{22}]\|_{\omega^2=0} = A_2$

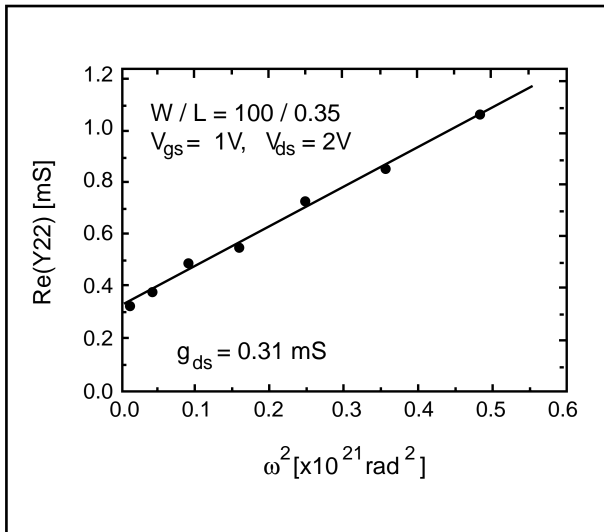

Figure 3. Extraction results of g_{ds}.

Step 3.

Extracted Parameter	Required Equation
C_{gd}	$C_{gd} = \dfrac{-\text{Im}[Y_{12}]}{\omega}$

* Extracted C_{gd} is the mean value as a function of frequency.

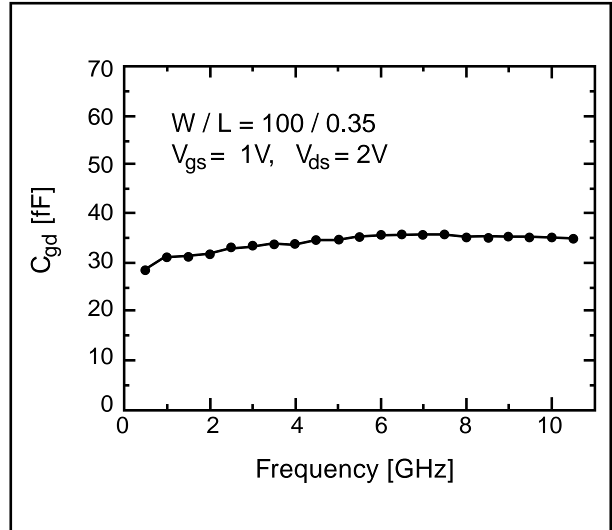

Figure 4. Extraction results of C_{gd}.

Step 4.

Extracted Parameter	Required Equation
C_{gs}	$C_{gs} = \dfrac{\text{Im}[Y_{11}]+\text{Im}[Y_{12}]}{\omega}$

* Extracted C_{gs} is the mean value as a function of frequency.

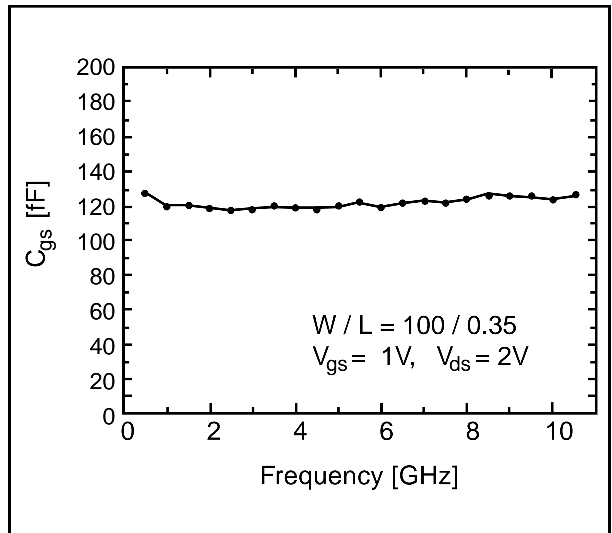

Figure 5. Extraction results of C_{gs}.

Step 5.

Extracted Parameter	Required Equation
R_g	$R_g = \dfrac{\mathrm{Re}[Y_{11}]}{(\mathrm{Im}[Y_{11}])^2}$

* Extracted Rg is the mean value as a function of frequency.

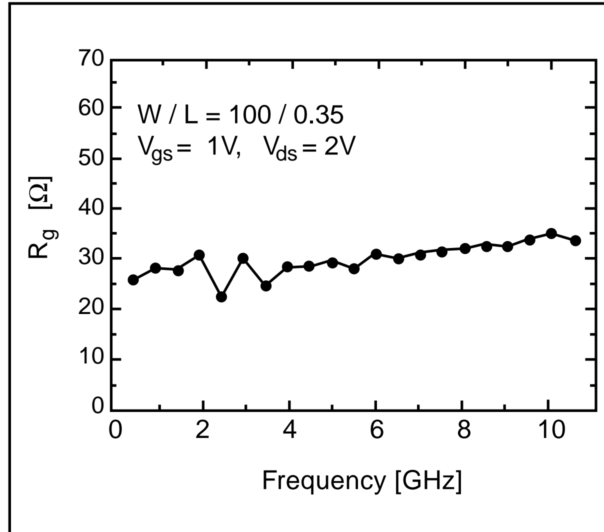

Figure 6. Extraction results of R_g.

Step 6.

Extracted Parameter	Required Equation
C_{dg}	$C_{dg} = -\mathrm{Im}[Y_{21}]/\omega - g_m R_g (C_{gs}=C_{gd})$

* Extracted Cdg is the mean value as a function of frequency.

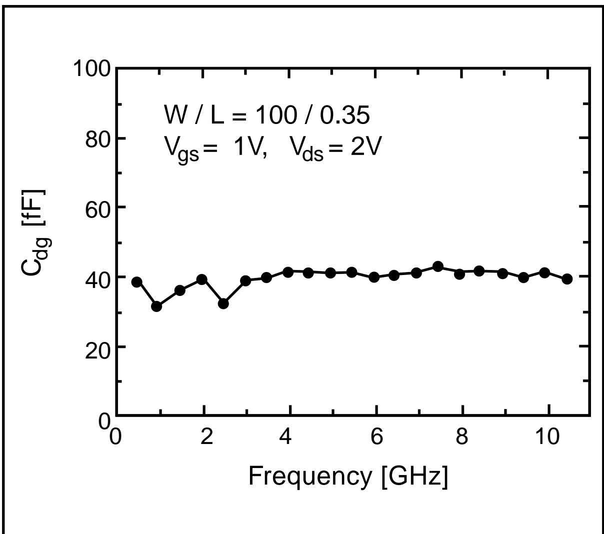

Figure 7. Extraction results of C_{dg}.

Step 7.

R_{subd} and C_{jd} are obtained from linear regression using the following relation.

$$Y = \frac{\omega^2}{\mathrm{Re}[Y_{22}] - g_{ds} - \omega^2 C_{gd} C_{dg} R_g - \omega^2 g_m R_g^2 C_{gd}(C_{gs} C_{gd})} = \omega^2 R_{subd} + \frac{1}{C_{jd}^2 R_{subd}}$$

R_{subd} is determined from slope of Y as a function of ω^2.

Extracted Parameter	Required Equation
	$Y = \dfrac{\omega^2}{\mathrm{Re}[Y_{22}] - g_{ds} - \omega^2 C_{gd} C_{dg} R_g - \omega^2 g_m R_g^2 C_{gd}(C_{gs}+C_{gd})}$

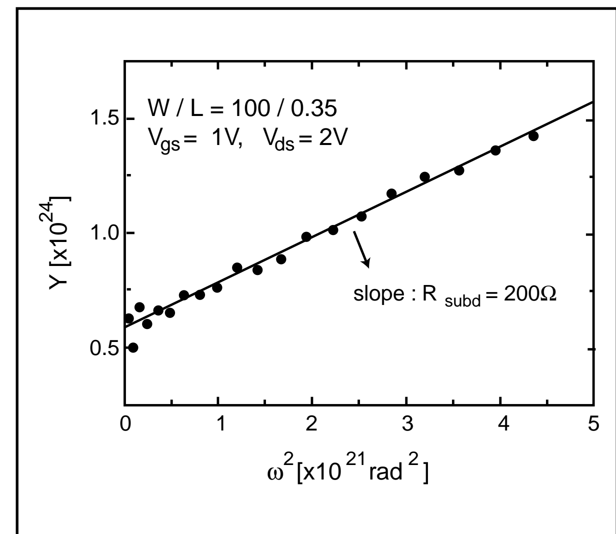

Figure 8. Extraction results of R_{subd}.

Step 8.

Extracted Parameter	Required Equation
C_{jd}	$C_{jd} = [(Y - \omega^2 R_{subd}) R_{subd}]^{-1/2}$

* Extracted Cjd is the mean value as a function of frequency.

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UFSOI: Process-Based Compact SOI MOSFET Models

Jerry G. Fossum, Mario M. Pelella, and Meng-Hsueh Chiang
Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611, U.S.A.

Introduction

SOI technology appears now to have become an advantageous, viable option for low-voltage and high-performance CMOS integrated circuits in digital, analog, and mixed-signal applications. The thin-film nature of the SOI MOSFET, however, can underlie physical mechanisms that complicate circuit simulation and portend equivocation in design. For example, floating-body (FB) effects [1], which in fact are obtained even in body-tied devices due to unavoidable high resistance [2], render empirical compact models like those used for designing bulk-Si CMOS circuits inadequate for reliable SOI circuit simulation. Furthermore, such models cannot be easily calibrated using common parameter-optimization techniques because of ambiguous data acquisition implied by SOI device self-heating in DC measurements and/or FB charge dynamics in pulse measurements designed to avoid self-heating; such optimization, because of the complex body charging dynamics, does not and cannot cover the large range of operational conditions that obtain in actual SOI CMOS circuits. Consequently, Silvaco has incorporated the physical process-based UFSOI MOSFET models [3] into ***SmartSpice*** and ***UTMOST***.

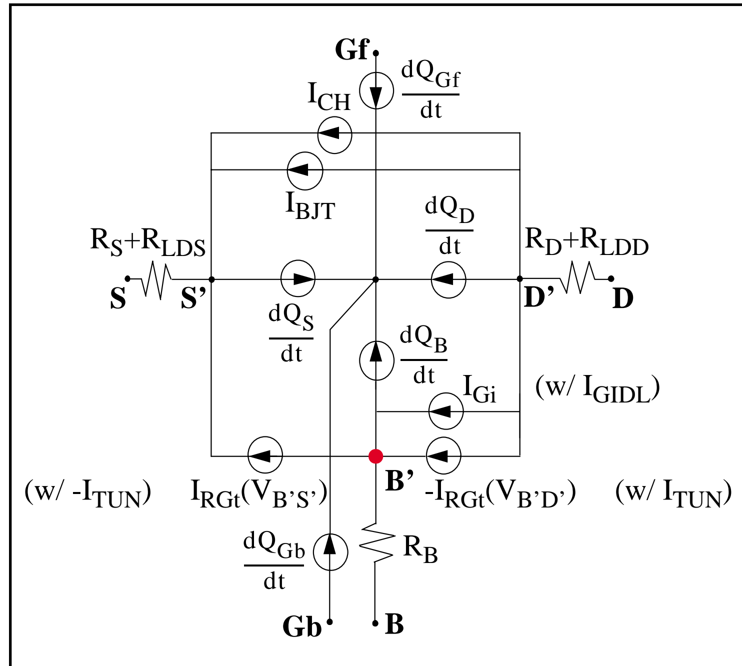

Figure 1. Network representation of the processed-based UFSOI (NFD and FD) MOSFET models.

Model Description

The UFSOI implementation includes options for both the partially, or non-fully depleted (NFD) model [4] and the fully depleted (FD) model [5]. As illustrated by the network representation in Fig. 1, the models are charge-based with five terminals, and they have the FB option. The NFD model physically accounts for dynamic as well as DC FB effects in all regions of operation. The FD model physically accounts for the charge coupling between the front gate and back gate (substrate). Both compact models account for all the important features and mechanisms prevalent in scaled SOI MOSFETs, which include polysilicon-gate depletion, quantization due to quantum-mechanical carrier confinement, non-local carrier temperature-dependent impact-ionization current (I G_i) [6] and velocity overshoot, and the parasitic bipolar transistor (BJT) currents and charges [7], which are properly coupled to the MOS currents and charges; the BJT base (body) current can comprise thermal generation, GIDL, junction tunneling, and impact-ionization currents. The noise (thermal, flicker, and shot) modeling accounts for hot-carrier effects on the channel thermal noise, important at high frequencies, and, with the implicit transimpedances, has been shown to predict the low-frequency Lorentzian excess noise component well [8]. The temperature modeling is truly physical [9], involving no extra parameters, and it is the basis of the self-heating option which uses a single-pole thermal subcircuit for each device. The FD model further accounts for the 2D source/drain field fringing in the back oxide (BOX), and the induced back-channel current (in weak/moderate inversion) [5]. The NFD model further accounts for nonuniform channel doping (e.g., via retrograde [4] and halo options), and its control of short-channel and parasitic BJT effects.

All currents and charges and their derivatives, which form the basis of the UFSOI quasi-static formalism, are continuous in all regions of operation [10]. The characterization of body charge (Q_B) in the FD model accounts for accumulation charge, which means that the model is hybrid-FD/NFD with regard to charge dynamics; in the FD (on) state, dQ_B /dt 0, which means that most FB effects are suppressed. In the NFD model, Q_B is defined by neutrality, which means that the charge dynamics properly reflects all the intrinsic transcapacitances. The FB effects are implicitly accounted for in the UFSOI models by proper merging of the carrier

generation/recombination currents, the BJT and channel currents, and the charging, or transcapacitance currents. The merging, which is unified for DC, AC, or transient simulations, is reflected by the floating-body (B') nodal equation indicated in equation 1:

$$\frac{dQ_B}{dt} = I_{Gi} - I_{RGt}(V_{B'S'}) - I_{RGt}(V_{B'D'}) \quad (1)$$

where neutrality implies

$$Q_B = -(Q_S + Q_S + Q_{Gf} + Q_{Gb}). \quad (2)$$

The combination of (1) and (2) defines V_{BS} and V_{BD} for any condition, and thereby describes how the intrinsic capacitive coupling and/or the recombination/generation in the device govern the FB effects as usually reflected by I_{CH} (V_{BS}) and/or I_{BJT} (V_{BS}).

The truly physical nature of the UFSOI models renders their formalisms implicit, meaning that Newton-like iterative solutions have to be derived. Further, the derivatives (transconductances and transcapacitances) needed for the nodal analysis have been computed via difference approximations, necessitating five passes through the model routine for each call by SmartSpice. Recently, however, the use of approximate analytical derivatives for the NFD model in DC and transient simulations has been incorporated in UFSOI, with the exception the critical V_{BS} -derivatives; difference approximations still have to be used in AC simulations. The result of this NFD speed-up is a physical yet computationally efficient model, requiring run-times that are not much longer than those required by empirical counterparts.

Process-Based Model Calibration and Utility

What makes the UFSOI models really unique, and, in our opinion, essential for reliable SOI circuit simulation, is their process basis. Key (~20) UFSOI model parameters are either structural or physics-based, and hence they are properly correlated and their evaluation can be done unequivocally in a straightforward manner, using device-structure data and measured data taken only in low-power regions where self-heating is negligible [11]. Such structure-dependent calibration renders the UFSOI models predictive, and useful for sensitivity analyses and next-generation performance projections [12], as well as reliable circuit simulation with devices in all possible regions of operation.

We exemplify this UFSOI utility by considering FB hysteresis in PD/SOI CMOS inverter-based circuits [13]. This hysteresis, first noted via UFSOI model predictions [14], is reflected by history-dependent propagation delays that are due to slow carrier recombination/generation processes superimposed on the fast body charge dynamics driven by the intrinsic capacitive coupling. The hysteresis is thus quite sensitive to the device structure as well as physics-based parameters such as carrier lifetimes. For example, Figure 2 shows a UFSOI-predicted "fast" open-inverter-chain delay in time (from DC to the dynamic steady state) for L eff = 145nm PD/SOI CMOS for two different SOI film thicknesses (t_{SOI}). The "fast" delay is the one corresponding to initially (t = 0) body-charged (V_{DS} =V_{DD} = 1.8V V_{BS} > 0 for the nMOSFETs, V_{BS} < 0 for the pMOSFETs) active devices in the inverter chain; whereas the "slow" delay would correspond to initially uncharged (V_{DS} =0 V_{BS} = 0) active devices. Note that reducing t_{SOI} decreases the delay, but alters the hysteretic variation to an increasing delay with time. These results are due to the varying ratio of the gate-body capacitance to the drain-body capacitance, which increases with decreasing t_{SOI} and tends to increase V BS (t). Thus, early in time, the "current overshoot" in the active device is enhanced; and later in time, a "dynamic strengthening" of the load device occurs. These results, which are consistent with experimental ones, clearly reflect the complexity of dynamic FB effects, and imply why a predictive (process-based) compact model is needed for reliable SOI circuit simulation.

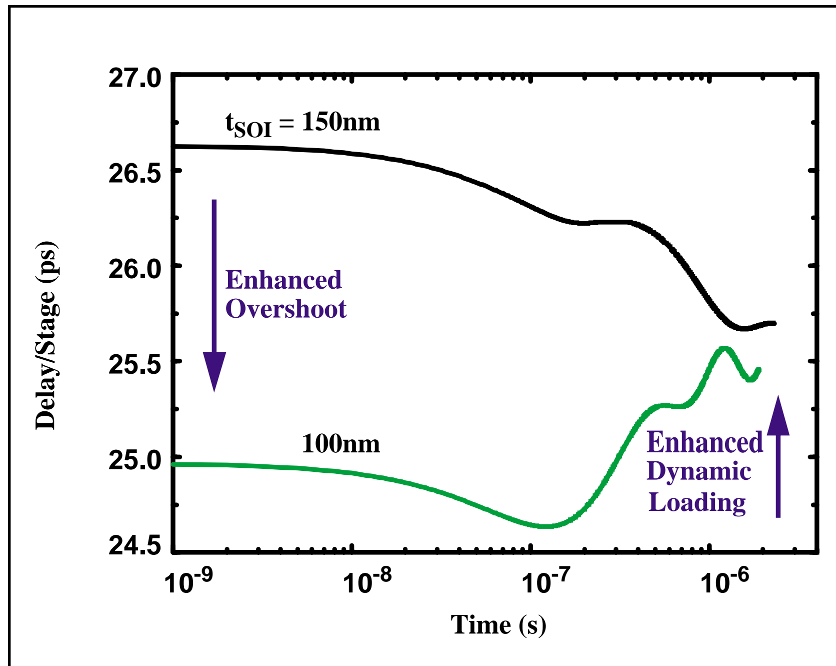

Figure 2. Network representation of the process-based UFSOI (NFD and FD) MOSFET models.

Summary

The process-based UFSOI models have been released to more than 100 companies and universities throughout the world, in addition to the SmartSpice releases. Both models are continually upgraded as the SOI technologies advance. In fact, the UFSOI/ NFD model is now being evolved into a unified process-based compact model for bulk-Si as well as PD/SOI MOSFETs; and the UFSOI/FD model is being upgraded for possible near-50nm node application and is the basis for a process-based model for double-gate MOSFETs now being developed at the University of Florida.

Acknowledgments

The development of UFSOI models at the University of Florida have been supported mainly by the Semiconductor Research Corporation. Many graduate students have made key contributions to the development over several years. The students include D. Chang, J. Y. Choi, L. Ge, K. Kim, H.-K. Lim, D. Suh, S. Veeraraghavan, G. O. Workman, and P. C. Yeh, in addition to coauthors Chiang and Pelella.

References

1. S. Krishnan and J. G. Fossum, IEEE Circuits & Devices, vol. 14, p. 32, July 1998.
2. G. O. Workman and J. G. Fossum, IEEE Trans. Electron Devices, vol. 45, p. 2138, Oct. 1998.
3. J. G. Fossum, "UFSOI MOSFET Models (Ver. 5.0) User's Guide," SOI Group (http://www.soi.tec.ufl.edu), Univ. of Florida, Gainesville, Nov. 1999.
4. D. Suh and J. G. Fossum, IEEE Trans. Electron Devices, vol. 42, p. 728, Apr. 1995.
5. P. C. Yeh and J. G. Fossum, IEEE Trans. Electron Devices, vol. 42, p. 1605, Sept. 1995.
6. S. Krishnan and J. G. Fossum, Solid-State Electron., vol. 39, p. 661, May 1996.
7. S. Krishnan, Ph.D. Dissertation, Univ. of Florida, Gainesville, 1996.
8. G. O. Workman and J. G. Fossum, IEEE Trans. Electron Devices, vol. 47, p. 1192, June 2000.
9. G. O. Workman, J. G. Fossum, S. Krishnan, and M. M. Pelella, Jr., IEEE Trans. Electron Devices, vol. 45, p. 125, Jan. 1998.
10. D. Chang, Ph.D. Dissertation, Univ. of Florida, Gainesville, 1997.
11. M.-H. Chiang and J. G. Fossum, SOI Group Report, Univ. of Florida, Gainesville, Nov. 1998.
12. M. M Pelella and J. G. Fossum, Preprint for IEEE Electron Device Lett., June 2000.
13. M. M. Pelella, J. G. Fossum, M.-H. Chiang, G. O. Workman, and C. R. Tretz, Tech. Digest Internat. Electron Devices Meeting, p. 831, Dec. 1999.
14. D. Suh and J. G. Fossum, Tech. Digest Internat. Electron Devices Meeting, p. 661, Dec. 1994.

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Step 9.

* Extracted C_{ds} is the mean value as a function of frequency.

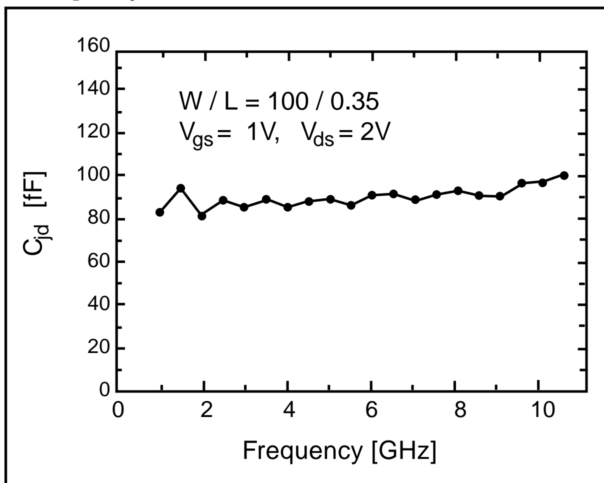

Figure 9. Extraction results of C_{jd}.

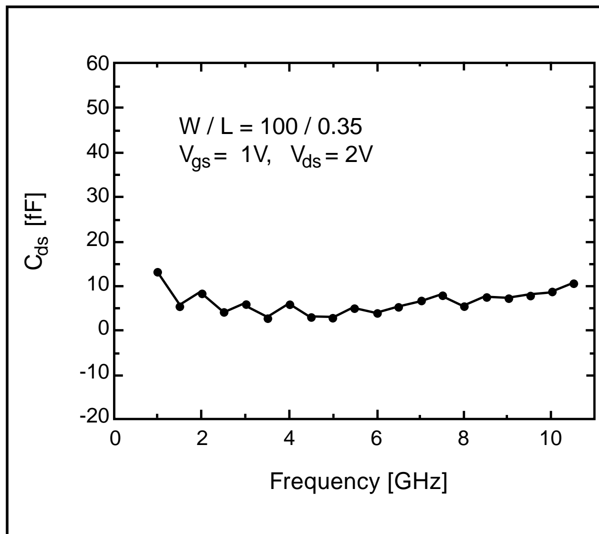

Figure 10. Extraction results of C_{ds}.

Extracted Parameter	Required Equation
C_{ds}	$C_{ds} = \frac{-\mathrm{Im}[Y_{22}]}{\omega} C_{gd} - \frac{C_{jd}}{1 + \omega^2 C_{jd}^2 R_{subd}^2} g_m R_g C_{gd} + \omega^2 C_{gd} C_{dg} (C_{gs}+C_g) R_g^2$

Calendar of Events

July

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5 10th Fine Process Technology - Tokyo
6 10th Fine Process Technology - Tokyo
7 10th Fine Process Technology - Tokyo
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12 7th Intl w/s on Active Matrix and TFT Tech - Tokyo
13 7th Intl w/s on Active Matrix and TFT Tech - Tokyo
14 7th Intl w/s on Active Matrix and TFT Tech - Tokyo
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24 NSREC - Reno, NV
25 NSREC - Reno, NV
26 NSREC - Reno, NV
27 NSREC - Reno, NV
28 NSREC - Reno, NV
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August

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20 2000 Topical on Hetro Structure Microelectronics – Kyoto, Japan
21 2000 Topical on Hetro Structure Microelectronics – Kyoto, Japan
22 2000 Topical on Hetro Structure Microelectronics – Kyoto, Japan
23 2000 Topical on Hetro Structure Microelectronics – Kyoto, Japan
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28 Intl Conf on Solid State Devices and Materials, Sendai, Japan
29 Intl Conf on Solid State Devices and Materials, Sendai, Japan
30 Intl Conf on Solid State Devices and Materials, Sendai, Japan
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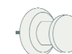
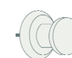
Bulletin Board



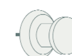
Silvaco Japan on the Move

The office in Japan is off to another busy month with 2 conferences in July. Silvaco's Japanese office is intent on providing the highest level of support to our Asian customers. With a suite of tools that are powerful and which significantly decrease design time it is easy to stand confidently behind Silvaco tools.



Process Technology Conference

July 5th through 7th is the 10th Fine Process Technology conference. Held in the Tokyo, Silvaco is anticipating a large turnout at this important conference. Silvaco's Asian customers continue to be the backbone of the growing success of Silvaco software worldwide.



NSREC Conference

July finishes strong with the Nuclear and Space Radiation Effects Conference (NSREC) held this year in Reno, Nevada. This conference always strengthens Silvaco's relationship with their valued military customers. With new development happening so rapidly in nuclear and space technology, Silvaco enables developers to speed up design times without compromising accuracy.

For more information on any of our workshops, please check our web site at ***http://www.silvaco.com***

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SILVACO
INTERNATIONAL

USA HEADQUARTERS

Silvaco International
4701 Patrick Henry Drive
Building 2
Santa Clara, CA 95054
USA

Phone: 408-567-1000
Fax: 408-496-6080

sales@silvaco.com
www.silvaco.com

CONTACTS:

Silvaco Japan
jpsales@silvaco.com

Silvaco Korea
krsales@silvaco.com

Silvaco Taiwan
twsales@silvaco.com

Silvaco Singapore
sgsales@silvaco.com

Silvaco UK
uksales@silvaco.com

Silvaco France
frsales@silvaco.com

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