Simulation Standard

TCAD Driven CAD

A Journal for Circuit Simulation and SPICE Modeling Engineers

Investigating Two Dimensional Implantation Effects Using The BCA Model

I. Introduction

The Monte Carlo Binary Collision Algorithm (BCA) implant module in ***ATHENA*** was introduced in an earlier article [*Simulation Standard* vol 10, #5, May 1999] which discussed the accuracy of the simulation model compared to one dimensional measurements using Secondary Ion Mass Spectroscopy (SIMS). In this article we discuss the two dimensional effects that can be simulated using the BCA module that cannot accurately be simulated using analytic models.

In the BCA model the deflection of the moving particles is calculated in a strict binary way - between the moving ion and the closest atom in the lattice. The difference between the BCA model and earlier implemented Monte Carlo crystalline model is in the precise determination of the closest atom and more accurate calculation of impact dependent inelastic energy losses. The BCA model therefore excels in the prediction of well-channeled particle trajectories which results in close agreement with experiments, especially in those cases where channeling processes are dominant, such as for zero degree or 45 degree implants.

II. Device Geometry Effects

The new BCA Monte-Carlo Impant Model is a true 3D simulation which can account for all crystal directions in the crystal lattice. In Athena, the 3D simulation is then Integrated in one direction to achieve a 2D profile.

The BCA model also takes account of the vacuum above the structure, such that if an ion is transmitted through one part of the structure, it will continue to be simulated if it then impinges into the structure later on. An example of this is shown in Figure 1, where a high angle, 15keV boron implant at 45 degrees passes right through the top corner of a poly gate and is then implanted into the silicon below through a 100A gate oxide. Only a single "pencil" beam aimed at the top corner of the polysilicon was modelled in this instance to show the shaddowing effect more clearly.

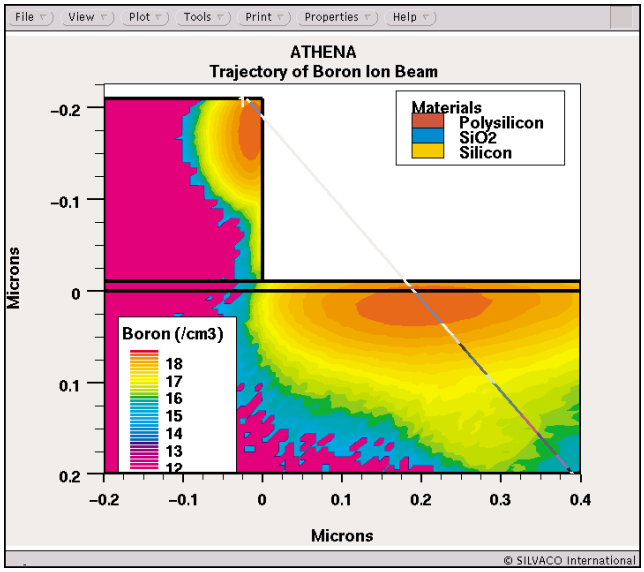

Figure 1. Showing device geometry effects. The Ion Beam passes through the top corner of the poly gate and into the silicon substrate below. In order to account for these effects, BCA also models the vacuum above the device.

Notice how the BCA model has taken account of the beam scattering from the polysilicon. The lateral spread of boron in the silicon is caused by the single point ion beam scattering after it passes through the top corner of the polysilicon. The BCA module also has knowledge of the crystalline or amorphous nature of the material being implanted in each part of the structure, including unannealed damage caused by previous implants as will be demonstrated in section III.

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INSIDE

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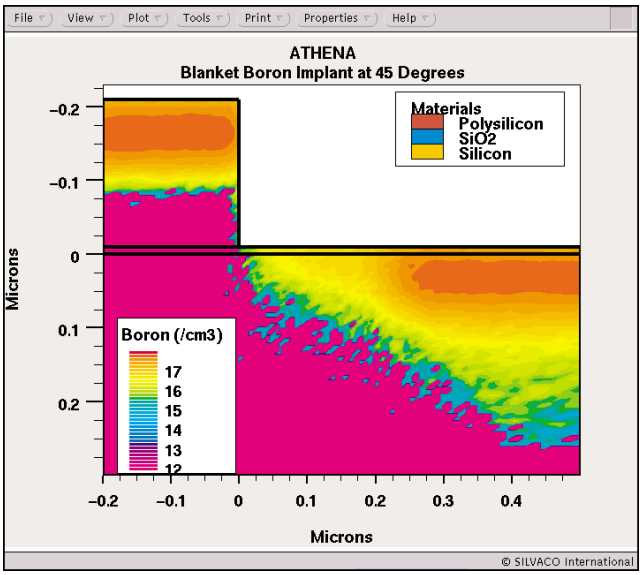


Figure 2. The same implant conditions as Figure1 but a blanket implant instead of a pencil beam. Channelling and shaddowing effects are clearly demonstrated. Note the difference in implant depth between the polysilicon and the crystalline substrate.

The Shaddowing effects demonstrated in Figure 1 can play a significant role in the final doping profile of high angle implants which are commonly used in MOSFET processing. The BCA module should be used for the highest accuracy in these cases, especially when the high angle implant is crucial to the correct modelling of the electrically active region of the device.

In Figure 2 a more realistic case of the same high angle implant is demonstrated. Here the whole structure is implanted at 45 degrees and zero degree rotation. Two effects are now seen in this example. The first effect is that the shaddowing of the polysilicon gate can be seen clearly with an obvious angle in the concentration profile at the edge of the gate.

The second effect is channelling at 45 degrees as this is an exact channelling angle for <100> crystalline silicon. The implant in this case penetrates much deeper in the areas where it is not scattered by the polysilicon as was the case in Figure 1. Notice how the depth of the implant in the polysilicon gate is significantly less than the depth of the implant into the silicon. This is due to the non-aligned grain structure of the polysilicon that prevents channelling from occurring.

Figure 3 shows the same implant but this time at zero degrees which is another channelling direction for <100> silicon. Once again, notice the difference in the implant depths between the scattered implant in the polysilicon and the channelling that occurs in the crystalline substrate.

It is important to control the beamwidth for simulations where significant channelling occurs. It should be stressed here that experimental results for well channeled implants are quite sensitive to many factors including surface conditions (thickness and uniformity of oxide surface layer) and precision of the ion beam orientation and beamwidth. Even 0.5 degree deviation in these parameters could result in considerable changes of measured implanted profiles. For this simulation, the beamwidth parameter has been set to 0.1 degrees.

Analytic implant models fall short of Monte Carlo implant models in these cases for two reasons. The first shortfall of analytic models is that they do not account for channeling other than in the normal direction. Channeling profiles have been well modelled for normally incident ions in [100] and [110] directions. However, analytic models cannot account for large angles from the normal which would have increased channeling effects in other crystal directions. Hence, for a <100> silicon substrate case where for a large angle implant, no channeling in the [110] direction (or any other crystal direction) would be calculated.

A second shortfall of analytic models is the lateral straggle which is not well defined. This is particularly important for LDD and source / drain implants, because of the lateral straggle of the implant underneath the poly gate. This effect is not significant at large gate lengths, but as gate lengths reduce to a quarter micron and below, MOSFET threshold voltages could be inaccurate if the BCA model is not used.

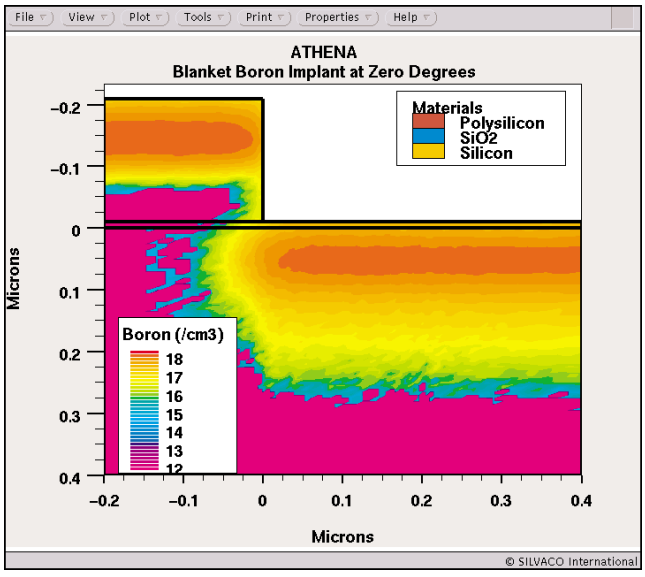
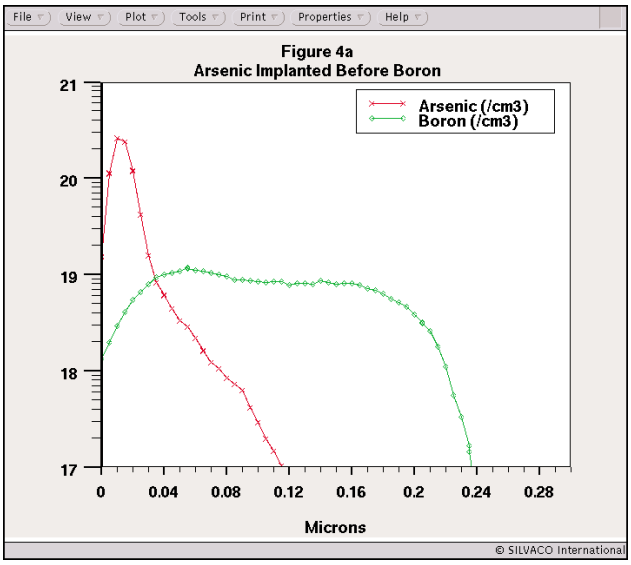


Figure 3. A zero degree tilt implant into the same structure for comparison.



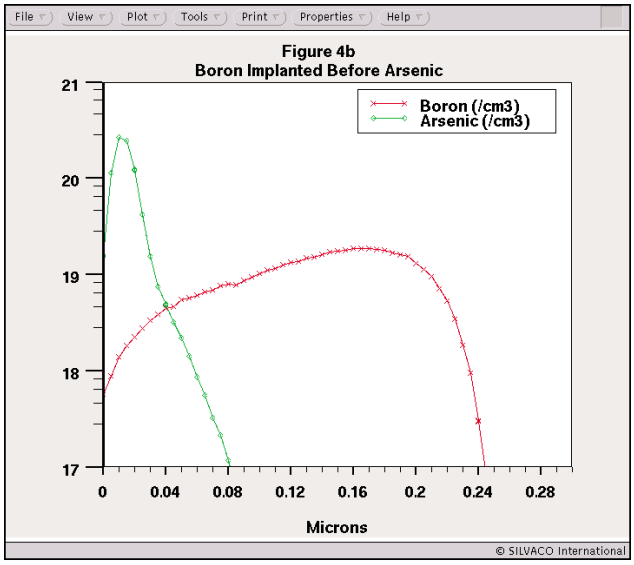


Figure 4. Comparison between two identical process flows, but where the order of two identical implants is switched. In the first profile (Figure 4a), the arsenic is implanted first, the surface is amorphised and little channelling occurs in the following boron implant. When the implant order is switched, significant channelling of boron occurs (Figure 4b).

III. Implantation Damage Effects

In silicon processing, the implant depth profile of a species can depend on previous processing steps. In this example, two implants are implanted at zero degrees tilt to emphasize the effect. In the first instance, 10keV Arsenic is implanted into undamaged silicon, followed by 10keV boron. Both implants also have the same dose. In the second instance, the implant conditions are identical, but the order of the implants is switched, such that the boron implant is carried out first.

The two implant species, boron and arsenic, are very different in mass and therefore cause different amounts of damage for a given dose and energy. Arsenic is heavy compared to boron which therefore creates significantly more damage and will amorphise the surface for typical MOSFET source / drain implant doses.

If the boron is implanted after the arsenic, the boron is now effectively being implanted into an amorphous substrate such that little channelling occurs even at zero degrees tilt. The peak concentration of boron will thus now occur closer to the surface of the substrate. Figure 4 shows the results of these two experiments.

This is a clear demonstration of the accurate damage model in the BCA module. Clearly the boron implant does not damage the silicon to the same extent as the the arsenic implant, since the arsenic profile is little affected by the previous boron implant.

In order to produce a similar effect using analytic models, one would need prior knowledge of the damaging effect of previous implants. Thus, in this case, an amorphous model would be used for the boron implant if it was after the arsenic implant but a crystalline model would be used if it was the first implant. However, one would have to choose between these two extremes since there is no analytical model for partially damaged silicon. In this case, it can be seen that the analytical approach would be inaccurate, since in Figure 4a it is clear that the boron is not completely de-channelled. The BCA model on the other hand continuously takes into account the gradual build up of damage as it occurs during the implant.

Any bipolar or CMOS fabrication process that incorporates a high atomic mass ion implant followed by a lower atomic mass ion implant without a thermal anneal in between will suffer from the effects demonstrated above. This problem is enhanced for very low energy implants used on today's aggressive deep sub-micron technologies. We strongly recommend the BCA module for accurate process simulation in these cases.

IV. Conclusion

Two dimensional ion implantation effects can be simulated accurately using the Monte Carlo Binary Collision Algorithm (BCA). The BCA model takes account of the vacuum above the device in order to model ions that fully penetrate one part of the device, travel through the vacuum region and impinge into another region. Un-annealed crystal damge due to previous implants is also correctly modelled. These effects are becoming increasingly relevant in the sub-quarter micron fabrication process where low energy implants are used routenely.

ATLAS Field Dependent Mobility: Model Parameters for (0001) 6H-SiC and (0001) 4H-SiC

Introduction

For high temperature, high power applications Silicon Carbide (SiC) continues to be a useful material for device fabrication because of its wide band gap, high breakdown field, and high thermal conductivity [1]. Some common power devices utilizing SiC include the following: Schottky and p-n junction diodes, thyristors, and UMOSFETs. Recent research has further contributed to the characterization of the electrical transport properties of 6H-SiC and 4H-SiC [2].

Model parameters reported in [2] are used in the standard field-dependent mobility model in ***ATLAS***, and the velocity-field characteristics for 6H-SiC and 4H-SiC are simulated for several temperatures. A UMOSFET device simulation example is created with ***ATLAS***, and the reported model parameters for 4H-SiC at 23 °C are used to simulate the drain characteristics for several gate voltages.

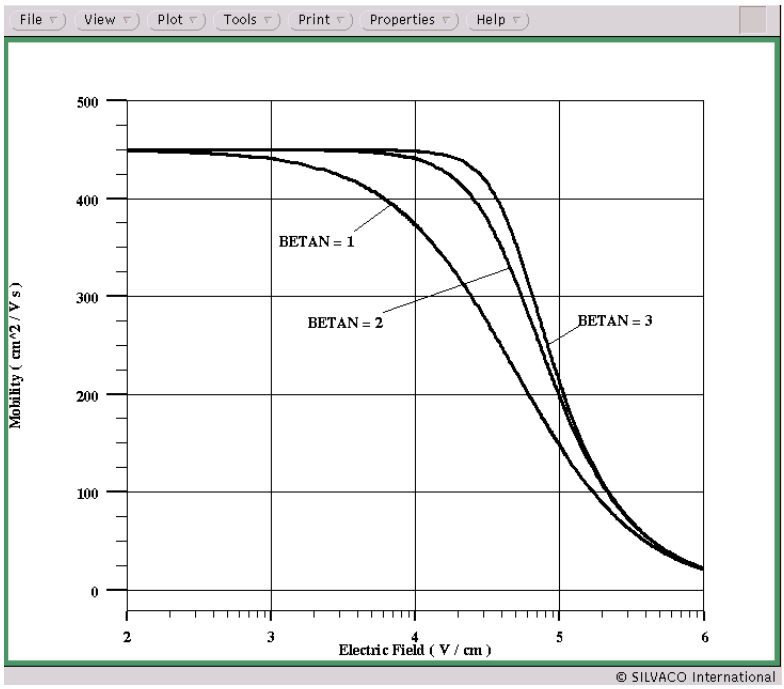


Figure 1: Mobility Versus Electric Field Generated Using Equation (1) for Several Values of BETAN (μ_{n0}=450 cm²/Vs, VSATN=2.2x10⁷ cm/s)

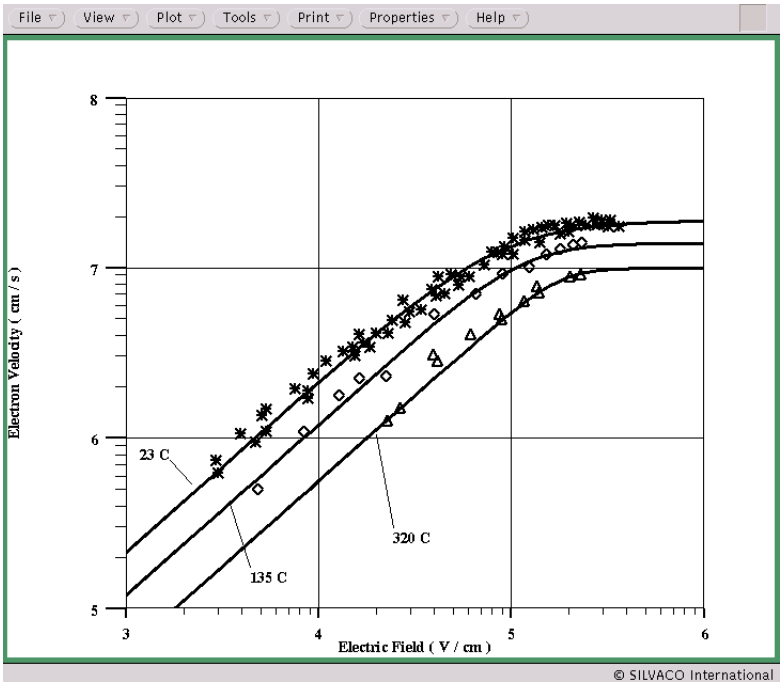


Figure 2: Velocity-Field Characteristics for (0001) 6H-SiC for 23 °C, 135 °C, and 320 °C, Simulated (solid lines), Experimental (symbols).

Model Description

As the electric field in a semiconductor is increased, the carriers gain energy and accelerate in the electric field until no further energy can be imparted to the carriers. Ultimately, near high electric fields the carrier velocity reaches an upper limit at which it can travel no faster, the carrier saturation velocity. Carrier saturation velocity effects are incorporated in the standard field-dependent mobility model for electrons in ***ATLAS***. This model is described by an analytical expression given by [3]

$$\mu_n = \frac{\mu_{n0}}{\left[1+\left[\frac{\mu_{n0}E}{VSATN}\right]^{BETAN}\right]^{\frac{1}{BETAN}}} \quad (1)$$

where μ_{n0} is the low field electron mobility, E is the electric field parallel to the current flow, VSATN is the electron saturation velocity, and BETAN is a unitless experimentally determined parameter.

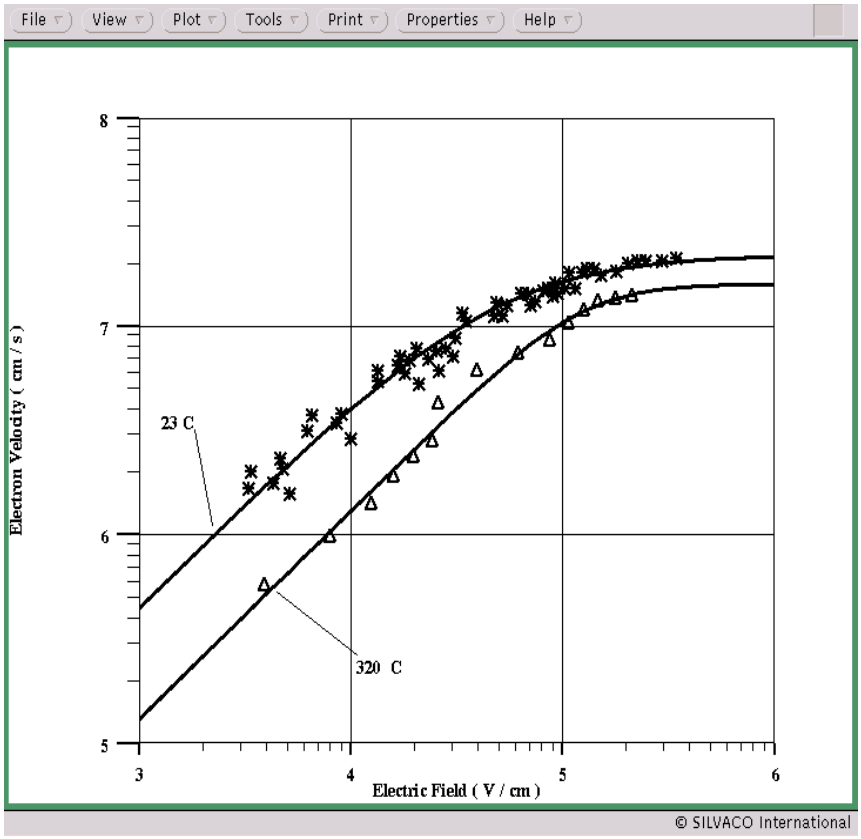


Figure 3: Velocity-Field Characteristics for (0001) 4H-SiC for Room Temperature and 320 °C, Simulated (solid lines), Experimental (symbols)

This model is activated in ***ATLAS*** using the FLDMOB parameter on the MODEL statement. A plot of equation (1) for several values of BETAN is shown in Figure 1 where μn0=450 cm^2/Vs and VSATN=2.2x10^7 cm/s have been used. As expected the electron mobility monotonically decreases as a function of increasing electric field, and the magnitude of the slope of the mobility increases with increasing BETAN.

Simulation Results

Electron drift velocity as a function of electric field has recently been measured for conduction in the (0001) plane of 6H-SiC and 4H-SiC [2]. From the velocity-field measurements equivalent parameters for μ_{n0},VSATN, and BETAN were determined at room temperature and elevated temperatures.

The extracted model parameters from [2] are specified in the FLDMOB model in ***ATLAS***, and are summarized in Table 1 and Table 2 for 6H-SiC and 4H-SiC, respectively. A uniformly doped substrate (N_d=1x10^{17} cm^{-3}) is created in ***ATLAS*** and the voltage across the sample is ramped such that the electric field varies between 10^3 and 10^6 V/cm. Using the PROBE statement the electron mobility and electric field are saved as a function of bias voltage in an ***ATLAS*** log file. The statements used for this operation are shown below

```
LOG OUTF=VEL_FIELD.LOG

PROBE X=0.5 Y=0.05 DIR=90 /
FIELD NAME=E_FIELD

PROBE X=0.5 Y=0.05 DIR=90 /
N.MOB NAME=N_MOB
```

The electron velocity is calculated from the product of the electron mobility and electric field. The simulated velocity field characteristics for 6H-SiC and 4H-SiC are shown in Figure 2 and Figure 3, respectively with the experimental data [2] overlaid. As expected the simulated curves show very good agreement with the experimental results.

The next simulation results are generated using a UMOSFET device. As previously reported in [4, 5], Id-Vd characteristics for UMOSFETs can be simulated without anisotropic mobility models because the majority

	23 °C	135 °C	320 °C
μ_{n0} (cm2/Vs)	215	120	56
VSATN (cm /s)	1.9x10^7	1.4x10^7	1x10^7
BETAN (unitless)	1.7	2.5	4

Table 1. Model Parameters [2] Used in Velocity-Field Simulations for 6H-SiC

	23 °C	320 °C
μ_{n0} (cm2/Vs)	450	130
VSATN (cm /s)	2.2x10^7	1.6x10^7
BETAN (unitless)	1.2	2.2

Table 2. Model Parameters [2] Used in Velocity-Field Simulations for 4H-SiC

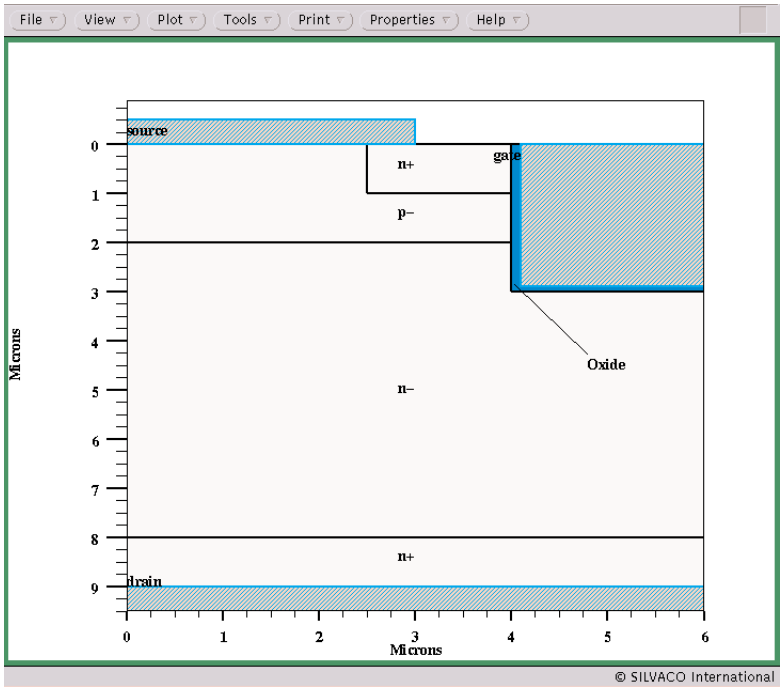


Figure 4: 4H-SiC UMOSFET Structure Generated with ATLAS (n^+=5x10^{19} cm^{-3}, n^-=2x10^{15} cm^{-3}, p^-=2x10^{17} cm^{-3})

References

[1] Jayarama N. Shenoy et al, "High-Voltage Double-Implanted Power MOSFETs in 6H-SiC," IEEE Trans. Electron Devices, Vol. 18, No. 3, pp. 93-95, March 1997.

[2] Imran A. Khan and James A. Cooper, "Measurement of High-Field Electron Transport in Silicon Carbide," IEEE Trans. Electron Devices, Vol. 47, No. 2, pp. 269-273, February 2000.

[3] ATLAS User's Manual.

[4] "ATLAS Simulation of SiC Devices Using Anisotropic Mobility Models," Simulation Standard, Vol. 8, No. 11, November 1997.

[5] Lades M. and Wachutka G., " Extended Anisotropic Mobility Model Applied to 4H/6H-SiC Devices", Proc. IEEE SISPAD, pp.169-171, 1997.

[6] Charles E. Weitzel et al., "Silicon Carbide High-Power Devices," IEEE Trans. Electron Devices, Vol. 43, No. 10, pp. 1732-1741, October 1996.

[7] B. Jayant Baliga, "Trends in Power Semiconductor Devices," IEEE Trans. Electron Devices, Vol. 43, No. 10, October 1996.

of the current flows in the (0001) plane. A UMOSFET device similar to the one described in [6, 7] is created using ***ATLAS***. The resulting structure is shown in Figure 4, where the doping levels in the structure and electrode locations have been indicated. Using the field-dependent mobility parameters for 4H-SiC at 23 °C, the drain characteristics are generated with ***ATLAS*** and are shown in Figure 5.

Conclusion

The standard field-dependent mobility model (FLDMOB) has been reviewed with emphasis on its application to 6H-SiC and 4H-SiC materials. Model coefficients extracted from recent experimental results have been used in the mobility model, and the velocity-field characteristics for 6H-SiC and 4H-SiC were generated using the PROBE feature in ATLAS. The extracted mobility coefficients were used to simulate the drain characteristics of a 4H-SiC UMOSFET at room temperature. Using the updated coefficients obtained from [2] in ATLAS will allow more accurate simulation results for devices based on 6H-SiC and 4H-SiC materials.

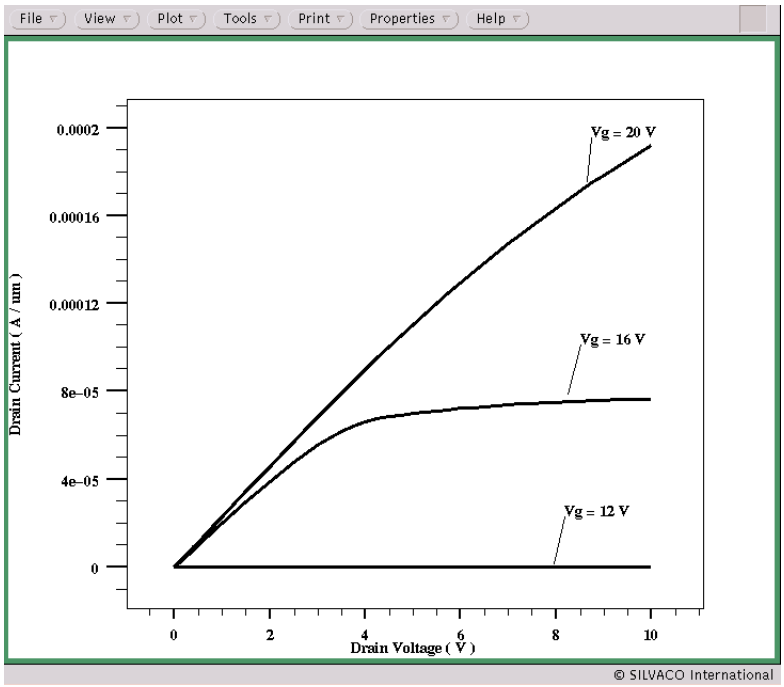


Figure 5: Drain Characteristics for UMOSFET Structure for V_g=12V, V_g=16V, and V_g=20V (μ_{n0}=450 cm^2/Vs, VSATN=2.2x10^7 cm/s, BETAN=1.2)

Reverse Engineering An AlGaAs/InGaAs PHEMT With *FastBlaze*

Introduction

FastBlaze is an ultra-fast physical MESFET and HEMT simulator which incorporates advanced physical models. By designing the simulator and its framework specifically for these devices, Silvaco has optimized device simulation algorithms and data structures for high speed without sacrificing the accuracy of the physical models. The application of ***FastBlaze*** to the simulation of a specific PHEMT is presented here. We highlight details of how the device was constructed and how the simulation was tuned to match the reported device characteristics.

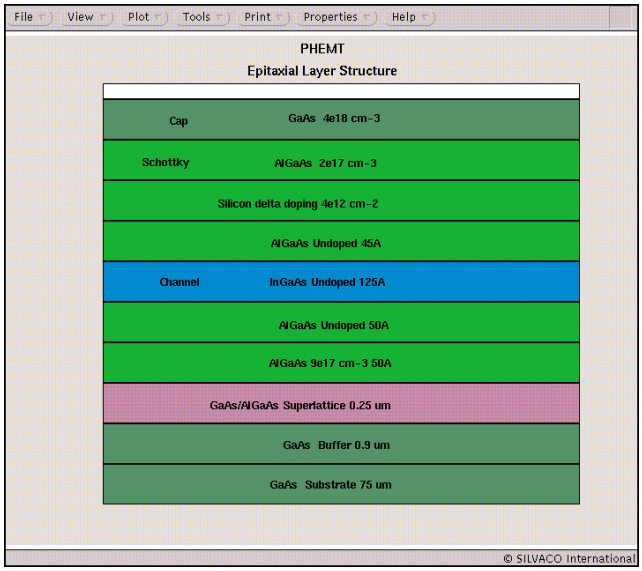


Figure 1. Layer structure of PHEMT[1] used in the ***FastBlaze*** simulation.

Device Description

This simulation was based on a double recessed pseudomorphic GaAs High Electron Mobility Transistor (PHEMT) for high voltage operation. The construction and operation of this device was described by Kao et al., of GE, in the 1992 IEEE IEDM Technical Digest [1]. They reported that a PHEMT with 0.25 um gate length exhibited a gate to drain breakdown voltage of 30 volts, a peak gm of 510 mS/mm, and a maximum current density of 540 mA/mm. The device also had excellent 4.5 and 10 GHz power performance.

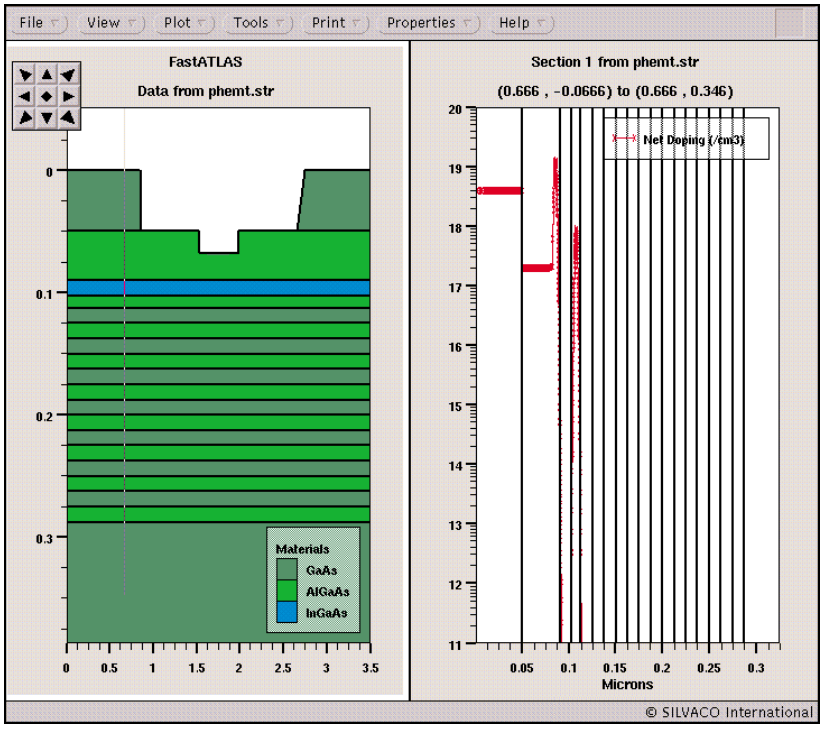


Figure 2. Two-dimensional structure of the initial PHEMT design and its net doping vertically through the source.

Construction Details

In the brief details about the device, the authors provided a lot of detail about the epitaxial layer structure, see Figure 1, but no information about the depths of the recesses, the recess lengths, gate-to-recess edge lengths, the Schottky barrier height and the gate-to-channel spacing. Also not mentioned are process related parameters like surface trap density and mobility in the channel, which require specialized measurement techniques and equipment. With reasonable choices of these parameters we have a starting point for tuning the simulation. A plot of the PHEMT structure is shown in Figure 2.

Tuning Procedures

The parameters are tuned for three results: Vt, Idss, and breakdown voltage, in that order.

(1) The threshold voltage is primarily a function of the charge under the gate and the Schottky built-in bias. Vt is not a strong function of surface state density. The parameters we need to tune are the gate-to-channel spacing, the top delta doping, and the Schottky bias.

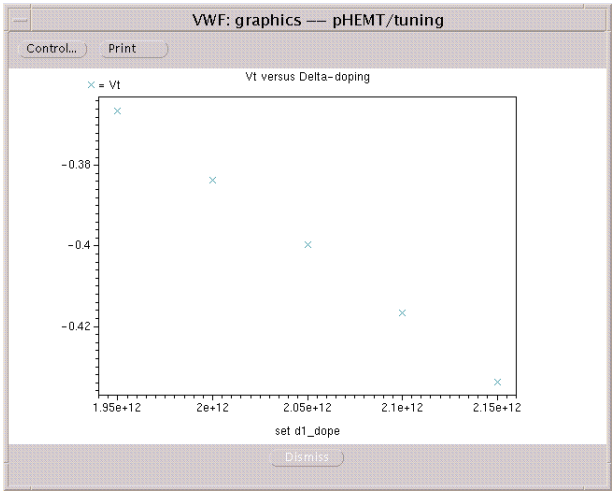


Figure 3. ***FastBlaze*** results showing the effect of delta layer doping on the threshold voltage.

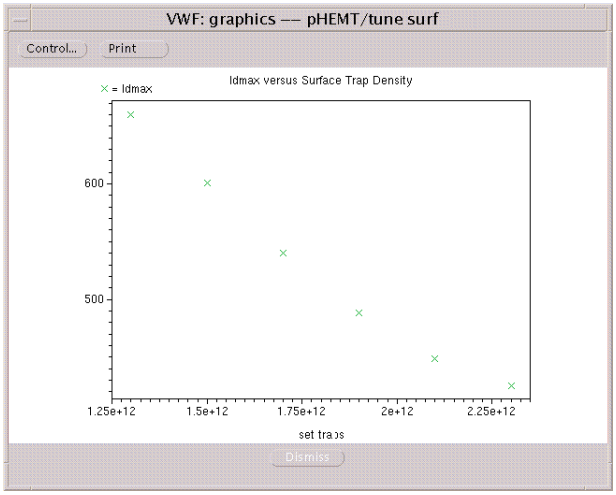


Figure 4. ***FastBlaze*** results showing effect of the surface trap density on the simulated maximum drain current.

(2) Idss is affected by the charge underneath the gate, the transport characteristics, and the access resistance to and from the gate. This access resistance is primarily a function of the charge under the cap region (also low-field mobility) hence this parameter is affected by the surface trap density, which captures carriers on the surface and decreases the total amount of free charge. Measurements show the surface pinning potential due to surface states to be around 0.5 - 0.7 eV and hence when designing your input deck you should always check this value at the gate recess depth. A note on mobility: ***FastBlaze*** uses the local impurity density to calculate the mobility. In PHEMT devices this omits any surface and non-local scattering mechanisms present in the device. To obtain better correlation with experimental results the user should scale down actual channel mobility to about 85% of the ideal InGaAs mobility. The parameters we need to tune for Idss are therefore surface trap density and mobility scaling.

(3) Finally the breakdown voltage is controlled principally by the peak lateral field generated in the device. (Impact ionization is an exponential function of field) The way to increase breakdown is to decrease the peak lateral field. This is done by using a double recess gate technology which spreads out the field generated at the drain edge of the gate over the 2nd recess gate-drain region reducing the overall peak field value. With uniformly doped caps the 2nd recess depth should be optimum between 65-85% of the total recess depth. Note that the 2nd recess has an adverse effect on Idss since we are producing a region of higher resistance and consequently the peak gm will also be

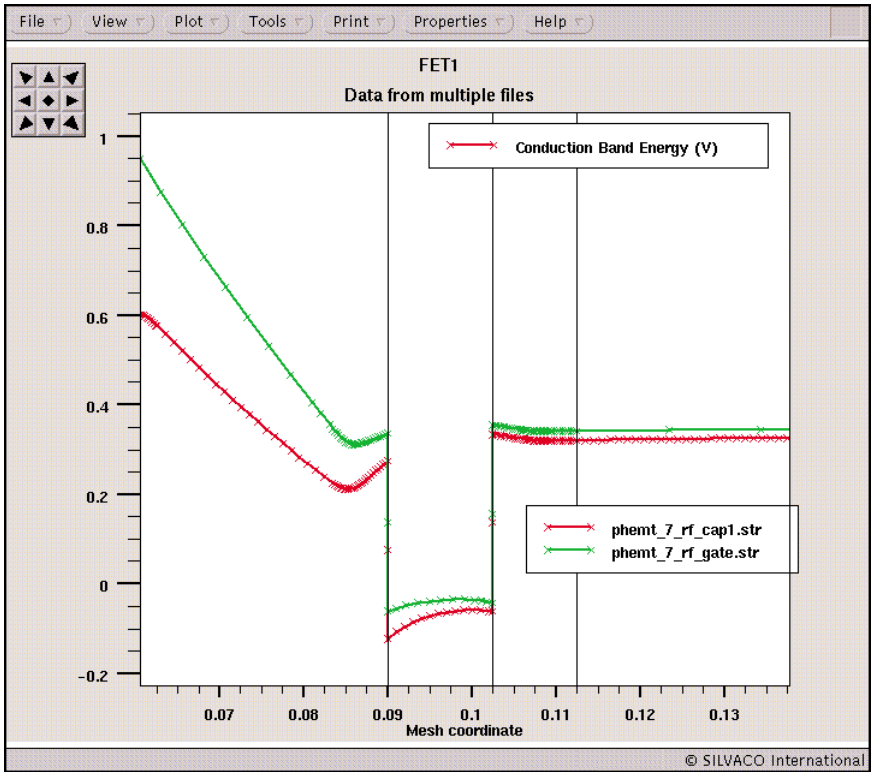


Figure 5. Conduction band profile under the recess of the PHEMT showing surface potential pinning.

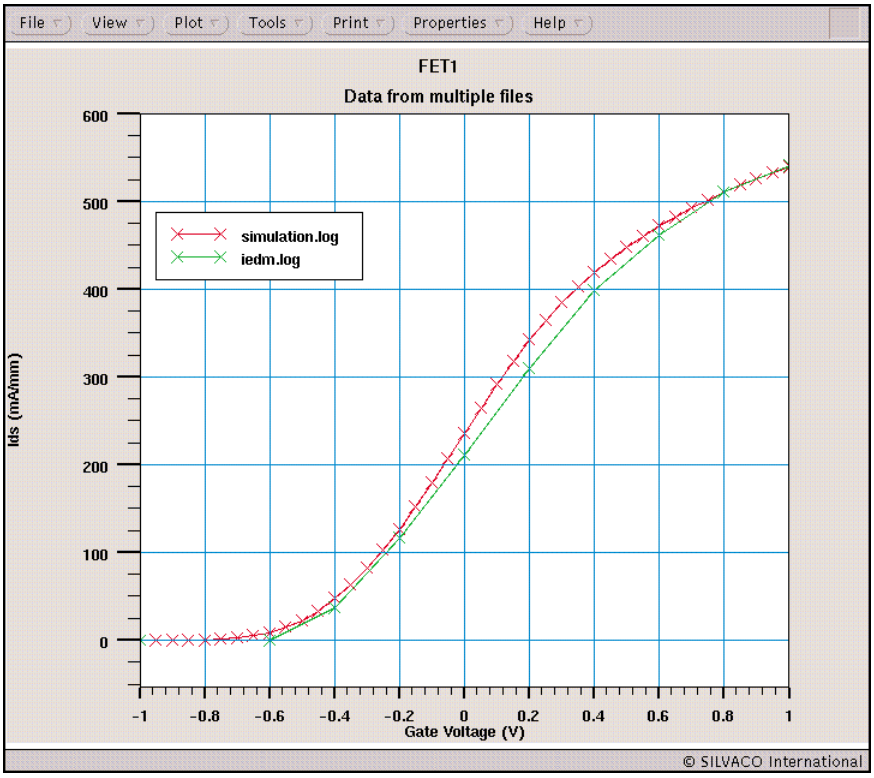


Figure 6. Comparison between the ***FastBlaze*** simulated drain current and measured data [1] as the gate voltage is swept from -IV to IV.

in Figure 6. After tuning, the breakdown voltage was 30.1 volts at the second recess depth of 0.044 um. The tuning curve for breakdown voltage versus second recess depth is shown in Figure 7.

Conclusions

By following a straightforward procedure for tuning a HEMT simulation, good agreement with experiment can be easily found. ***FastBlaze*** is not only an excellent tool for designing HEMTs and MESFETs, it is fast enough to be used quickly within VWF to reverse engineer HEMT designs.

References

[1] M-Y Kao, S-T Fu, P Ho, P. M. Smith, P. C. Chao, K. J. Nordheden, and S. Wang, "Very High Voltage AlGaAs/InGaAs Pseudomorphic Power HEMTs",, 1992 IEEE IEDM Technical Digest, p.319 - 321, 1992.

reduced. You therefore have to balance any increase of breakdown voltage with a reduction in gm. The parameter we need to tune for breakdown voltage is the second recess depth.

(4) Iterate the above until agreement is obtained. ***FastBlaze*** can be used within the ***Virtual Wafer Fab Automation Tools*** to facilitate the design of the tuning simulations.

Simulation Results

Tuning the delta doping for threshold voltage gave the results shown in Figure 3. The delta dose was chosen to make Vt = -0.4. Tuning the surface trap density for Idmax gave the results shown in Figure 4. The surface trap density was therefore chosen to be 1.7e12, which implies Idmax = 540 mA/mm. The surface potential was extracted from a charge-control analysis under the gate and under the cap layer at the total recess depth. Figure 5 shows conduction band voltage versus depth. In this case the potential at the surface of the recess is 0.6 volts. The result of tuning the simulation for Vt and Ids with this procedure is shown in the close agreement with the experimental data

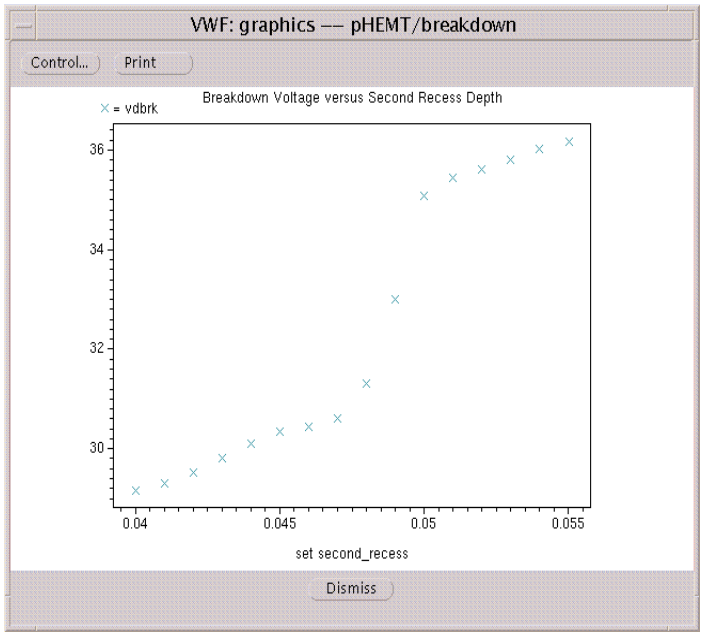


Figure 7. ***FastBlaze*** results showing the simulated variation of breakdown voltage with depth of the second recess.

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Bulletin Board

ICMTS in Monterey

Attendees and exhibitors will spend March 13-16 in Monterey, CA for the International Conference on Microelectronic Test Structures. Our time there will be devoted to answering questions and showcasing our tools. The conference will be beneficial in matching the needs of attendees with our innovative line of EDA tools.

European Expansion

Silvaco International achieved yet another milestone with the purchase of an exclusive building site in Grenoble, France. This new property will house a major research, development, and support center for the European sub-continent. The new technology center in France will be staffed with over 100 engineers in approximately 2,400 square meters of office space. The latest Silvaco building will be completed by the close of 2000.

Ready to Rumble

Remodeling is almost complete on two new structures at our Santa Clara, CA headquarters. Upon completion, they will provide greater office space and flexibility. Building 26 will be the new home base for our Applications Engineers and Building 25 will house ECAD Integration. This expansion is symbolic of our growth as the technology leader in the EDA industry.

If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

William French, Applications and Support Manager

Q. How can I ensure that the vertical Y.MESH spacing in my process simulation is adequate for my particular implant condition ?

A. A good technique to check that the mesh is not causing a problem is to perform an integration of the as-implanted species, directly after the implant within ***ATHENA***. There are two ways the user may do this either by using an EXTRACT command or through ***TonyPlot***.

To illustrate, if I perform the following implantation:

```
implant arsenic dose=1.0e13 energy=50
```

the EXTRACT command to integrate the dose is

```
extract name="Simulated dose" area from
curve(depth, impurity="Arsenic" material=
"Silicon" mat.occno=1 x.val=0.1)*1e-4
```

The scaling factor of 1e-4 exists to convert from um on the depth scale to cm. Depending upon the mesh density different values of "Simulated dose" will be obtained. These values can vary up to 50% of the desired dose for a poor mesh, clearly a problem. By improving the quality of the mesh, in this case by reducing the Y.MESH spacing at the silicon surface, the error may be reduced to less than 1% which is quite good enough. In this case for a surface Y.MESH spacing of 0.001 um the output is

```
EXTRACT> extract name="Simulated dose" area
from curve(depth, impurity="Arsenic" materi-
al="Silicon" mat.occno=1 x.val=0.1)*1e-4
Simulated dose=9.97292e+12   X.val=0.1
```

The same analysis may be performed inside ***TonyPlot*** by using the integration tool underneath the "Tools" menu. Figure 1 shows an Arsenic profile and the resultant integrated dose of 9.93e12 cm-2 which is less than 1% error.

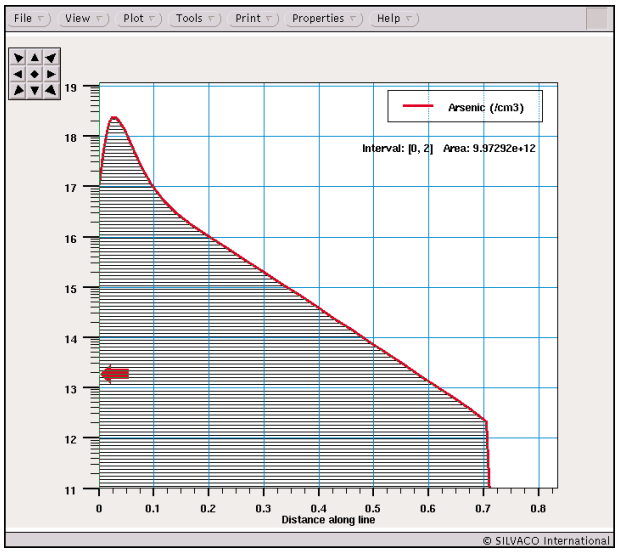

Figure 1

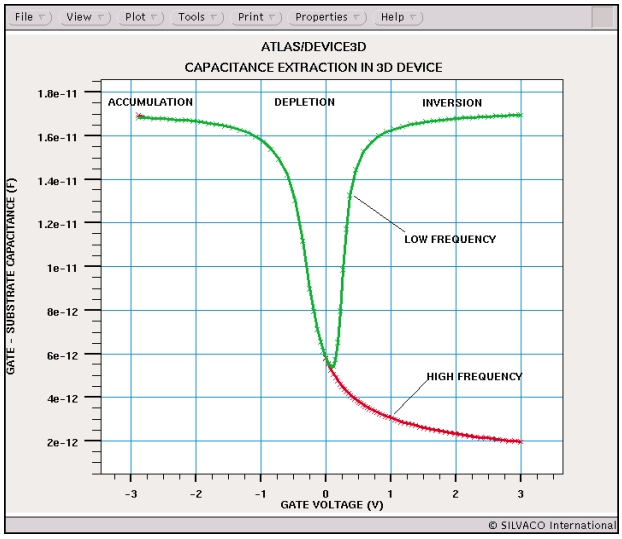

Figure 2.

Q. Is there a method that can extract the capacitance from a three-dimensional device ?

A. A simple method to extract the capacitance in 3D is to perform a very simple transient analysis. Simple theory gives us that the theoretical capacitance is

$$C = I \times dt / dV$$

To illustrate this I have chosen a simple MOS capacitor of 1um x 1um in area with a oxide thickness of 200A. Using ***Device3D*** an initial solution is obtain at a gate voltage of -3V before a transient ramp is applied to the gate contact with a final gate voltage of 3V. Thus the capacitance is

$$C = I(gate) \times ramptime(sec) / 6$$

where the ramptime is given on the transient analysis statement

```
solve  vgate=3 ramptime=6e-4 tstop=6e-4 dt=1e-5
```

The ramptime for the gate voltage can be chosen to reproduce either the low frequency or high frequency CV curves for the MOS capacitor. Figure 2 illustrates this with a ramptime of 600s for the low frequency CV curve and 6us for the high frequency curve.

Call for Questions

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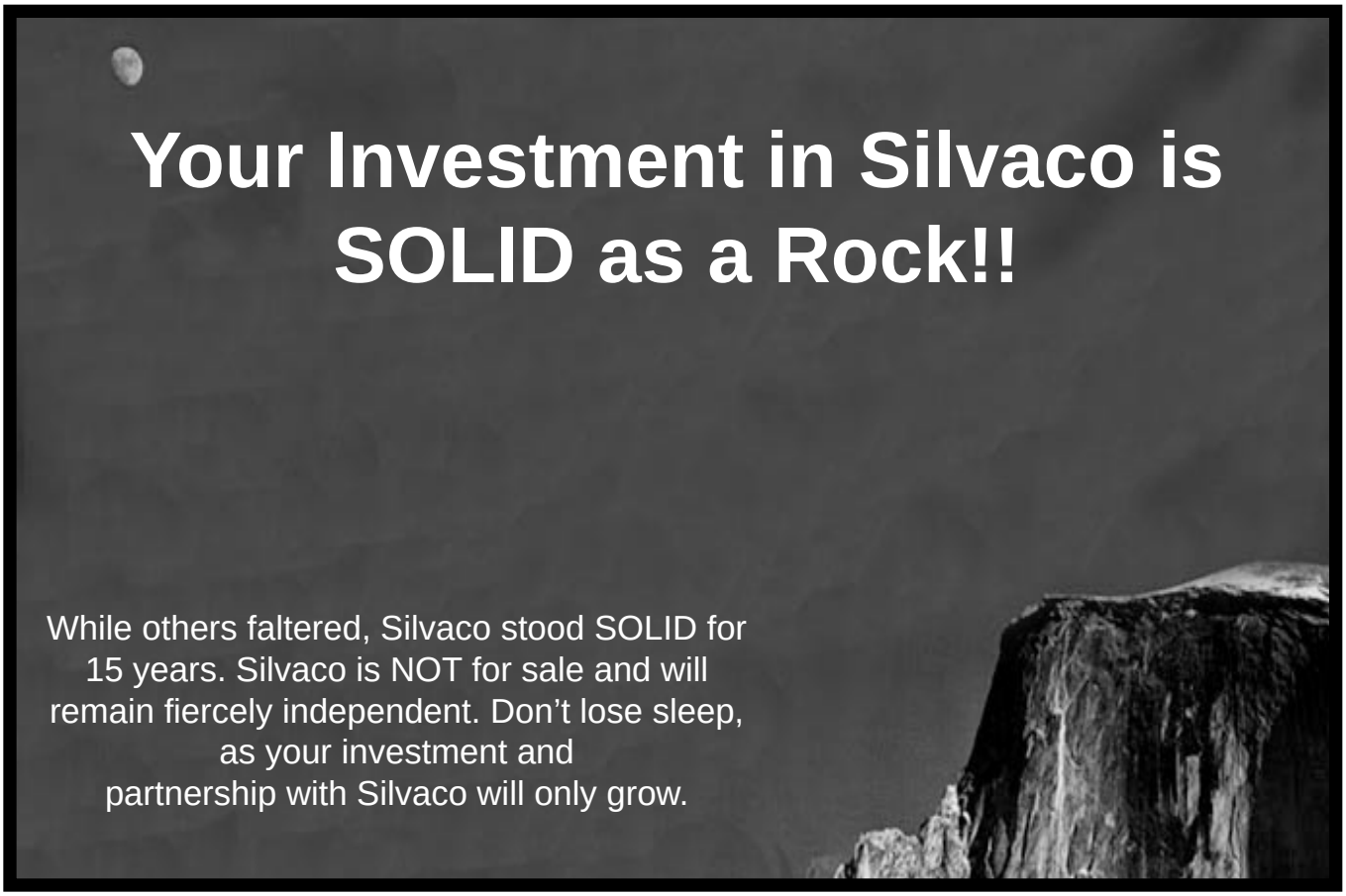

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