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BSIM3SOI Version 2.1 (FD, DD and PD) Models Released in SmartSpice

Introduction

The Berkeley BSIM3SOI version 2.1 models, released in September 1999, have been implemented in ***SmartSpice***. The three new models are selected according to LEVEL selector.

- LEVEL = 26 selects the BSIM3SOI2FD (Fully depleted) model
- LEVEL = 27 selects the BSIM3SOI2DD (Dynamic depletion) model
- LEVEL = 29 selects the BSIM3SOI2PD (Partially depleted) model

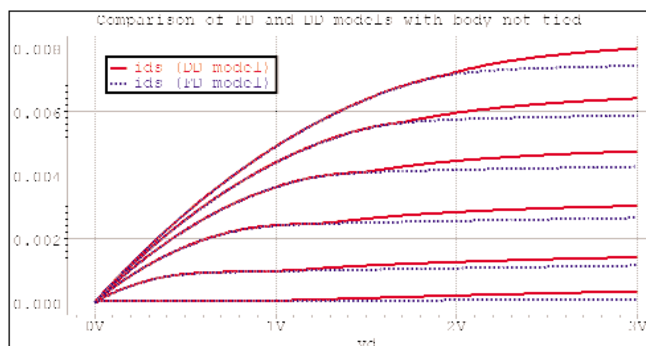

Figure 1 : Example of Id-Vds curves with FD and DD models (default model card from Berkeley)

The ***SmartSpice*** implementation of the three models is close but not identical to the UC Berkeley releases. The ***SmartSpice*** implementation provides a number of improvements and additional parameters currently unsupported in Berkeley's BSIM3SOIv2 models.

In the ***SmartSpice*** implementation of the BSIM3SOIv2 models, enhanced convergence is obtained by properly handling the GMIN and DCGMIN control options during transient and DC analysis.

The GMIN option connects a conductance in parallel with the bulk diodes. This conductance is very useful when the diode model has a very high off-resistance. The conductance DCGMIN is connected between drain and source.

The present section provides all the information needed to understand and use the three models.

BSIM3SOI FD (Fully Depleted) version 2.1 (Model LEVEL = 26)

Major Features

BSIM3SOI FD v2.1 is a suite of BSIM3SOI FD v2.0 released in February 1999. The version 2.0 is a derivative of BSIM3SOI v1.3 (level=25 in ***SmartSpice***). BSIM3SOIFDv2.0 has improved simulation efficiency and noise modeling. The basic IV for this model is modified from BSIM3v3.1 equation set. The major features are summarized as follows [1]:

- Supports external body bias and backgate bias : a total of 5 external nodes;
- Self-heating implementation improved over the alpha version of Berkeley (LEVEL 23 in ***SmartSpice***);
- New depletion charge model (EBCI) introduced for better accuracy in capacitive coupling prediction. An improved BSIM3v3 based model is added as well;
- Single I-V expression as in BSIM3v3.1 to guarantee continuities of Ids, Gm, and Gds and their derivatives for all bias conditions.

New version BSIM3SOI FDv2.1 includes the binning feature to enhance the model flexibility and fixes some bugs found in the previous version 2.0.

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Parameter	Description	Units	Default
SHMOD	Flag for self-heating 0 - no self-heating 1 - self-heating	-	0
TSI	Silicon film thickness	m	1e-7
TBOX	Buried oxide thickness	m	3e-7
VBSA	Transition body voltage offset	V	0
DELP	Constant for limiting Vbseff to Phis	V	0.02
KB1	Coefficient of Vbs0 dependency on Ves	-	1
KB3	Coefficient of Vbs0 dependency on Vgs at subthreshold region	-	1
DVBD0	First coefficient of Vbs0 dependency on Leff	V	0
DVBD1	Second coefficient of Vbs0 dependency on Leff	V	0
MXC	Fitting parameter for Abeff calculation	-	-0.9
ADICE0	DICE bulk charge factor	-	1
ISDIF	Body to source/drain injection saturation current	A/m^2	0.0
ISREC	Recombination in depletion saturation current	A/m^2	1e-5
RBODY	Intrinsic body contact sheet resistance	Ω	0
RBSH	Extrinsic body contact sheet resistance	Ω/m^2	0
CGE0	Gate substrate overlap capacitance per unit channel length	F/m	0.0
VSDFB	Source/drain bottom diffusion capacitance flatband voltage	V	calculated
VSDTH	Source/drain bottom diffusion capacitance threshold voltage	V	calculated
CSDMIN	Source/drain bottom diffusion minimum capacitance	F	calculated
ASD	Source/drain bottom diffusion minimum parameter	-	0.3
CSDESW	Source/drain sidewall fringing capacitance per unit length	F/m	0
CTH0	Normalized thermal capacity	m.°C / (W*s)	0
RTH0	Normalized thermal resistance	m.°C/W	0

Table 1. The additional parameters to BSIM3v3 that correspond to the BSIM3SOI FD Version 2.1 model.

Model Parameters

The additional parameters to BSIM3v3 listed in Table 1 correspond to the BSIM3SOI FD Version 2.1 model.

SilvacoImprovements

Options

The options VZERO and EXPERT are supported in the ***SmartSpice*** BSIM3SOI FD v2.1 model.

The option VZERO=2 allows faster runtime when large circuits are used.

The EXPERT option can be specified to detect possible problems in models, before and during simulation, such as:

- negative conductances GM, GDS and GMBS,
- negative gate capacitances.

New Model Parameters

New model parameters are listed in the following table :

Parameter	Description	Units	Default
VERSION	Version selector	-	2.1
LMIN	Limit for binning	m	0.0
LMAX	Limit for binning	m	1.0
WMIN	Limit for binning	m	0.0
WMAX	Limit for binning	m	1.0

The VERSION model parameter is used to switch between the current versions 2.0 and 2.1. The four others new model parameters are used for binning to select a model. For the binning, Silvaco has also added new binned model parameters that are displayed in Table 2.

BSIM3SOI DD (Dynamic Depletion) version 2.1 Model (LEVEL=27)

Major Features

BSIM3SOI DD v2.1 is a suite of BSIM3SOI DD v2.0 released in February 1999. The version 2.0 is a derivative of BSIM3SOI v1.3 (level=25 in Smartspice). BSIM3SOI DD v2.0 has improved simulation efficiency and noise modeling. The BSIM3SOI DDv2.0 model can be used for both Partially Depleted (PD) and Fully Depleted (FD). The basic IV for this model is modified from BSIM3v3.1 equation set. The major features are summarized as follows [2]:

- Dynamic depletion approach is applied on both I-V and C-V. Charge and drain current are scalable with Tbox and Tsi continuously;
- Supports external body bias and backgate bias : a total of 5 external nodes;
- Real floating body simulation in both I-V and C-V. Body potential is properly bounded by diode and C-V formulation;

AT	GAMMA1	GAMMA2	VBM	VBX	XT	KT1
KT1L	KT2	UA1	UB1	UC1	UTE	RTH0
PRT	CGDL	CGSL	CKAPPA	CF	CLC	CLE
XJ	RBODY	CSDMIN	CTH0	ASD	CSDESW	

Table 2. Silvaco's new binned model parameters.

- Self-heating implementation improved over the alpha version of Berkeley (LEVEL 23 in ***SmartSpice***);
- An improved impact ionization current model;
- Various diode leakage components and parasitic bipolar current included;
- New depletion charge model (EBCI) introduced for better accuracy in capacitive coupling prediction. An improved BSIM3v3 based model is added as well;
- Dynamic depletion can suit different requirements for SOI technologies;
- Single I-V expression as in BSIM3v3.1 to guarantee continuities of Ids, Gm, and Gds and their derivatives for all bias conditions.

New version BSIM3SOI DDv2.1 includes the binning feature to enhance the model flexibility and fixes some bugs found in the previous version 2.0.

Model Parameters

The additional parameters to BSIM3v3 listed below in Table 3 correspond to the BSIM3SOI DD Version 2.1 model.

Parameter	Description	Units	Default
SHMOD	Flag for self-heating 0 - no self-heating 1 - self-heating	-	0
TSI	Silicon film thickness	m	1e-7
TBOX	Buried oxide thickness	m	3e-7
VBSA	Transition body voltage offset	V	0
DELP	Constant for limiting Vbseff to Phis	V	0.02
KB1	Coefficient of Vbs0 dependency on Ves	-	1
KB3	Coefficient of Vbs0 dependency on Vgs at subthreshold region	-	1
DVBD0	First coefficient of Vbs0 dependency on Leff	V	0
DVBD1	Second coefficient of Vbs0 dependency on Leff	V	0
ABP	Coefficient of Abeff dependency on Vgst	-	1
MXC	Fitting parameter for Abeff calculation	-	-0.9
ADICE0	DICE bulk charge factor	-	1
ALPHA1	The second parameter of impact ionization current	m/V	1.0
AII	First Vds dependence Ecrit parameter	-	0
BII	Second Vds dependence Ecrit parameter	m	0
CII	Vgsteff dependence Ecrit parameter	1/m	0
DII	Vbseff dependence Ecrit parameter	1/m	-1.0
AGIDL	GIDL constant	W-1	0
BGIDL	GIDL exponential coefficient	V/m	0
NGIDL	GIDL Vds enhancement coefficent	V	1.2
NTUN	reverse tunneling non-ideality factor	-	10.0
NDIODE	Diode non-ideality factor	-	1.0
ISBJT	BJT injection saturation current	A/m^2	1e-6
ISDIF	Body to source/drain injection saturation current	A/m^2	0.0
ISREC	Recombination in depletion saturation current	A/m^2	1e-5
ISTUN	Reverse tunneling saturation current	A/m2	0
EDL	Electron diffusion length	m	2e-6
KBJT1	Parasitic bipolar early effect coefficient	m/V	0
RBODY	Intrinsic body contact sheet resistance	Ω/m^2	0
RBSH	Extrinsic body contact sheet resistance	Ω/m^2	0
CGE0	Gate substrate overlap capacitance per unit channel length	F/m	0.0
TT	Diffusion capacitance transit time coefficient	s	1e-12
VSDFB	Source/drain bottom diffusion capacitance flatband voltage	V	calculated
VSDTH	Source/drain bottom diffusion capacitance threshold voltage	V	calculated
CSDMIN	Source/drain bottom diffusion minimum capacitance	F	calculated
ASD	Source/drain bottom diffusion minimum parameter	-	0.3
CSDESW	Source/drain sidewall fringing capacitance per unit length	F/m	0
CTH0	Normalized thermal capacity	m.°C / (W*sec)	0
RTH0	Normalized thermal resistance	m.°C/W	0
XBJT	Power dependence of jbjt on temperature	-	2
XDIF	Power dependence of jdif on temperature	-	2
XREC	Power dependence of jrec on temperature	-	20
XTUN	Power dependence of jtun on temperature	-	0
NOIF	Floating body excess noise ideality factor	-	1.0

Table 3. The additional parameters to BSIM3v3 correspond to the BSIM3SOI DD Version 2.1 model.

Silvaco Improvements

Options

The options VZERO and EXPERT are supported in the ***SmartSpice*** BSIM3SOI DD v2.1 model.

The option VZERO=2 allows faster runtime when large circuits are used.

The EXPERT option can be specified to detect possible problems in models, before and during simulation, such as:

- negative conductances GM, GDS and GMBS,
- negative gate capacitances.

New Model Parameters

New model parameters are listed in the following table :

Parameter	Description	Units	Default
VERSION	Version selector	-	2.1
SMART	Improvement selector	-	1
LMIN	Limit for binning	m	0.0
LMAX	Limit for binning	m	1.0
WMIN	Limit for binning	m	0.0
WMAX	Limit for binning	m	1.0

The VERSION model parameter is used to switch between the current version 2.0 and 2.1. The four new model parameters (LMIN, LMAX, WMIN and WMAX) are used for binning to select a model. For the binning, Silvaco has also added the following new binned model parameters shown in Table 4.

The SMART model parameter Silvaco improvements which are not compatible with original Berkeley model allows to switch on . SMART model parameter has been created as follows :

- if SMART = 0: the original Berkeley model is used with its different versions
- if SMART > 0: the Berkeley model is used with the following improvements:
  - problem with RBODY model parameter has been fixed;
  - some derivatives related to body tied have been corrected;
  - the limitation of vb has been modified.

BSIM3SOI PD (Partially depleted) version

AT	GAMMA1	GAMMA2	VBM	VBX	XT	KT1
KT1L	KT2	UA1	UB1	UC1	UTE	RTH0
PRT	CGDL	CGSL	CKAPPA	CF	CLC	CLE
XJ	RBODY	CSDMIN	CTH0	ASD	CSDESW	CJSWG
PBSWG	MJSWG	TT	XBJT	XDIF	XREC	XTUN

Table 4. Silvaco's new binned model parameters.

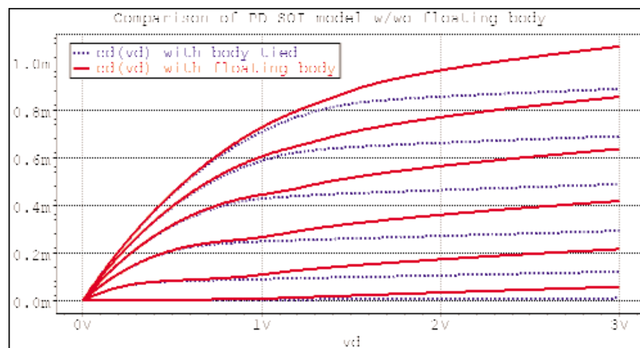

Figure 2 : Example of Id-Vds curves with PD model (default model card from Berkeley)

2.1 Model (LEVEL = 29)

Major Features

BSIM3SOI PD v2.1 is a suite of BSIM3SOI PD v2.01 released in April 1999. The version 2.01 is a derivative of BSIM3SOI v1.3 (level=25 in Smartspice). Many enhanced features are included in BSIM3SOI PD v2.0.1. BSIM3SOI PD v2.0.1 has the following new features relative to BSIM3SOIv1.3 [3]:

- Real floating body simulation in both C-V and I-V. The body potential is determined by the balance of all the body current components;
- Enhancements in the threshold voltage and bulk charge formulation of the high positive body bias regime;
- An improved parasitic bipolar current model. This includes enhancements in the various diode leakage components, second order effects (high-level injection & early effect), diffusion charge equation and temperature dependence of the diode junction capacitance;
- An improved impact ionization current model. The contribution from BJT current is also modeled by the parameter FBJTII;
- Instance parameters (PDBCP, PSBCP, AGBCP, AEBCP, NBC) are provided to model the parasitics of devices with various body-contact and isolation structures.
- An external body node (the 6th node) and other improvements are introduced to facilitate the modeling of distributed body-resistance;
- Self-heating: an external temperature node (the 7th node) is supported to facilitate the simulation of thermal coupling among neighboring devices;
- A unique SOI low frequency noise model, including a new excess noise resulting from the floating body effect;
- Width dependence of the body effect is modeled by parameters (K1, K1W1, K1W2);
- Improved history dependence of the body charges with two new parameters (FBODY, DLCB);

Parameter	Description	Units	Default
SHMOD	Flag for self-heating 0 - no self-heating 1 - self-heating	-	0
TSI	Silicon film thickness	m	1e-7
TBOX	Buried oxide thickness	m	3e-7
KIW1	First body effect with dependent parameter	m	0
KIW2	Second body effect with dependent parameter	m	0
KB1	Coefficient of Vbs0 dependency on Ves	-	1
KETAS	Surface potential adjustment for bulk charge effect	V	0
DWBC	Width offset for body contact isolation edge	m	0.0
FBJTII	Fraction of bipolar current affecting the impact ionization	m/V	0.0
BETA0	First Vds dependence parameter of impact ionization cur-rent	1/V	0
BETA1	Second Vds dependence parameter of impact ionization current	1/V	0
BETA2	Third Vds dependence parameter of impact ionization current	V	0.1
VDSATII0	Nominal drain saturation voltage at threshold for impact ionization current	V	0.9
TII	Temperature dependent parameter for impact ionization current	-	0
LII	Channel length dependent parameter at threshold for impact ionization current	-	0
ESATII	Saturation channel electric field for impact ionization cur-rent	V/m	1e7
SII0	First vgs dependent parameter for impact ionization cur-rent	1/V	0.5
SII1	Second vgs dependent parameter for impact ionization current	1/V	0.1
SII2	Third vgs dependent parameter for impact ionization cur-rent	1/V	0
SIID	vds dependent parameter of drain saturation voltage for impact ionization current	1/V	0
AGIDL	DIDL constant	Ω^{-1}	0
BGIDL	GIDL exponential coefficient	V/m	0
NGIDL	GIDL Vds enhancement coefficent	V	1.2
NTUN	reverse tunneling non-ideality factor	-	10.0
NDIODE	Diode non-ideality factor	-	1.0
NRECF0	Recombination non-ideality factor at forward bias	-	2.0
NRECR0	Recombination non-ideality factor at reversed bias	-	10.0
ISBJT	BJT injection saturation current	A/m^2	1e-6
ISDIF	Body to source/drain injection saturation current	A/m^2	0
ISREC	Recombination in depletion saturation current	A/m^2	1e-5
ISTUN	Reverse tunneling saturation current	A/m^2	0
LN	Electron/hole diffusion length	m	2e-6
VREC0	Voltage dependent parameter for recombination current	V	0
VTUN0	Voltage dependent parameter for tunneling current	V	0
NBJT	Power coefficient of channel length dependency for bipolar current	-	1
LBJT0	Reference channel length for bipolar current	m	0.2 e-6
VABJT	Early voltage for bipolar current	V	10
AELY	Channel length dependency of early voltage bipolar current	V/m	0
AHLI	High level injection parameter for bipolar current	-	0
RBODY	Intrinsic body contact sheet resistance	Ω/m^2	0
RBSH	Extrinsic body contact sheet resistance	Ω/m^2	0
TT	Diffusion capacitance transit time coefficient	s	1e-12
NDIF	Power coefficient of channel length dependency for diffusion capacitance	-	-1
LDIF0	Channel length dependency coefficient of diffusion capacitance	-	1
VSDFB	Source/drain bottom diffusion capacitance flatband voltage	V	calculated
VSDTH	Source/drain bottom diffusion capacitance threshold voltage	V	calculated
CSDMIN	Source/drain bottom diffusion minimum capacitance	-	calculated
ASD	Source/drain bottom diffusion minimum parameter	-	0.3
CSDESW	Source/drain sidewall fringing capacitance per unit length	F/m	0
DLCB	Length offset fitting parameter for body charge	m	0.0
DLBG	Length offset fitting parameter for backgate charge	m	0.0
DELVT	Threshold voltage adjust for C-V	V	0.0
FBODY	Scaling factor for body charge	-	1.0
ACDE	Exponetial coefficient for charge thickness in CAPMOD=3 for accumulation and depletion regions	m/V	1.0
MOIN	Coefficient for the gate-bias dependent surface potential	$V^{0.5}$	15.0
TCJSWG	Temperature coefficient of CJSWG	1/K	0
TPBSWG	Temperature coefficient of PBSWG	V/K	0
CTH0	Normalized thermal capacity	m.°C / (W*sec)	0
RTH0	Normalized thermal resistance	m.°C/W	0
NTRECF	Temperature coefficient for NRECF	-	0
NTRECR	Temperature coefficient for NRECR	-	0
XBJT	Power dependence of jbjt on temperature	-	1
XDIF	Power dependence of jdif on temperature	-	XBJT
XREC	Power dependence of jrec on temperature	-	1
XTUN	Power dependence of jtun on temperature	-	0

Table 5. The additional parameters to BSIM3v3 correspond to the BSIM3SOI PD Version 2.1 model.

- An instance parameter vbsusr is provided for users to set the transient initial condition of the body potential;
- The new-charge thickness capacitance model introduced in BSIM3v3.2, CAPMOD3, is included.

New version BSIM3SOI PD v2.1 includes the binning feature to enhance the model flexibility and fixes some bugs found in the previous version 2.0.1.

Model Parameters

The additional parameters to BSIM3v3 listed in Table 5 correspond to the BSIM3SOI PD Version 2.1 model.

Silvaco Improvements

Options

The options VZERO and EXPERT are supported in the ***SmartSpice*** BSIM3SOI PD v2.1 model.

The option VZERO=2 allows faster runtime when large circuits are used.

The EXPERT option can be specified to detect possible problems in models, before and during simulation, such as:

- negative conductances GM, GDS and GMBS,
- negative gate capacitances.

New model parameters

New model parameters are listed in the following table:

Parameter	Description	Units	Default
VERSION	Version selector	-	2.1
SMART	Improvement selector	-	1
LMIN	Limit for binning	m	0.0
LMAX	Limit for binning	m	1.0
WMIN	Limit for binning	m	0.0
WMAX	Limit for binning	m	1.0

The VERSION model parameter is used to switch between the current versions 2.0.1 and 2.1. The four new model parameters (LMIN, LMAX, WMIN and WMAX) are used for binning to select a model. For the binning, Silvaco has also added the following new binned model parameters shown in Table 6.

The SMART model parameter allows to switch on Silvaco improvements which are not compatible with original Berkeley model. The SMART model parameter has been created as follows :

- if SMART = 0: the original Berkeley model is used with its different versions
- if SMART > 0: the Berkeley model is used with the following improvements:
  - incorrect implementation of model parameter AHLI has been fixed;
  - the limitation of vb has been modified.

Figures 1, 2, 3 and 4 illustrate different models.

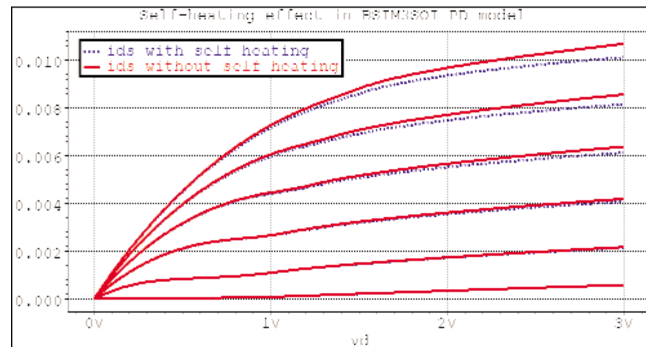

Figure 3 : Self-heating effect with PD model (default model card from Berkeley)

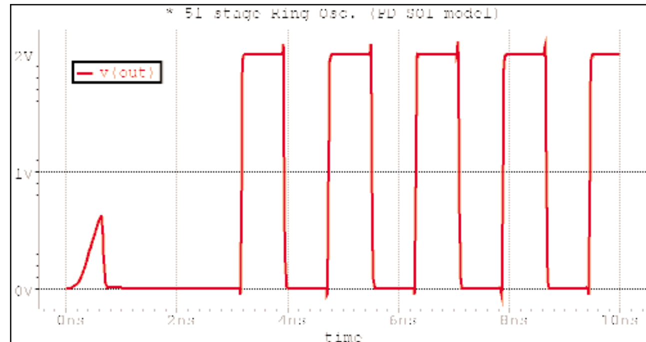

Figure 4 : Example of a ring oscillator with PD model (default model card from Berkeley)

AT	GAMMA1	GAMMA2	VBM	VBX	XT	KT1
KT1L	KT2	UA1	UB1	UC1	UTE	RTH0
PRT	CGDL	CGSL	CKAPPA	CF	CLC	CLE
XJ	RBODY	CSDMIN	CTH0	ASD	CSDESW	CJSWG
PBSWG	MJSWG	TT	XBJT	XDIF	XREC	XTUN
LN	NDIF	LDIF0	TCJSWG	TPBSWG	NTRECF	NTRECR

Table 6. Silvaco's new binned model parameters.

References

[1] BSIM3SOIFDv2.1 User's Manual, 1999, Department of EECS, University of California, Berkeley

[2] BSIM3SOIDDv2.1 User's Manual, 1999, Department of EECS, University of California, Berkeley

[3] BSIM3SOIPDv2.1 User's Manual, 1999, Department of EECS, University of California, Berkeley

New Improvements in TFT Models: Amorphous (Level=35) and Poly-Silicon (Level=36) TFT

Introduction

New improvements have been added to Shur models. These enhancements include a self-heating effect and a new charge conservative model.

Self-heating

The self-heating effect is a major feature for TFT which exhibits low thermal conductivity ([1],[2]). The self-heating is activated with SHMOD selector (model parameter). If this parameter is set to 1 and the thermal resistance is different from 0, an internal single thermal node and a thermal circuit are created. The thermal circuit includes a thermal resistance and a thermal capacitance in parallel.

Modified Device Declaration

Syntax

```
Mxxx nd ng ns mname <M> <OFF> <IC=vds, vgs>
+ <TEMP=val or DTEMP=val> <L=val> <W=val> <NRS=val>
+ <NRD=val> <AD=val> <AS=val> <PD=val> <PS=val>
+ <GEO=val> <RTH=val> <CTH=val> <NOSELFT=val>
```

New instance parameters:

RTH: Thermal resistance (deg. C / W). The default value is the model parameter RTH0.

CTH: Thermal capacitance (W.s/ deg. C). The default value is the model parameter CTH0.

NOSELFT: Selector to de-activated self-heating at device level. It overrides SHMOD model parameter. The default value is 0.

New Model Parameters

Parameter	Description	Units	Default
SHMOD (SELFT)	Self-heating selector	-	0
RTH0	Thermal resistance	°C/W	0.0
CTH0	Thermal capacitance	W.s/°C	0.0

New Output Device Variables

Parameter	Description	Units
TEMPNODE	Number of temperature node	-
TDEV	Device temperature when self-heating is turned on	deg. C
DELT	Device temperature difference when self- heating is turned on	deg. C

Characteristics

Curves Id-Vd exhibit different behavior according to parameters related to temperature. Whereas the curves show more saturation with DVTO model parameter (>0) than the curves without self-heating , the curves with DMU1 (<0) give less current and can lead to gds < 0 (Figure 1). This can be explained by the following equations:

$$Vteff = VTO - DVTO \,.\, (temp - TNOM)$$

and

$$Tmu1 = MU1 + DMU1 \cdot (temp - TNOM)$$

Since the model parameter DVTO (>0) decreases the threshold voltage, the ids current increases. On the contrary, DMU1 (<0) decreases ids current since Tmu1 (FET mobility) decreases.

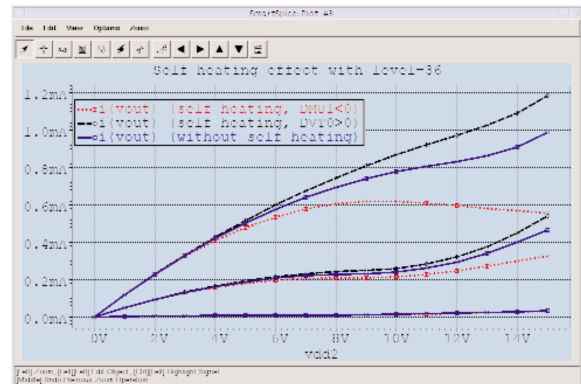

Figure 1 : Self-heating effect with level=36

New Charge Conservative Model

In Shur capacitance model, the charges qgs and qgd are numerically calculated from the capacitance capgs and capgd. This leads to problems of charge non-conservation. The charge based approach announced in [3] is presented here. This charge conservative model is selected with CAPMOD=-2 and is based on Leroux's charge model (level=15). This new model also allows speed up (factor 2.5) and simple extraction (only one parameter).

New Model Parameter

Parameter	Description	Units	Default
TC	Characteristic temperature	K	390

Description of the charge model

This charge model is the same as in level 15 (Leroux's model). Please refer to the ***SmartSpice/UTMOST*** manual for more information (equations, parameters,...) about this model charge.

New Output Device Variables

When CAPMOD = -2, the following output variables are available:

Parameter	Description	Units
QG	Gate charge	C
QD	Drain charge	C
QS	Source charge	C
CGGS	Derivative of Qg over Viss	F
CGGD	Derivative of Qg over Vidd	F
CDGS	Derivative of Qd over Viss	F
CDGD	Derivative of Qd over Vidd	F
CSGS	Derivative of Qs over Viss	F
CSGD	Derivative of Qs over Vidd	F
GCGGS	Derivative with time of Cggs	F/s
GCGGD	Derivative with time of Cggd	F/s
GCDGS	Derivative with time of Cdgs	F/s
GCDGD	Derivative with time of Cdgd	F/s
GCSGS	Derivative with time of Csgs	F/s
GCSGD	Derivative with time of Csgd	F/s
CQG	Current due to gate charge	A
CQD	Current due to drain charge	A
CQS	Current due to source charge	A

Demonstration of the Charge Conservative Feature

We have simulated a 5-stages ring-oscillator with model MOS16 (level 36) to compare the Shur capacitance model and the Leroux's charge model. We note in the following figures that whereas we do not see differences in the output voltage of the first stage (figure 2), the corresponding gate charge (figure 3) in one among transistors of the first stage is completely different. The gate charge is not conserved with the Shur model (CAPMOD=0).

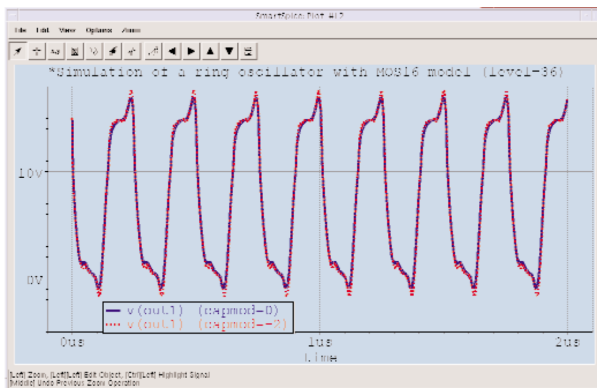

Figure 2 : Output of the first stage of a ring oscillator.

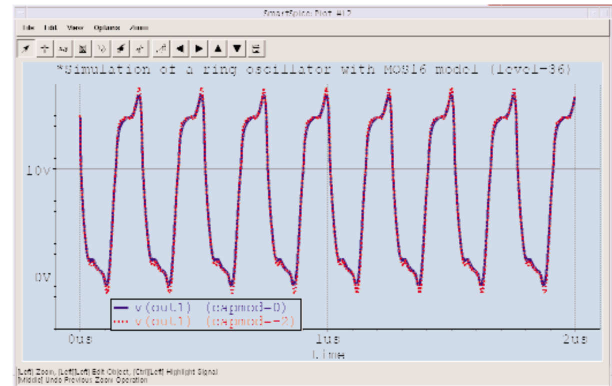

Figure 3 :Gate charge evolution of a transistor in a ring oscillator

New Improvements Selector

Smart selector has been added to select different Silvaco improvements. This selector is compatible with the existing RPI flag selector as following:

- if RPI is given, Smart = 0,
- if RPI is not given, Smart is the model parameter SMART (RPI has priority over SMART);
- if SMART = 0, this is equivalent to RPI given,
- if SMART = 1, this is the Silvaco implementation of the Shur model with some corrections (equivalent to RPI not given in the previous version of ***SmartSpice***);
- if SMART = 2, this is equivalent to SMART = 1 with new limitations. The new limitations allows to reduce up to a factor 2 the number of iterations during an OP analysis.

By default, SMART = 2 (the default is the last improvement)

References

[1] M. S. Shur and al., "Modeling and scaling of a-Si:H and Poly-Si Thin Film Transistors", Material Research Society Proceeding, Amorphous and Microcrystalline Silicon Technology, 467, 1997.

[2] G. A. Armstrong and al., "Modeling of Laser-Annealed Polysilicon TFT Characteristics", IEEE Electron Device Letters, vol. 18, No. 7, July 1997.

[3] "New parameters for TFT model : Amorphous (level=35)and Polysilicon (level=36) TFT", Simulation Standard, Volume 10, Number 1, January 1999, pp 9.

Calendar of Events

October

1
2
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4 Intrnl' SOI Conference, Rohnert Park, CA
5 Intrnl' SOI Conference, Rohnert Park, CA
6 Intrnl' SOI Conference, Rohnert Park, CA
7 Intrnl' SOI Conference, Rohnert Park, CA
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17 GaAs IC Tech, Monterey, CA
18 GaAs IC Tech, Monterey, CA
19 GaAs IC Tech, Monterey, CA
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November

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7 ICCAD, San Jose, CA
8 ICCAD, San Jose, CA
9 ICCAD, San Jose, CA
10 ICCAD, San Jose, CA
11 ICCAD, San Jose, CA
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13 SuperComputing 99, Portland, OR
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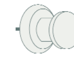
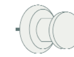
Bulletin Board



SUN Rises on Silvaco

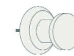
Concluding a 7-month, comprehensive evaluation of leading SPICE simulators, SUN Microsystems has signed a significant 5-year contract with Silvaco International. **SmartSpice is now the official, company wide SPICE simulator for SUN.** This is a major SPARC in the brushfire of support for the clear industry leader: Silvaco's ***SmartSpice***!



DMOS European Project

Silvaco International has been selected to participate in the development of a new DMOS compact model. The development will be funded by the European Community Research Office out of Brussels.

The main objective is to develop and validate a new unified model for lateral DMOS transistors for the design of advanced circuits. The new model will be physically based, scalable and usable for DMOS devices in sub-micron technologies. The participants of this European project in addition of Silvaco are: EPFL, ALCATEL, Microelectronics, Robert BOSH and IMEC.



Grand Opening of a Major Silvaco Technology Center

Chelmsford, Massachusetts is the home of Silvaco's new 18,000 square foot office building. On December 1st, after 8 months of construction, our Northeast Sales and Support team moved into a structure identical to Silvaco itself; strong, proud, and solid as a rock.

The office will be managed by Mr. Micheal Ridenger. You can contact him at:

phone: 978-452-2000
fax: 978-452-6488

For more information on any of our workshops, please check our web site at ***http://www.silvaco.com***

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Hints, Tips and Solutions

Mustafa Taner, Applications and Support Engineer

Q. How can I re-measure a certain device in the middle of BSIM3_MG routine's data collection without closing and re-opening the log file?

A. It is likely that there may be some contact problems or defected devices during the data collection. This problem can occur when the log file is open and some good device data has already been stored in the log file. Then it becomes a time consuming process to close the log file, deselect the good devices from the device strategy screen, append the log file and re-measure the device which created the problem.

In order to simplify this process, "Re_Measure Last Plot" feature was developed. The user can re-measure the device which didn't have good data by pressing the "Re_Measure" button and selecting the "Last plot" Menu option in the Graphics Screen. (Figure 1.) During the "Re-measure Last Plot" operation the log file can stay open. ***UTMOST*** will automatically overwrite the last device data with latest measured data.

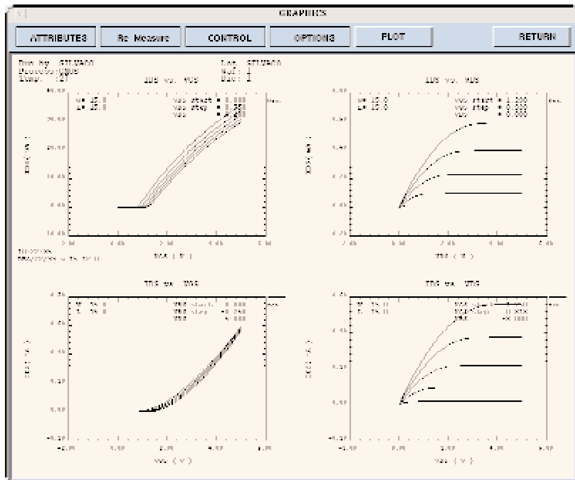

Figure 1. BSIM3_MG routine Graphics Screen showing the "Re-Measure" button.

Q. What are the available routines in UTMOST SOI module for measuring the parasitic bulk diode and Bipolar effects in SOI devices?

A. There were number of routines developed in ***UTMOST III*** SOI module to characterize the parasitic diode or bipolar effects. All parasitic effect characterization routines require devices with body contact for measurements and 5 Terminal selection for simulation. Summary of these routines are:

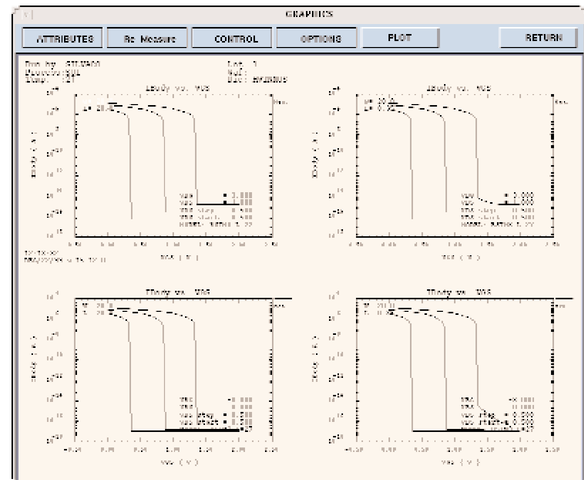

Figure 2. IB/VG_MG Characteristics.

IB/VG_MG Routine: This routine is used to measure IBody current versus VGS at different VDS steps and different Bulk voltage steps. The user can also specify the Back Gate voltage during the measurements. The IB/VG_MG routine can be used for multiple geometry measurements.

IB/VB_MG Routine: This routine is used to measure IBody current versus Bulk voltage (VB) at different VGS steps. IB/VB_MG Routine allows users to bias the Back Gate , Drain and Source terminals with constant voltage sources. The IB/VB_MG routine can be used for multiple geometry measurements.

IC/VCE Routine: This routine is used to characterize the parasitic bipolar effects in SOI devices. IC/VCE routine can measure IDrain versus Vdrain characteristics

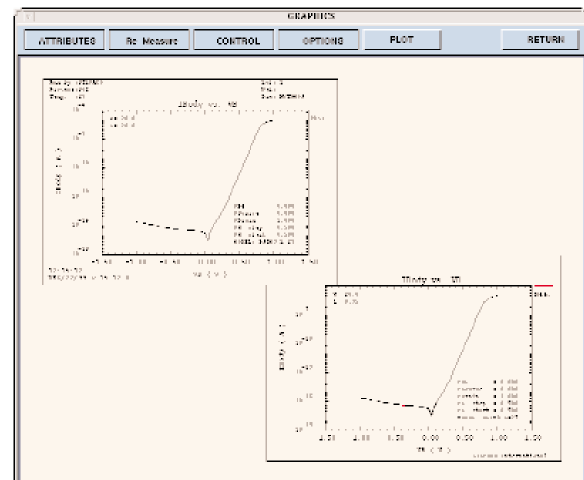

Figure 3. IB/VB_MG Characteristics.

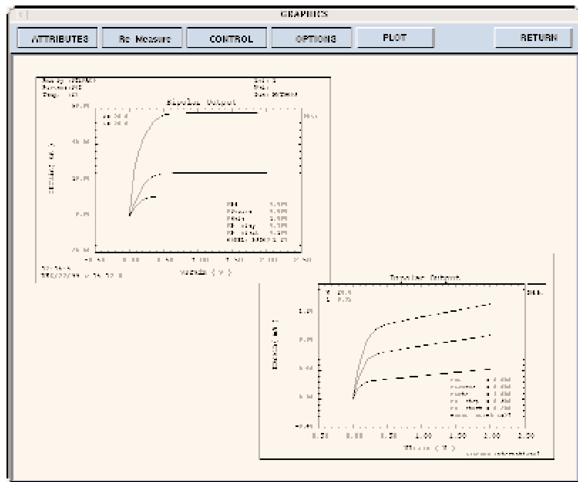

Figure 4. IC/VCE Characteristics.

at different VBulk voltage steps. The user can bias the Back Gate, Drain and Source terminals with constant voltage sources. The IC/VCE routine can be used for multiple geometry measurements.

DIODE Routine: This routine can be used to measure the Drain-Body and Source-Body diodes. The displayed results will present the IBody versus VBulk characteristics. The VGS voltage can be stepped during the measurement. The user can also bias the Back Gate , Drain and Source terminals with constant voltage sources. In order to measure only Drain to Bulk diode without any additional source terminal current, the Source terminal is left floating during the measurement. The Drain terminal is left floating during the Source to Bulk diode measurements. The DIODE routine can be used for multiple geometry measurements.

Gummel Routine: This routine is used to measure IBody and Idrain currents versus Vbody voltage. The measured data is similar to the Gummel characteristics of a bipolar device. The Gummel routine allows users

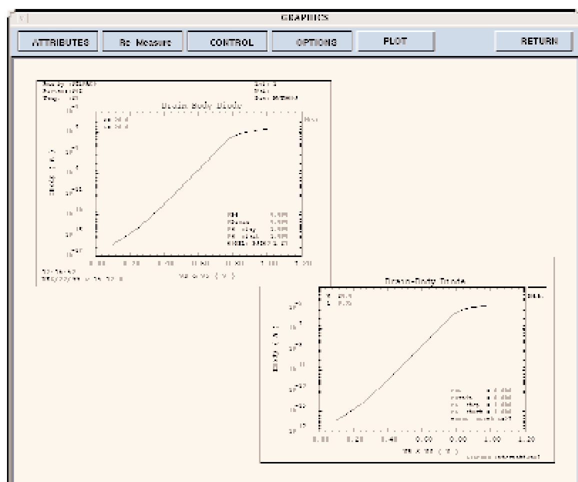

Figure 5. DIODE Characteristics.

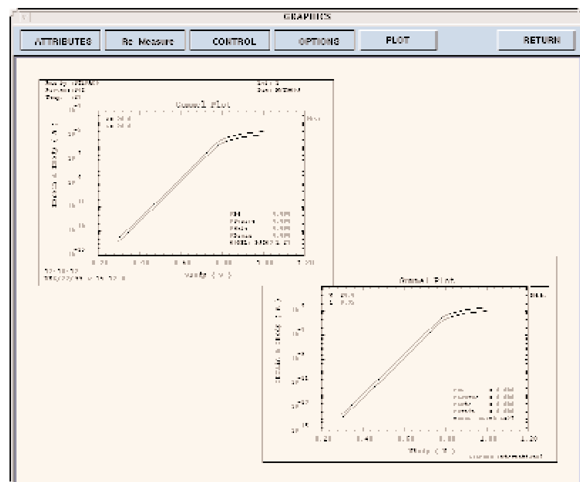

Figure 6. Gummel Characteristics.

to bias the Back Gate, Drain and Source terminals using constant voltage sources. The Gummel routine can be used for multiple geometry measurements.

GP_VS Routine: The GP_VS routine is similar to the Gummel routine. However in GP_VS routine the IBody and IDrain currents are measured against the Vsource voltage. The Drain, Gate, Bulk and Back Gate terminals can be biased using constant voltage sources. The GP_VS routine can be used for multiple geometry measurements.

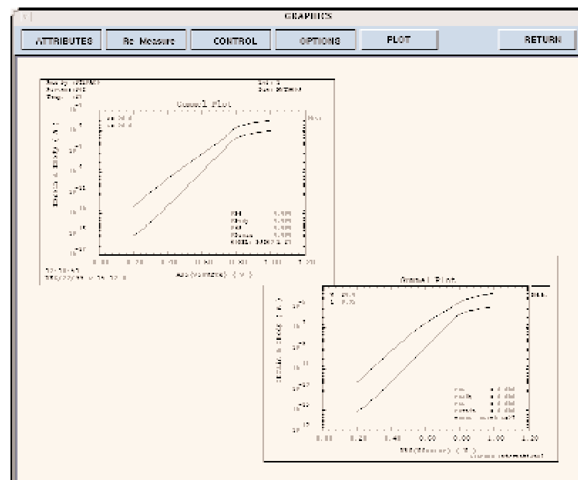

Figure 7. GP_VS Characteristics.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

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Silvaco International
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Santa Clara, CA 95054
USA

Phone: 408-567-1000
Fax: 408-496-6080

sales@silvaco.com
www.silvaco.com

CONTACTS:

Silvaco Japan
jpsales@silvaco.com

Silvaco Korea
krsales@silvaco.com

Silvaco Taiwan
twsales@silvaco.com

Silvaco Singapore
sgsales@silvaco.com

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