New Improvements in TFT Models: Amorphous (Level=35) and Poly-Silicon (Level=36) TFT

Introduction

New improvements have been added to Shur models. These enhancements include a self-heating effect and a new charge conservative model.

Self-heating

The self-heating effect is a major feature for TFT which exhibits low thermal conductivity ([1],[2]). The self-heating is activated with SHMOD selector (model parameter). If this parameter is set to 1 and the thermal resistance is different from 0, an internal single thermal node and a thermal circuit are created. The thermal circuit includes a thermal resistance and a thermal capacitance in parallel.

Modified Device Declaration

Syntax

```
Mxxx nd ng ns mname <M> <OFF> <IC=vds, vgs>
+ <TEMP=val or DTEMP=val> <L=val> <W=val> <NRS=val>
+ <NRD=val> <AD=val> <AS=val> <PD=val> <PS=val>
+ <GEO=val> <RTH=val> <CTH=val> <NOSELFT=val>
```

New instance parameters:

RTH: Thermal resistance (deg. C / W). The default value is the model parameter RTH0.

CTH: Thermal capacitance (W.s/ deg. C). The default value is the model parameter CTH0.

NOSELFT: Selector to de-activated self-heating at device level. It overrides SHMOD model parameter. The default value is 0.

New Model Parameters

Parameter	Description	Units	Default
SHMOD (SELFT)	Self-heating selector	-	0
RTH0	Thermal resistance	°C/W	0.0
CTH0	Thermal capacitance	W.s/°C	0.0

New Output Device Variables

Parameter	Description	Units
TEMPNODE	Number of temperature node	-
TDEV	Device temperature when self-heating is turned on	deg. C
DELT	Device temperature difference when self- heating is turned on	deg. C

Characteristics

Curves Id-Vd exhibit different behavior according to parameters related to temperature. Whereas the curves show more saturation with DVTO model parameter (>0) than the curves without self-heating , the curves with DMU1 (<0) give less current and can lead to gds < 0 (Figure 1). This can be explained by the following equations:

$$Vteff = VTO - DVTO \,.\, (temp - TNOM)$$

and

$$Tmu1 = MU1 + DMU1 \cdot (temp - TNOM)$$

Since the model parameter DVTO (>0) decreases the threshold voltage, the ids current increases. On the contrary, DMU1 (<0) decreases ids current since Tmu1 (FET mobility) decreases.

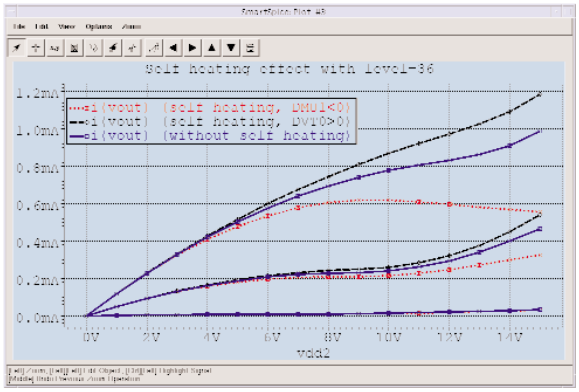

Figure 1 : Self-heating effect with level=36

New Charge Conservative Model

In Shur capacitance model, the charges qgs and qgd are numerically calculated from the capacitance capgs and capgd. This leads to problems of charge non-conservation. The charge based approach announced in [3] is presented here. This charge conservative model is selected with CAPMOD=-2 and is based on Leroux's charge model (level=15). This new model also allows speed up (factor 2.5) and simple extraction (only one parameter).

New Model Parameter

Parameter	Description	Units	Default
TC	Characteristic temperature	K	390

Description of the charge model

This charge model is the same as in level 15 (Leroux's model). Please refer to the ***SmartSpice/UTMOST*** manual for more information (equations, parameters,...) about this model charge.

New Output Device Variables

When CAPMOD = -2, the following output variables are available:

Parameter	Description	Units
QG	Gate charge	C
QD	Drain charge	C
QS	Source charge	C
CGGS	Derivative of Qg over Viss	F
CGGD	Derivative of Qg over Vidd	F
CDGS	Derivative of Qd over Viss	F
CDGD	Derivative of Qd over Vidd	F
CSGS	Derivative of Qs over Viss	F
CSGD	Derivative of Qs over Vidd	F
GCGGS	Derivative with time of Cggs	F/s
GCGGD	Derivative with time of Cggd	F/s
GCDGS	Derivative with time of Cdgs	F/s
GCDGD	Derivative with time of Cdgd	F/s
GCSGS	Derivative with time of Csgs	F/s
GCSGD	Derivative with time of Csgd	F/s
CQG	Current due to gate charge	A
CQD	Current due to drain charge	A
CQS	Current due to source charge	A

Demonstration of the Charge Conservative Feature

We have simulated a 5-stages ring-oscillator with model MOS16 (level 36) to compare the Shur capacitance model and the Leroux's charge model. We note in the following figures that whereas we do not see differences in the output voltage of the first stage (figure 2), the corresponding gate charge (figure 3) in one among transistors of the first stage is completely different. The gate charge is not conserved with the Shur model (CAPMOD=0).

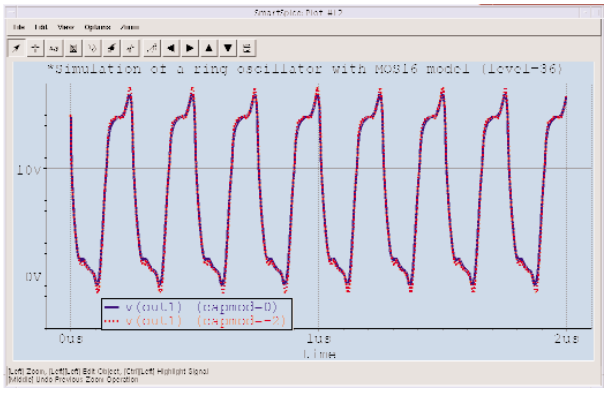

Figure 2 : Output of the first stage of a ring oscillator.

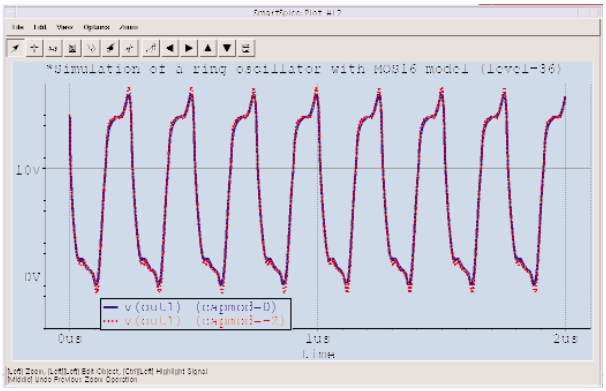

Figure 3 :Gate charge evolution of a transistor in a ring oscillator

New Improvements Selector

Smart selector has been added to select different Silvaco improvements. This selector is compatible with the existing RPI flag selector as following:

- if RPI is given, Smart = 0,
- if RPI is not given, Smart is the model parameter SMART (RPI has priority over SMART);
- if SMART = 0, this is equivalent to RPI given,
- if SMART = 1, this is the Silvaco implementation of the Shur model with some corrections (equivalent to RPI not given in the previous version of ***SmartSpice***);
- if SMART = 2, this is equivalent to SMART = 1 with new limitations. The new limitations allows to reduce up to a factor 2 the number of iterations during an OP analysis.

By default, SMART = 2 (the default is the last improvement)

References

[1] M. S. Shur and al., "Modeling and scaling of a-Si:H and Poly-Si Thin Film Transistors", Material Research Society Proceeding, Amorphous and Microcrystalline Silicon Technology, 467, 1997.

[2] G. A. Armstrong and al., "Modeling of Laser-Annealed Polysilicon TFT Characteristics", IEEE Electron Device Letters, vol. 18, No. 7, July 1997.

[3] "New parameters for TFT model : Amorphous (level=35)and Polysilicon (level=36) TFT", Simulation Standard, Volume 10, Number 1, January 1999, pp 9.