Simulation Standard

TCAD Driven CAD

A Journal for Process and Device Engineers

The Industry Standard of SOI Technology From Process To Circuit Simulation

Abstract

SOI technology for state of the art CMOS technology is rapidly approaching maturity. PD-SOI device design has the advantage of easier manufacturing but requires more sophisticated device and circuit design to reduce the effects of the floating-body. FD-SOI device design potentially has the advantage of no floating-body effects but requires very thin silicon films making manufacturing more challenging. As a consequence the optimization of SOI device design requires a coupled solution where both process and circuit simulation can be tied together. Silvaco provides a complete, well integrated simulation software for all aspects of SOI technology. Our SOI specific software includes technology simulation, SPICE model extraction, interconnect parasitic analysis, SPICE circuit simulation and traditional CAD. The ***TCAD Driven CAD*** approach provides the most accurate models for both device engineers and circuit designers.

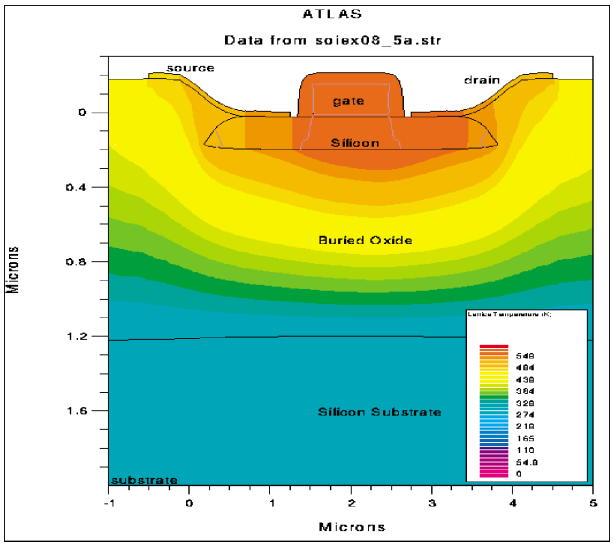


Figure 1. Short channel SOI MOSFET created using ***ATHENA***. Local oxidation is used to isolate the active layer. Here temperature distribution is shown due to self heating.

1 Introduction

The continuing trend for high speed circuits has resulted in a market increase in the application of Silicon-On-Insulator (SOI) MOSFETs. Consequently a number of phenomena, such as the presence of floating body effect, carrier heating and non-localized transport, have acquired a lot of importance in the field of semiconductor modeling. Not only they are interesting from a theoretical point of view but also play a relevant role in the functioning of devices and circuits and for this reason, need to be simulated very accurately. In this paper we will show how Silvaco's software simulator now accounts for all the specific SOI related physics from process technology simulation to circuit level including interconnect parasitics extraction.

2 Technology Simulation

The ***ATHENA*** and ***ATLAS*** simulators allow device engineers to study deep sub-micron physical effects in SOI devices. Technology simulation includes models for simulation of both fully and partially depleted SOI transistors based on accurate process geometry and doping profiles. ***ATHENA*** can model local oxidation to form silicon islands (Figure 1), shallow implant, RTA diffusion process steps and physical etching. ***ATLAS*** provides among common models for BULK and SOI technologies, the following SOI specific device simulation features: Impact Ionization model for breakdown and kink effect, self heating model for negative differential resistance simulation (Figure 2).

Continued on page 2....

INSIDE

SILVACO INTERNATIONAL

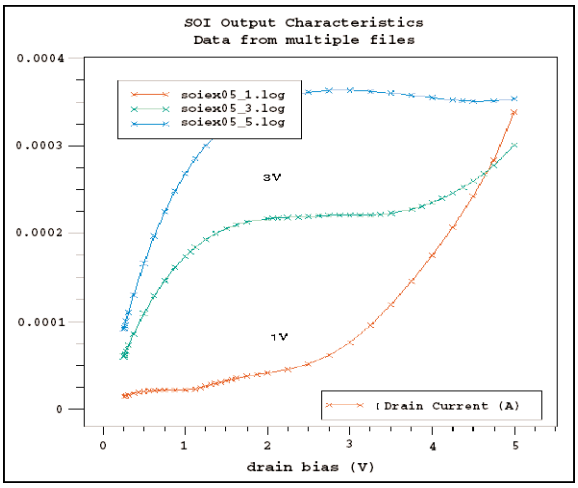


Figure 2. The impact of Self Heating is shown on Drain IV curves for SOI devices.

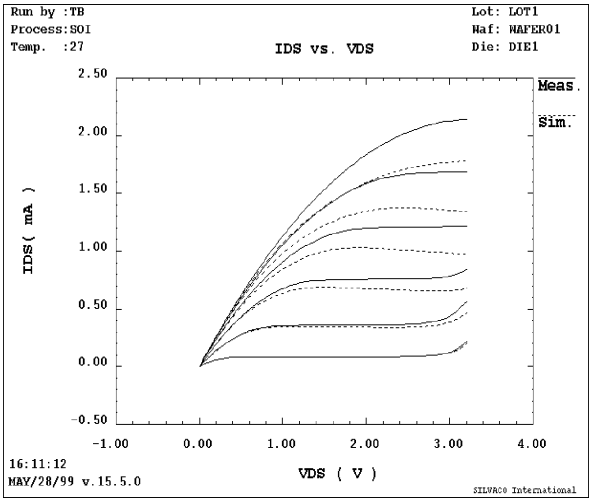


Figure 3 Global or local optimization and parameter extraction can be performed on up to 40 geometries to obtain a single scalable model.

3 Parameters Extraction

UTMOST is a complete integrated software package which provides automatic data acquisition, parameters fitting and extraction, optimization, simulation and model validation. ***UTMOST*** supports the following models: Honeywell, Florida FD and PD, STAG, BSIM3SOI (Figure 3). Thus, a complete solution is now available to fully characterize SOI devices including parasitic effects (Bipolar, diode) on either 4 or 5 terminals devices.

4 Circuit Simulator

SOI circuits pose unique problems for reliable and accurate circuit simulation. SPICE-like programs are not designed to handle negative conductances forcing designers to simulate circuits for only positive gate voltages. ***SmartSpice*** has been improved to accept any bias conditions and provide accurate and reliable SOI simulations. Some of Silvaco's fundamental improvement to BSIM3SOI model are the optimization of the Impact Ionization model and the self heating model (Figure 4).

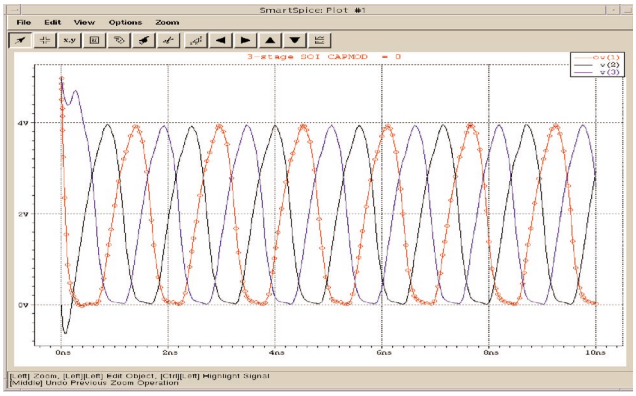


Figure 4. ***SmartSpice*** waveform from high speed digital circuit designed with fully depleted SOI devices.

5 Interconnect Parasitic Extraction from Layout

SOI devices are being used in complex deep sub-micron circuits. An accurate physical calculation of interconnect delay is important to successfully design circuit with this technology [1][2][3]. ***CLEVER*** is a physical interconnect parasitic extractor built on 3D process simulation and fast field solution techniques (Figure 5) and (Figure 6). ***CLEVER*** generates fully annotated SPICE netlist for circuit simulation (extract active devices and associated geometrical parameters (W,L,NRS,NRD,AD,PD). It can model: floating silicon islands, low-k and damascene processing, handle multiple metals and di-electrics, lithography effects including optical proximity correction and physical deposition and etch.

Continued on page 5....

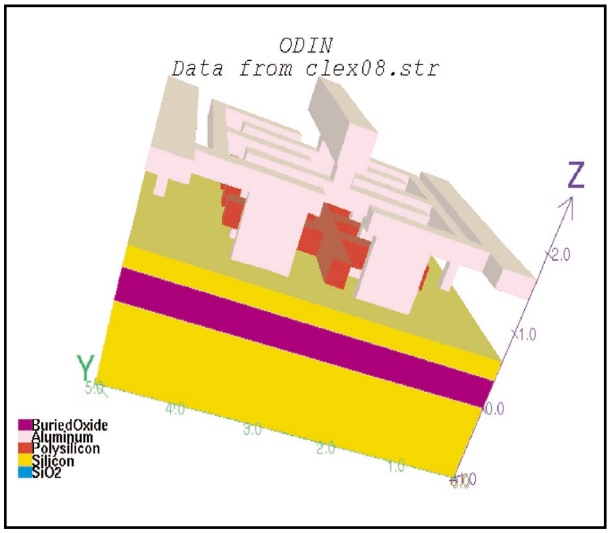


Figure 5. 3D Interconnect geometry from SOI cell layout. CLEVER applies a field solver to the 3D structure to calculate parasitics from the interconnect.

Optoelectric Device Simulation of a Dual-Base BJT Using *Luminous*

Introduction

With the continuing emergence of optical technologies, optoelectronic device structures are becoming increasingly important for modern telecommunications and data network applications. Like other semiconductor technologies, two-dimensional numerical simulation can be an invaluable tool for studying and understanding semiconductor device behavior in response to optical stimulation. This article seeks to demonstrate the simulation of optoelectric device structures using ***Luminous***.

The first section of the article discusses briefly the capabilities of ***Luminous*** and how it models the interaction of light with semiconductor materials. The following sections briefly overview the methodology for optoelectric simulation using ***Luminous*** and present the optoelectric simulation results for a dual-base BJT structure.

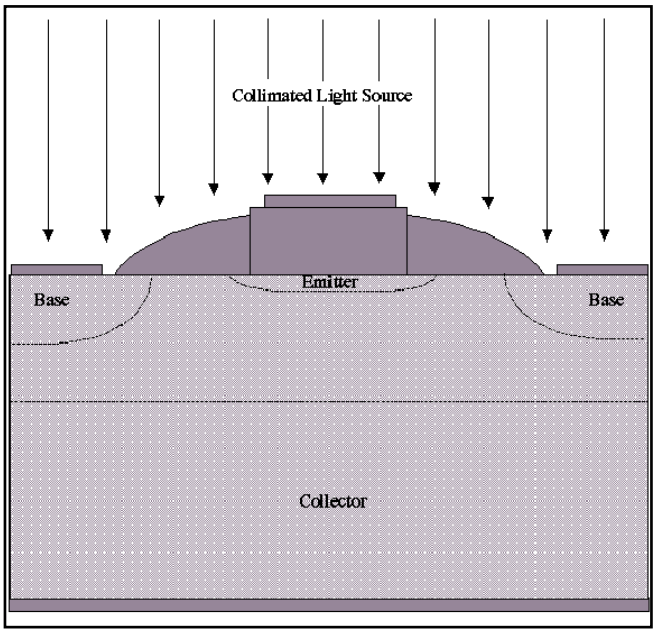


Figure 1. Diagram of dual-base BJT structure used for optoelectric device structure.

Background

Luminous is the general purpose ray trace and light absorption program available within the ***ATLAS*** framework. Designed to model light absorption and photogeneration in non-planar semiconductor devices, ***Luminous*** provides the capability to simulate DC, AC, transient, and spectral responses of generic device structures in the presence of arbitrary optical sources. ***Luminous*** is applicable to a wide array of device technologies including, but not limited to, pn and pin photodiodes, optical transistors, solar cells, and charged coupled devices (CCDs). Optoelectronic simulation within ***Luminous*** is separated into two distinct models.

The optical ray tracing model uses the real component of the optical index of refraction for a given semiconductor material to calculate optical intensity at each simulation grid point. By using this geometric model, ***Luminous*** is able to account for arbitrary topologies, internal and external reflections and refraction, polarization dependencies and dispersion. In ***Luminous***, an optical beam is modeled as a collimated source entering the device through a prescribed illumination window. To resolve topological differences, ***Luminous*** automatically splits the beam into a series of rays covering the width of the illumination window. The optical rays are further separated into transmitted and reflected rays as they cross material interfaces.

```
File  View  Edit  Find  Main Control  Commands  Tools

go atlas

# read in device structure
mesh inf=bjt.str

# specify models
models consrh auger conmob fldmob print

# obtain initial solution
solve init

# define beam
beam num=1 x.origin=0 y.origin=-1 angle=90 wavelength=0.8

# specify solution scheme
method gummel newton trap

# solve
solve b1=1 vcollector=0.5

ATHENA started                                    ATHENA
```

Figure 2. Example input deck for optoelectric device simulation.

The second model accounts for absorption and photogeneration within the device structure. Using the imaginary component of the optical index of refraction, the carrier concentrations are calculated at each simulation point as follows:

$$G = \eta_0 \frac{P^*\lambda}{hc} \alpha e^{-\alpha y}$$

P* represents the cumulative effects of reflections, transmissions, and loss due to absorption over the ray path, η_0 is the internal quantum efficiency (representing the number of carrier pairs generated per photon observed), y is a relative distance for the ray in question, h is Planck's constant, λ is the wavelength, and c is the speed of light. α is the absorption coefficient defined as:

$$G = \eta_0 \frac{P^*\lambda}{hc} \alpha e^{-\alpha y}$$

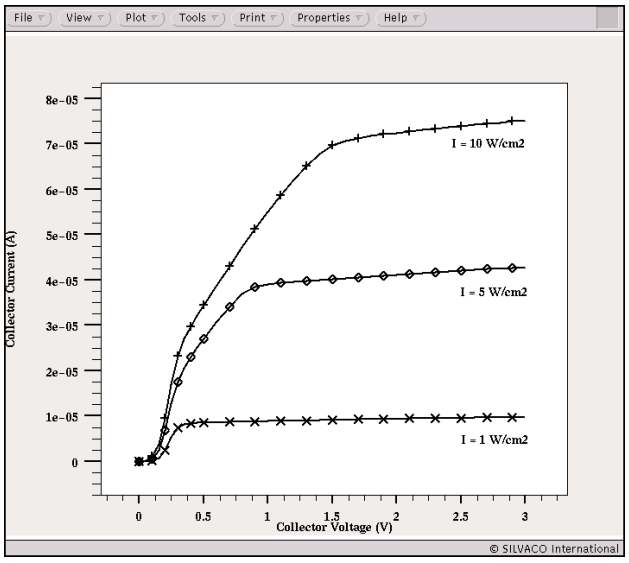


Figure 3. Common-emitter output characteristics (Ic vs. Vce) for dual-base BJT.

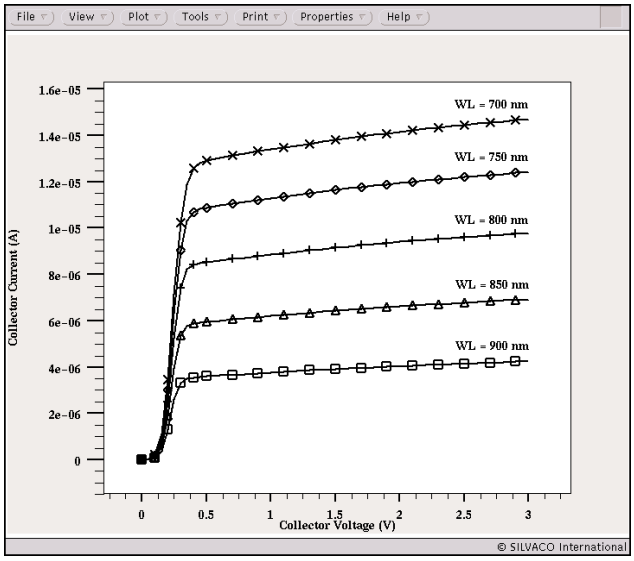


Figure 4. Common-emitter output characteristics (Ic vs. Vce) for dual-base BJT.

where k is the imaginary component of the optical index of refraction. The cumulative effects of the reflection coefficients, transmission coefficients, and the integrated loss due to absorption over the ray path are saved for each ray. In ***Luminous***, the optical ray trace model and the adsorption/ photogeneration model are calculated at each DC bias point or transient time step prior to electrical simulation. The calculated carrier concentrations are then used within ***S-Pisces*** or ***Blaze*** to calculate the terminal currents.

Simulation Setup

A diagram of the dual-base BJT device structure used for this work is presented in Figure 1. The structure was created using the general purpose process simulator ***ATHENA***. Optoelectric simulations are initiated through the definition of one or more optical sources.

Optical sources are specified in the form of a collimated beam of light using the BEAM statement. The minimum set of conditions necessary to conduct an optoelectric simulation include the beam's origin (x,y coordinates), its wavelength, and its propagation angle in relation to the semiconductor surface.The source's intensity is specified using the SOLVE statement. Figure 2 presents an example input deck for an optoelectric simulation using ***Luminous***. Here, the BEAM statement specifies a single optical source (labeled numerically as 1) originating one micron above the semiconductor surface. The source's wavelength λ is 0.8 µm, or 800 nm, and it enters the device vertically (90 degrees from the horizontal axis). The second SOLVE statement specifies

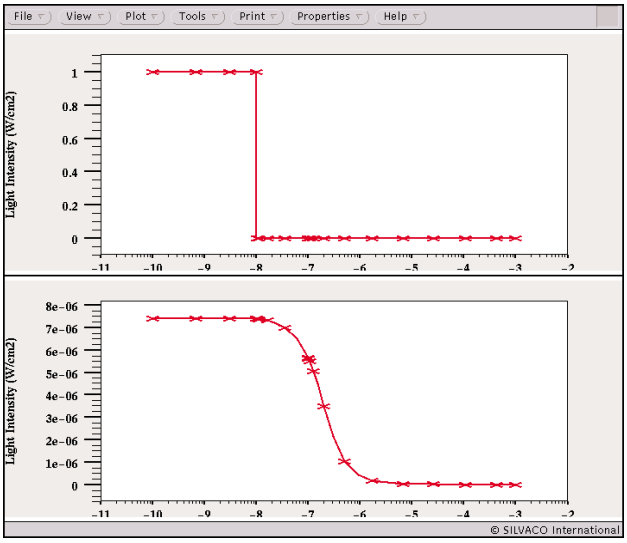


Figure 5. Device turn-off characteristics of dual-base BJT (in seconds). Source intensity = 1 W/cm², Source wavelength = 800 nm.

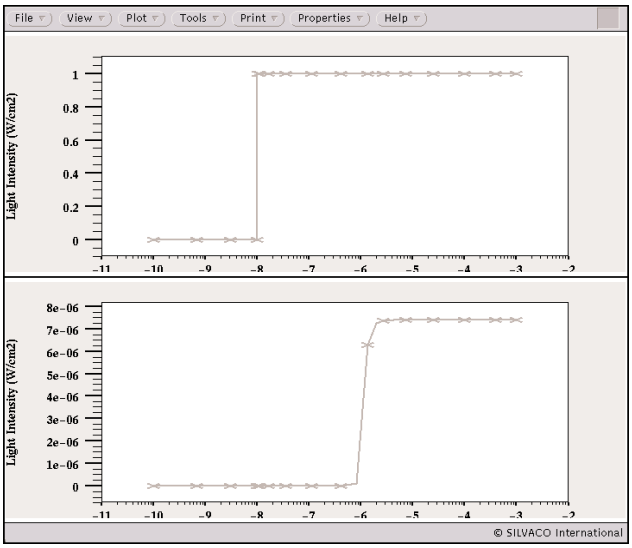


Figure 6. Device turn-on characteristics of dual-base BJT (in seconds). Source intensity = 1 W/cm², Source wavelength = 800 nm.

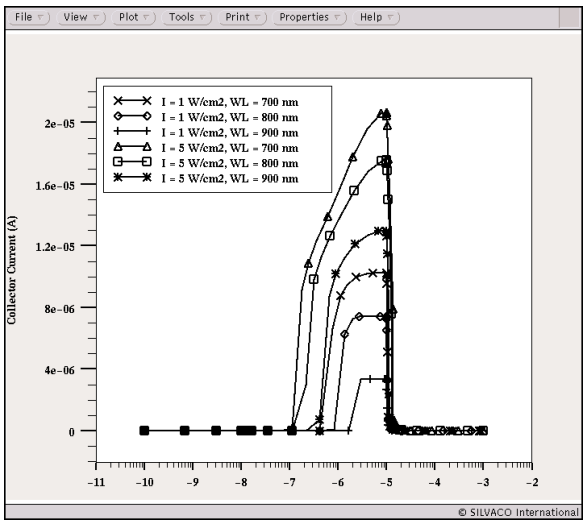


Figure 7. Device pulse response of dual-base BJT (in seconds) for varying source intensities and wavelengths.

a solution for a collector voltage of 0.5V and a light intensity of 1 W/cm^2. More advanced controls of the optical source (including definition of multi-spectral sources) are available using the BEAM statement, but are outside the scope of this article.

Results

To demonstrate optoelectric device simulation using ***Luminous***, a series of DC and transient analyses were conducted on a dual-base BJT structure. For all analyses, the emitter was grounded and the base and collector acted as the input and output terminals, respectively. The optical source was the only source of current in the base areas of the device.

Figure 3 presents the common-emitter output characteristics (Ic vs Vce) of the dual-base BJT for varying levels of light intensity. As shown, three levels of light intensity were simulated: 1, 5, and 10 W/cm^2. As the light intensity increases, the collector current, output conductance, and saturation voltage all increase. Figure 4 presents the same output characteristics for varying wavelengths of light. The wavelength was stepped from 700 to 900 nm in increments of 50 nm. As shown, the saturation current is inversely proportional to the wavelength of light and both the output conductance and saturation voltage remain constant.

Figure 5 presents the turn-off characteristics of the dual-base BJT. Initially on, the optical source (intensity = 1 W/cm^2, wavelength = 800 nm) was removed after 10 ns. The fall time was approximately 0.7 µs. Here, fall time was defined as the time required for Ic to reach 10% of its initial value. Figure 6 presents the turn-on characteristics of the BJT. Initially off, the device was illuminated after 10 µs (intensity = 1 W/cm^2, wavelength = 800 nm). Defined as the time for the output current to reach 90% of its final value, the rise time of the dual-base BJT was approximately 7 µs.

Figure 7 presents the device's response to a pulse of light with varying intensities and wavelengths. The device was illuminated after 10 ns and the light source was removed after 10 us. The wavelength was varied from 700 to 900 nm in increments of 100 nm. The intensity was stepped from 1 to 5 W/cm2.The device exhibits the same basic behavior seen in Figures 5 and 6.

Summary

The accurate simulation of optical processes in semiconductors is a valuable tool for the development of current and future optoelectric device structures. This article presented an overview of the optoelectric device simulation capabilities of ***Luminous***. The basic device models incorporated in ***Luminous*** were presented, an example input deck for completing an optoelectric device simulation was included, and the results of the DC and transient simulation results for a dual-base BJT device structure were discussed.

...continued from page 2

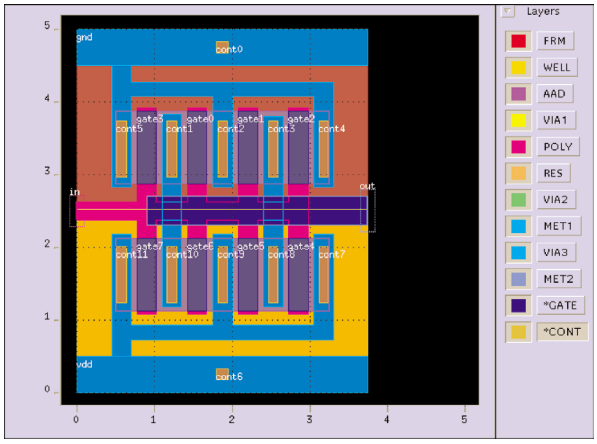


Figure 6. SOI cell layout from which 3D back end process simulation is based.

Conclusion

It has been shown that Silvaco's software is able to simulate and predict adequately state of the art SOI technology from process to circuit simulation.

References

[1] B.Froment et al,, "New interconnect capacitance characterization method for mutilevel CMOS processes" IITC 1999.

[2] Gilles Lecarval et al, 'Advanced Intercoonect Scheme Analysis: Real Impact of Technological Improvements" IEDM 1998

[1] B.Froment et al, "Ultra Low capacitance measurements in Multilevel metallisation CMOS by using q built-in Electronmeter" IEDM1999.

Modelling Tunneling Currents in Ultra Thin Oxides

I. Introduction

Ever decreasing minimum geometries in MOSFET design results in a corresponding reduction in the thickness of the gate oxide. This is an inevitable result of the increasing doping levels in the channel that are required to prevent depletion from the drain becoming too high a percentage of the total device length. For these new aggressive technologies, the required ultra thin gate oxides suffer a significant oxide tunnelling component. It has therefore become important to include this component in device modelling.

For some time now, Silvaco has had models to deal with current conduction through oxides. It is only recently, however, that the number of questions to the customer support groups related to gate tunnelling effects has been increasing. It is appropriate, therefore to re-address this issue at this time.

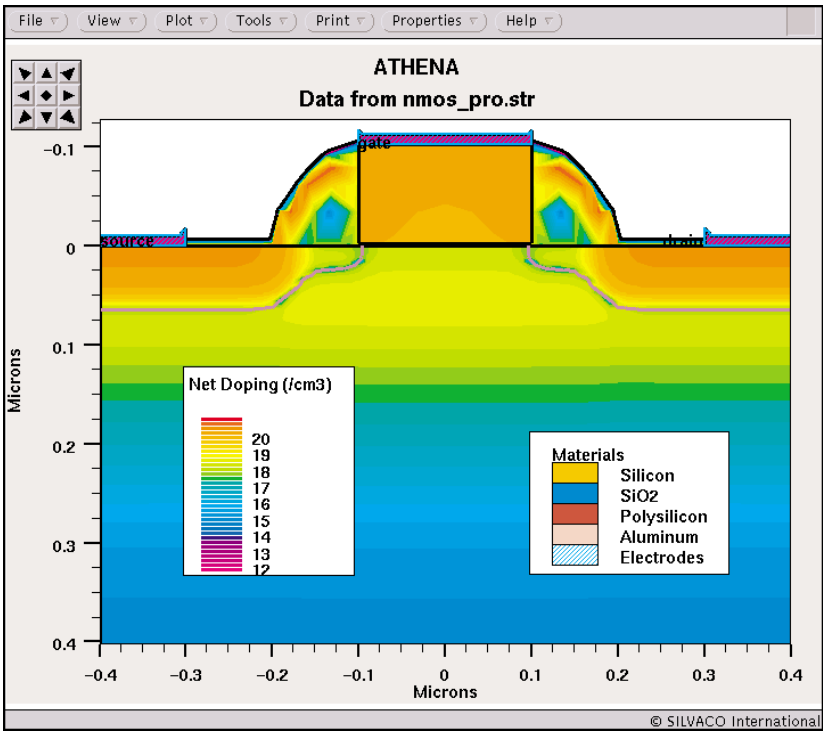


Figure 1. The typical 0.2um MOSFET with 25A gate oxide used in this example.

There are two types of models in Silvaco's device simulator, ***ATLAS***, which address oxide current conduction.

(i) Fowler Nordheim Tunnelling

(ii) Hot Carrier Injection.

The essential difference between these two components of current arises from from the direction of the field that is accelerating the mobile carriers.

Hot carrier injection occurs when a high local electric field exists in the same direction as the oxide/semiconductor interface. The statistics of huge numbers of free carriers travelling at high velocity results in a probability that some of them, through multiple "lucky" collisions, will attain sufficient energy to surmount the oxide/silicon energy barrier and thus enter into the oxide. Once in the oxide, electrons and holes have a low but finite mobility to move around or become trapped. This mechanism of hot carrier injection is usually studied in relation to reliability issues or for memory devices where mobile carriers in the oxide are used to to charge or discharge an isolated floating gate. Users requiring more information and worked examples on this mechanism are directed towards the "EPROM" section in the ***DeckBuild*** examples menu.

Fowler Nordheim tunnelling, on the other hand, arises from high local fields perpendicular to an energy barrier interface. An energy barrier interface can be induced by the presence of a semiconductor with a different band gap, in which case it is called a "hetero-junction" or it can be induced by the presence of an insulator. The insulator interface is the situation which is of most interest to silicon MOSFET designers and is the subject of this article.

II. Requirements for Modelling Tunnelling in *ATLAS*

ATLAS offers two types of model for electron or hole tunnelling that are specified in the "MODELS" statement.

(i) Post Processing Fowler Nordheim Model (FNPP)

(ii) Self Consistent Fowler Nordheim Model (FNORD)

The Post Processing model (FNPP) is a very stable model which will work for any situation. This model simply calculates the current flowing through the gate once ***ATLAS*** has found a solution to each solve statement and adds this current to the gate electrode. The presumption here is that the gate current is a small

```
File  Edit  Format  Options                    Help
go atlas

mesh infile=nmos_pro.str
models cvt srh fnord
method climit=1e-4
output efield flowlines

solve init
solve vdrain=0.005
solve vdrain=0.05

log outfile=nmos_pro.log
solve vgate=0.005
solve vgate=0.02 vstep=0.1 vfinal=0.42 name=gate
solve vgate=0.5 vstep=0.05 vfinal=0.75 name=gate
solve vgate=0.9 vstep=0.25 vfinal=5.4 name=gate
save outfile=nmos_pro_bd.str
```

Figure 2. The entire device simulation input file used in this example.

fraction of the total terminal currents, since clearly with this method, adding all terminal currents will no longer equal zero. For small gate leakage currents, however, this is of little consequence.

The self consistent model, FNORD, has the tunnelling equations inside the solution loop and therefore correctly calculates all terminal currents. This self consistent method, however, does require one condition for reliable convergence, namely:

> there must be a majority carrier source of the tunnelling species within a depletion width of the tunnelling oxide interface.

For most structures, such as MOSFETs, the above requirement is satisfied and good convergence should ensue.

III. Worked Example

The most common situation where oxide tunnelling is modelled is for deep sub-micron MOSFETs with very thin oxides. Figure 1 shows a typical MOSFET created using the process models in ***ATHENA***. To exaggerate the effect of oxide tunnelling, a gate oxide of 25A nominal thickness was grown. The structure called "nmos_pro.str" was then imported into ***ATLAS*** and the gate oxide ramped to a voltage of 5.4 volts with a typical applied drain voltage of 50mV. The entire simulation deck is shown in Figure 2 for those who may wish to use this example as a starting point for their own device simulations. It is evident from this input file how simple it is to do these simulations.

The results of the simulation are shown in Figure 3. It is observed from these results that tunnelling current through the gate was mostly at the expense of drain current in this case. The small drain bias was applied to to demonstrate the self consistency of the solution method by monitoring the drain current.

IV. Conclusion

The Fowler Nordheim oxide tunnelling models in ***ATLAS*** are simple to implement and assist in the study of deep sub-micron MOSFETs gate current effects. The study here shows that for a gate oxide thickness of 25A in a typical MOSFET structure, gate oxide current can exceed the drain current for a applied gate voltages greater than 5 volts.

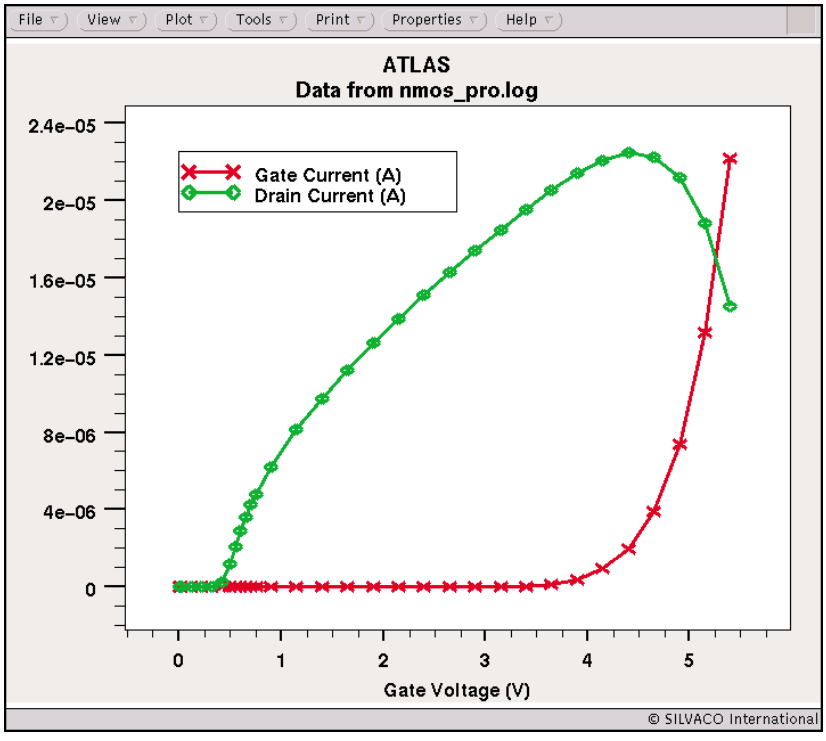


Figure 3. The simulated gate and drain currents of the device shown in Figure 1 demonstrating the self consistent Fowler Nordheim oxide tunnelling model in ***ATLAS***.

Modeling Bidirectional Thyristors Using *ATLAS*

Part 1: The Steady-State

Introduction

Thyristors are semiconductor devices that exhibit multi-stable or bi-stable electrical characteristics, and can be switched between a high-impedance OFF state and a low-impedance ON state. Bidirectional thyristors are particularly useful for ac applications because they operate in the first and third quadrants of the I-V curve, depending on the anode and cathode polarities. It is useful to simulate and predict the important electrical characteristics of these devices, so they can be optimized for figures-of-merit such as breakover voltage, holding current, and switching speed.

In Part 1, we examine the principal voltage-current characteristics of two diac (diode ac switch) structures: the *ac trigger diode* and the *p-n-p-n diode switch*. In the next issue of the *Simulation Standard*, we will examine the transient electrical behavior of the *p-n-p-n diode switch* for large current pulses typically associated with ESD and other discharge phenomena. This characterization typically requires 3-D simulation of z-plane effects due to asymmetry of the electric fields in the device.

AC Trigger Diode

Figure 1 shows a typical ac trigger diode structure, constructed like a bipolar transistor with no base contact and equally doped emitter and collector regions. When either bias is applied to a contact, one junction is forward-biased and the other is reverse-biased. The current is limited initially by the reverse-biased junction leakage at lower voltages, and the device eventually breaks down at $V_{br} = BV_{CBO}\,(1-\alpha)^{1/n}$, where α is the common-base current gain, BV_{CBO} is the avalanche

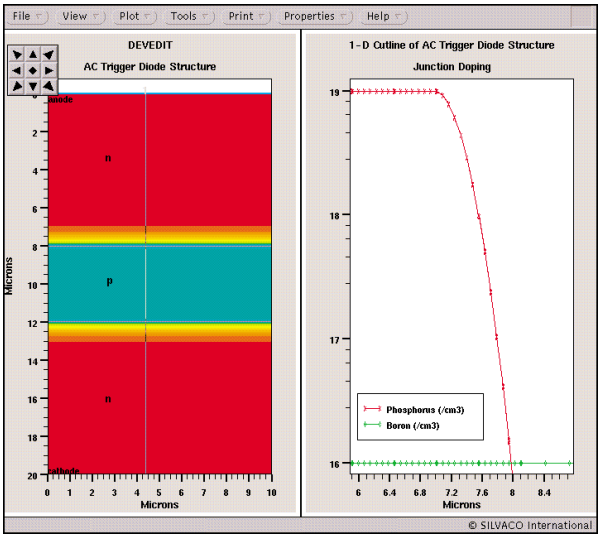


Figure 1. AC trigger diode structure created in ***DevEdit***.

breakdown voltage of the reverse-biased *p-n* junction, and n is an empirical constant [1]. As the current increases after breakdown, α increases, causing a drop in contact voltage and negative-resistance region shown in Figure 2.

The data of Figure 2 was simulated in ***ATLAS*** from a device created analytically using the ***DevEdit*** device editor in 2-D mode. The solution was obtained in one sweep using the ***Curvetrace*** automatic curve tracing routine in ***ATLAS***. The sweep ends when the controlling current contact reaches a current compliance limit of 20 µA / µm.

Continued on page 11....

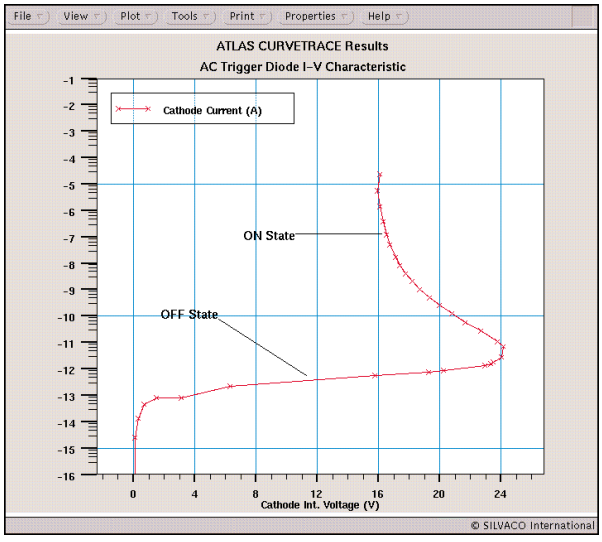


Figure 2. Simulated I-V characteristic of AC trigger diode structure from ***ATLAS*** Curvetrace routine.

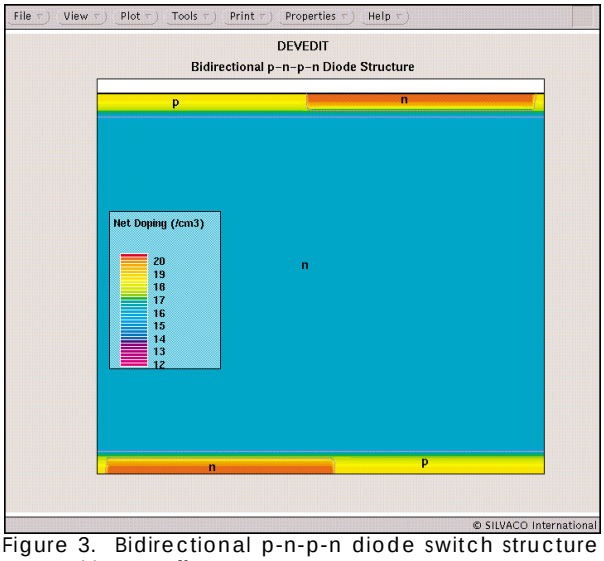


Figure 3. Bidirectional p-n-p-n diode switch structure created in ***DevEdit***.

Calendar of Events

November

1	
2	
3	
4	
5	
6	
7	ICCAD, San Jose, CA
8	ICCAD, San Jose, CA
9	ICCAD, San Jose, CA
10	ICCAD, San Jose, CA
11	ICCAD, San Jose, CA
12	
13	SuperComputing 99, Portland, OR
14	SuperComputing 99, Portland, OR
15	SuperComputing 99, Portland, OR
16	SuperComputing 99, Portland, OR
17	SuperComputing 99, Portland, OR
18	SuperComputing 99, Portland, OR
19	SuperComputing 99, Portland, OR
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	

December

1	
2	
3	
4	
5	IEDM - Washington D.C.
6	IEDM - Washington D.C.
7	IEDM - Washington D.C.
8	IEDM - Washington D.C.
9	
10	
11	
12	
13	
14	
15	
15	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	

Bulletin Board

CNFM Contract

Silvaco is proud to announce the signature of a new CNFM contract where more than 12 French Universities will have the opportunity to use 2D and 3D ***ATHENA*** and ***ATLAS*** (Process and Device simulators) as well as ***UTMOST*** (parameter extraction simulator) for educational purposes.

Announcing HF-EXACT

HF-EXACT is an advanced tool dedicated to high frequency geometric test pattern characterization. Using a new technique based on fictitious domain (IEDM 99, IITC 98) parasitic resistance, capacitance and inductance are extracted in the frequency domain as a function of design or process parameters. ***HF-EXACT*** allows resistance, capacitance and inductance model generation using response model surface. ***HF-EXACT*** currently has no competitors and is a badly needed solution to high frequency parasitic modeling.

STELLAR 2D is Born

Stellar 2D is a revolutionary approach to cell and macro-cell characterization. Based on the fictitious domain technique, ***STELLAR 2D*** extracts parasitics resistance, capacitance and inductance over a very wide GHz range of frequncies. Fast and accurate parasitic extraction is mandatory for ultra deep sub-micron designs and ***STELLAR 2D*** fills the void.

If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

William French, Applications and Support Manager

Q: Can ATLAS model the CV behavior of an MOS capacitor ?

A: ***ATLAS/S-Pisces*** and ***ATLAS/Blaze*** both have a small signal ac analysis capability built into them. This analysis is based upon the work of S.Laux [1] and results in the extraction of the Y parameter matrix. These Y parameters contain the conductance and capacitance information for each electrode in the device. This information allows the user to examine the frequency behavior of the CV simulation and also other parameters such as interface fixed charge, doping , oxide thickness, etc.

Small signal analysis can be switched on by syntax found on the SOLVE statement. The user can simulate a bias ramp and perform a small signal analysis at one frequency using the syntax

```
SOLVE VSTEP=0.1 VFINAL=1.0 NAME=GATE AC
FREQ=1E6
```

It is also possible to solve one bias condition and to sweep the frequency of the applied small signal voltage or to do both simultaneously.

In the simulation of the CV curves shown below it is important to include Shockley-Read-Hall recombination mechanisms. In addition, a useful tip when performing such simulations is to introduce additional generation mechanisms such as from a light source. This will ease the reproduction of some the characteristics. In this work a light source above the silicon has been defined using the BEAM statement

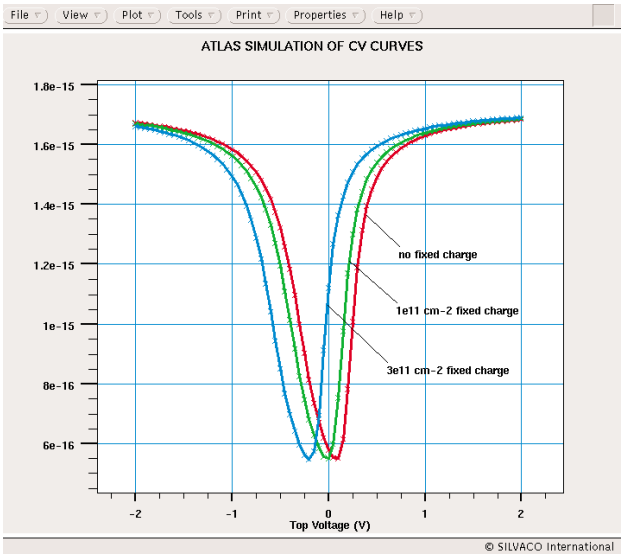


Figure 2

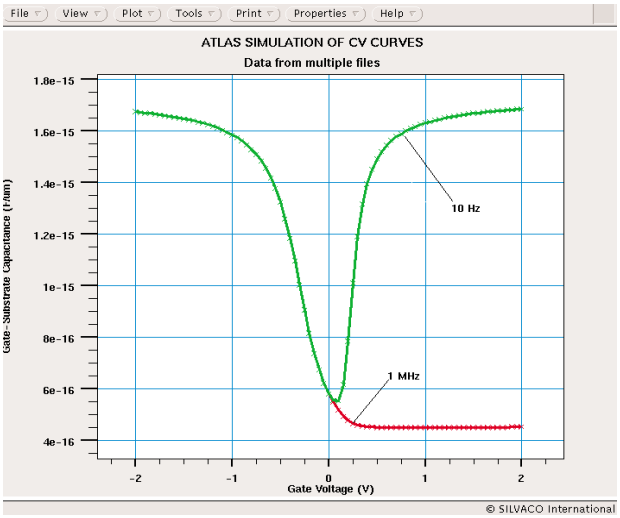


Figure 1

```
BEAM NUM=1 WAVELENGTH=0.6
X.ORIG=0.5 Y.ORIG=-1 ANG=90
RAYS=10
```

A simple MOS capacitor has been chosen to show some simulated CV characteristics. It is well known that a MOS capacitor has two parts; the oxide capacitance (a constant) and the depletion capacitance (voltage dependent). When the surface is in accumulation the oxide capacitance will dominate but as the surface moves into depletion, the depletion region formed acts as a dielectric in series with the gate oxide and so the total capacitance will decrease. However, two different curves will be produced depending upon the frequency of the applied small signal [2].

Figure 1 shows the simulated gate to substrate capacitance at two frequencies, 1MHz and 10 Hz. At the low frequency the channel electrons are able to be modulated by the applied small signal and the inversion layer will act to “screen” the depletion region. As a result the total gate capacitance will begin to increase and finally reach the gate oxide capacitance value. At the high frequency the recombination-generation rates of minority carriers cannot keep up with the signal variation and therefore the inversion region appears transparent and the total gate capacitance remains low.

ATLAS also allows the definition of fixed interface charge with the statement

INTERFACE QF=1e11

Figure 2 shows the low frequency CV curves at different fixed charge values. As expected the CV curve shifts along the voltage axis.

References

[1] S.E. Laux, "Techniques for Small Signal Analysis of Semiconductor Devices", IEE Trans. Elect. Devices, ED-32, pp. 2028-2037, 1985.

[2] S.M.Sze, Physics of Semiconductor Devices", Wiley, 1967.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

Phone: (408) 567-1000 Fax: (408) 496-6080

e-mail: *support@silvaco.com*

Hints, Tips and Solutions Archive

Check our our Web Page to see more details of this example plus an archive of previous Hints, Tips, and Solutions

www.silvaco.com

...continued from page 8

Bidirectional p-n-p-n Diode Switch

Figure 3 shows a bidirectional p-n-p-n diode, or 5-layer diode structure, as created in ***DevEdit***, based on an actual device (thus no direct geometric information is shown). If we consider a vertical axis of symmetry dividing the structure in to left and right halves, we can see two conventional Shockley diodes connected in anti-parallel. The structure can therefore be triggered into conduction by dV/dt, by exceeding the breakover voltage, or by increasing the temperature and saturation current until the common-base current gains sum to one. Also, due to the common-base current gains, the 5-layer thyristor will have carrier generation features, a larger range of negative resistance, and a smaller forward drop than the ac trigger diode. Figure 4 illustrates the simulated current-voltage characteristics of the p-n-p-n diode switch structure. Figure 5 shows the simulated impact ionization rate just before breakdown, and the current density at turn-on.

Another important feature of the p-n-p-n diode is the emitter overlap, evident in Figure 3. This overlap creates a lateral current path, increasing the lateral voltage drop for a given current density, and helping to trigger the device at a lower current density. In Part 2 of this series, we will consider the operation of the p-n-p-n diode in greater detail, and also examine the introduction of emitter shunts, which break the monolithic emitter into curved areas, decreasing the associated electric fields and allowing greater control of critical voltages and currents [2].

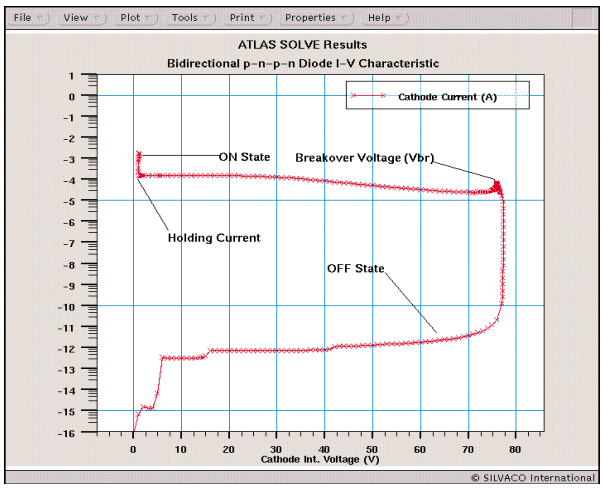


Figure 4. Simulated I-V characteristic of p-n-p-n diode from ***ATLAS***.

Summary

The current-voltage characteristics of two classes of bidirectional thyristor structures is described theoretically and simulated using the ***ATLAS 2-D*** device simulator in automatic curve trace mode and in standard voltage/current driven solution modes. Simulated results of steady-state I-V curves for the ac trigger diode and for the p-n-p-n diode are typical for these devices. Physical models used in the simulation solutions are standard drift-diffusion with Boltzmann carrier statistics, Shockley-Read-Hall recombination, concentration-dependent low-field mobility and parallel electric field-dependent high-field mobility, bandgap narrowing, and the Selberherr impact ionization models.

In Part 2 we analyze temporal behavior of the bidirectional p-n-p-n diode switch in three dimensions, based on more complex thermal and impact ionization models. This analysis will allow us to understand the mechanisms and geometries of the device that may be optimized using simulation.

Rerences

[1] S.M. Sze, Physics of Semiconductor Devices, 2nd Edition, John Wiley & Sons, New York, 1981.

[2] A. Blicher, Thyristor Physics, Springer-Verlag, New York, 1976.

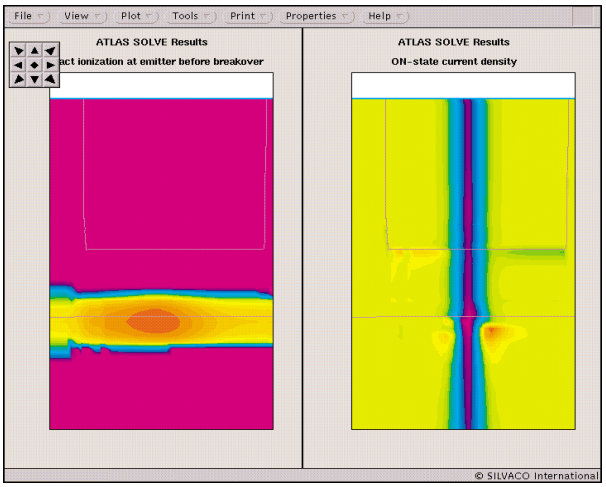
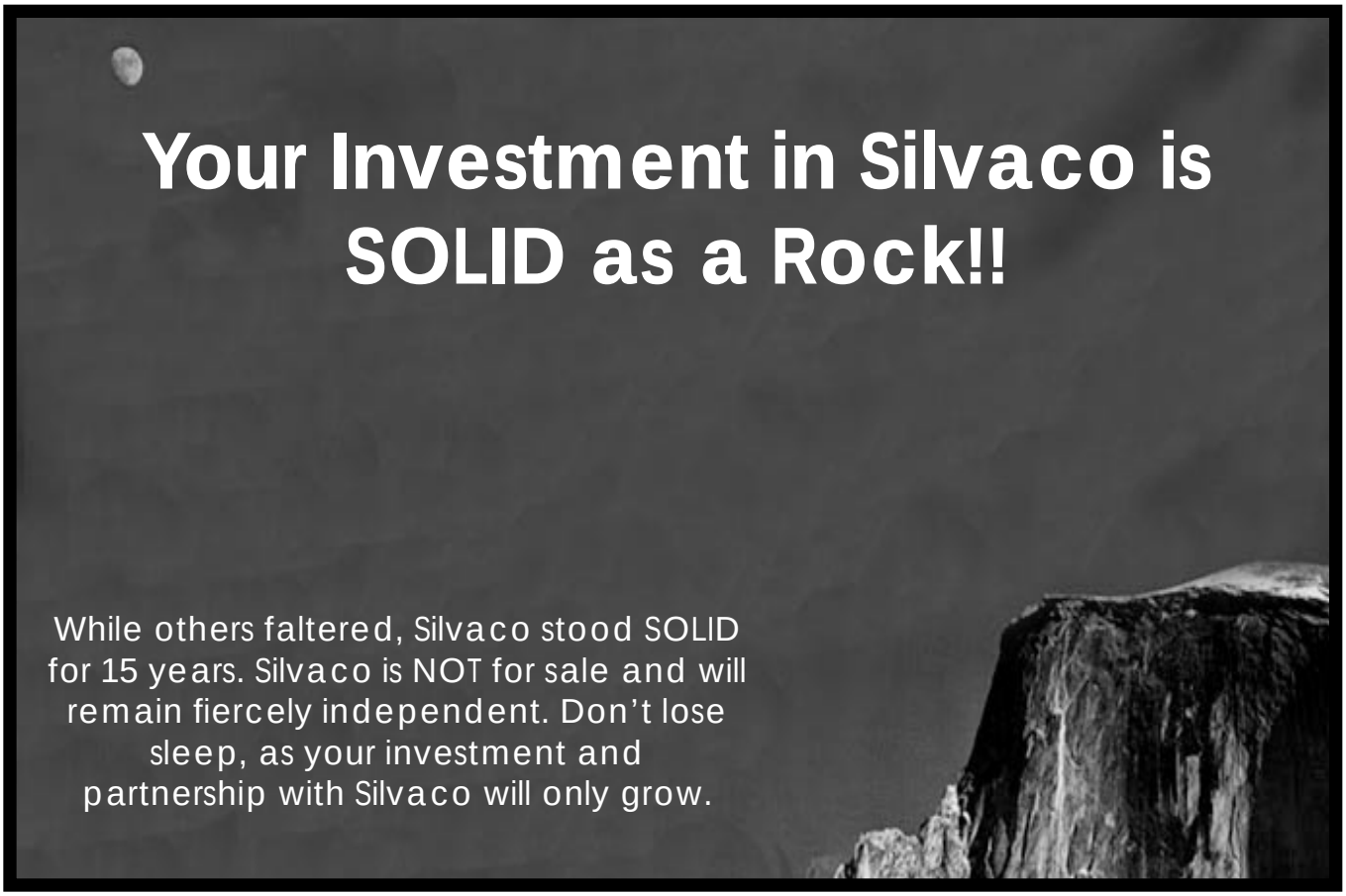


Figure 5. Simulated impact ionization rate at breakdown and total current density after device turn-on.



SILVACO INTERNATIONAL

USA HEADQUARTERS

Silvaco International
4701 Patrick Henry Drive
Building 2
Santa Clara, CA 95054
USA

Phone: 408-567-1000
Fax: 408-496-6080

sales@silvaco.com
www.silvaco.com

CONTACTS:

Silvaco Japan
jpsales@silvaco.com

Silvaco Korea
krsales@silvaco.com

Silvaco Taiwan
twsales@silvaco.com

Silvaco Singapore
sgsales@silvaco.com

Silvaco UK
uksales@silvaco.com

Silvaco France
frsales@silvaco.com

Silvaco Germany
desales@silvaco.com

Products Licensed through Silvaco or e*ECAD

e*ECAD
Vendor Partner