Hints, Tips and Solutions

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Q: Can ATLAS model the CV behavior of an MOS capacitor ?

A: ***ATLAS/S-Pisces*** and ***ATLAS/Blaze*** both have a small signal ac analysis capability built into them. This analysis is based upon the work of S.Laux [1] and results in the extraction of the Y parameter matrix. These Y parameters contain the conductance and capacitance information for each electrode in the device. This information allows the user to examine the frequency behavior of the CV simulation and also other parameters such as interface fixed charge, doping , oxide thickness, etc.

Small signal analysis can be switched on by syntax found on the SOLVE statement. The user can simulate a bias ramp and perform a small signal analysis at one frequency using the syntax

```
SOLVE VSTEP=0.1 VFINAL=1.0 NAME=GATE AC
FREQ=1E6
```

It is also possible to solve one bias condition and to sweep the frequency of the applied small signal voltage or to do both simultaneously.

In the simulation of the CV curves shown below it is important to include Shockley-Read-Hall recombination mechanisms. In addition, a useful tip when performing such simulations is to introduce additional generation mechanisms such as from a light source. This will ease the reproduction of some the characteristics. In this work a light source above the silicon has been defined using the BEAM statement

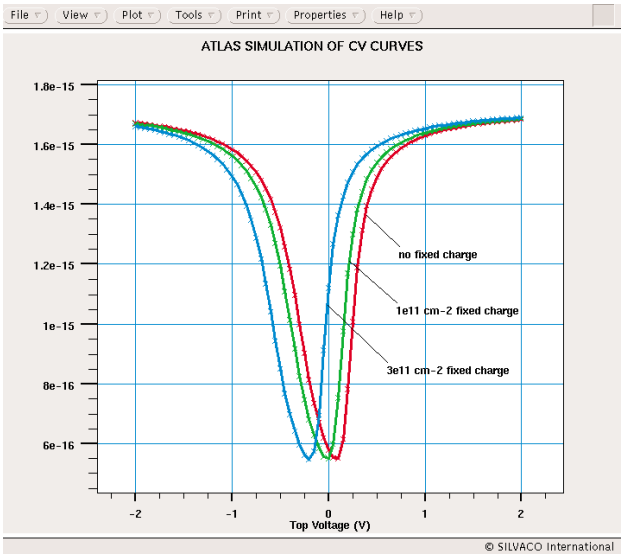

Figure 2

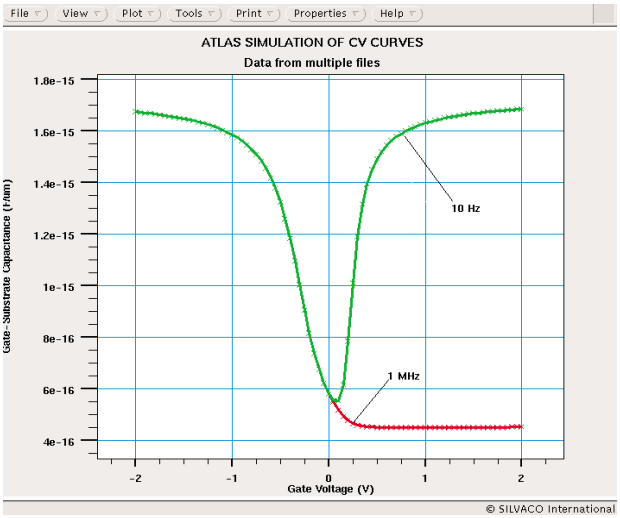

Figure 1

```
BEAM NUM=1 WAVELENGTH=0.6
X.ORIG=0.5 Y.ORIG=-1 ANG=90
RAYS=10
```

A simple MOS capacitor has been chosen to show some simulated CV characteristics. It is well known that a MOS capacitor has two parts; the oxide capacitance (a constant) and the depletion capacitance (voltage dependent). When the surface is in accumulation the oxide capacitance will dominate but as the surface moves into depletion, the depletion region formed acts as a dielectric in series with the gate oxide and so the total capacitance will decrease. However, two different curves will be produced depending upon the frequency of the applied small signal [2].

Figure 1 shows the simulated gate to substrate capacitance at two frequencies, 1MHz and 10 Hz. At the low frequency the channel electrons are able to be modulated by the applied small signal and the inversion layer will act to “screen” the depletion region. As a result the total gate capacitance will begin to increase and finally reach the gate oxide capacitance value. At the high frequency the recombination-generation rates of minority carriers cannot keep up with the signal variation and therefore the inversion region appears transparent and the total gate capacitance remains low.

ATLAS also allows the definition of fixed interface charge with the statement

INTERFACE QF=1e11

Figure 2 shows the low frequency CV curves at different fixed charge values. As expected the CV curve shifts along the voltage axis.

References

[1] S.E. Laux, "Techniques for Small Signal Analysis of Semiconductor Devices", IEE Trans. Elect. Devices, ED-32, pp. 2028-2037, 1985.

[2] S.M.Sze, Physics of Semiconductor Devices", Wiley, 1967.

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